# IRPS

International Reliability Physics Symposium

# 2016 IRPS Conference Proceedings

IEEE

Electron Devices Society

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# Intro

For 59 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world.

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Sang Woo Pae, Samsung
Shinji Yokogawa, Polytechnic U. of Japan
Nagarajan Raghavan, Singapore U. of Technology and Design

# Topics of Interest

## SPECIAL FOCUS TOPICS

IRPS16 is soliciting increased participation in the following areas: Self-heating effects on transistors and circuits aging, Consumer Electronics, Reliability of 2D NAND Flash replacement technologies, Packaging

## Circuits and Products

**Circuit Reliability** – Includes digital, mixed-signal, and RF applications; design for reliability

**Circuit Aging Simulation** – Includes compact modeling; statistical methods

**Product IC Reliability** – Includes burn-in; defect detection; on-chip sensors; modeling

**Consumer Electronics Reliability** – Includes smart phones; wearable devices; tablets; ultrabooks; health devices

**Electronic System Reliability** – Includes automotive, space, communications, medical, energy, and photovoltaic applications; screening techniques; system monitoring; failure root cause determination; modeling methodologies

**Soft Errors** – Includes neutron and alpha particle SER; multi-bit SER/SEU; mitigation techniques; simulation

**3D Assembly** – Includes multichip modules; 3D integration with TSV; thermomechanical stress; wafer thinning effects

**Packaging** – Includes chip-package interaction; fatigue; power dissipation issues

## Device, Process, and Materials

**Transistors** – Includes hot carrier phenomena; biastemperature instability; random telegraph noise; advanced transistor scaling challenges; Ge and III-V channels

**Gate Dielectrics** – Includes TDDB modeling; reliability of novel gate dielectrics; modeling of progressive breakdown; gate dielectric reliability for III-V FETs

**Beyond CMOS Devices** – Includes reliability of tunnel FETs, transistors with 2D semiconductor (graphene, MoS2), and spintronics

**Compound/Opto Electronics** – Includes reliability of wide bandgap (GaN, SiC) power devices, optoelectronics, and silicon photonics

**Back-end Reliability** – Electromigration; Joule heating; stress migration; low-k dielectric breakdown. Includes middle of the line

**Process Integration** – Includes new process related reliability issues; foundry reliability challenges

**Failure Analysis** – Includes evidence of new failure mechanisms; advances in failure analysis techniques

**Memory** – Includes DRAM and NVM; failure mechanisms in novel memory devices including 3D Flash and ReRAM

**ESD and Latchup** – Includes component and systemlevel ESD design; modeling and simulation

# Program

*NOTE – For full Program, including Abstracts and Speaker information, view Appendix*

*VIDEOS – https://www.youtube.com/user/IEEEIRPS/videos*

# Keynote Speakers

## Keynote 1

### "Implications for System Reliability in Future Industrial and Automotive Designs"

Scott Roller, Vice President Systems Engineering and Marketing, Texas Instruments

## Keynote 2

### "Driverless Vehicles? The Journey Ahead"

Raj Rajkumar, George Westinghouse Professor, Carnegie Mellon University

# Tutorials

### Track 1: Technology Section F/G

- Introduction to Reliability Physics and Engineering - Joe McPherson – McPherson Reliability Consulting LLC
- FEOL Reliability – From Dielectric Trap Properties to Degradation Mechanisms and Their Distributions - Ben Kaczer and Robin Degraeve – imec
- MOL Process Integration and Reliability Assessment Challenges - Richard Southwick – IBM
- BEOL Reliability – Challenges from Technology Scaling to Chip Design and System Integration - Baozhen Li – IBM
- Wafer Level Reliability – Techniques and Models for Determining FEOL/BEOL Failure Mechanisms - Yung-Huei Lee – TSMC
- Challenges in Reliability Evaluations Due to FINFET SelfHeating Effects - Ben Kaczer and Robin Degraeve – imec
- Failure Analysis Techniques - Kevin Johnson – Intel

### Track 2: Component Section D

- MEMORY 1 – The Physics of Flash Memory Reliability - Riichiro Shirota / Hiroshi Watanabe – National Chiao Tung Univ.
- MEMORY 2 – Advanced Memory Technologies: CBRAM and OxRAM - Shosuke Fujii – Toshiba Corp
- 2.5D PACKAGING – Si Interposer, Heterogeneous Devices - Sam Gu – Qualcomm
- 3D PACKAGING – Reliability of 3D Through-Silicon-Via (TSV) Technologies - Dimitris P. Ioannou – GlobalFoundries
- CIRCUIT AGING 1 – Optimizing VLSI Circuit Reliability through Presilicon Design and Postsilicon Adaptation - Sachin S. Sapatnekar – University of Minnesota
- CIRCUIT AGING 2 – Measurement Techniques - Takashi Sato and Hidetoshi Onodera – Kyoto University
- Reliability Differences Between RF and Power Switching GaN Power Transistors - Michael J Uren – University of Bristo

### Track 3: System Section E

- An Overview of Mechanical Reliability Challenges in Electronics Across Length Scales -Shankar Ganapathysubramanian and Sudarshan Rangaraj – Amazon Lab126
- Learning from and Reduction of IC Customer Returns - Fred Kuper and Michael Stevens – NXP Semiconductors
- SECURITY – What are the interactions between hardware reliability and system security? - Swarup Bhunia – University of Florida
- Concepts for Managing System Behavior in the Presence of Hardware Faults - Jim Lewis – Oracle America Inc
- Soft Errors in Functional and System Safety Standards - Riccardo Mariani – Yogitech SpA
- ESD and EOS Design and Qualification Methods - Charvaka Duvvury – Charvaka Duvvury LLC at ESD Consultin

# Workshops

### Transistor / Circuit

WS.1 – Advanced CMOS Nodes (FDSOI, FinFET) usage for High Reliability Markets from Device and Design - Moderator: Puneet Gupta, UCLA

### BEOL

WS.2 – Challenges for EM and SM / Test Time / Power Management

Challenges for EM & SM / Test time / Power management

- Scaling trends and challenges for EM and SM, IR drop, barrier options and Blech Effect, 7nm and beyond
- Best test method and structure to reduce test time
- Power EM and interaction with package Integrated power and on die power management

Thermal effect/thermal mechanism concerns

Moderators: Ki-Don and Gavin Hall, OnSemi

### Compound

WS.3 – GaN Reliability – What is Missing? What Should be Looked at Beyond What's Already Known? - Moderators: Jungwoo Joh (Texas Instruments), Toshi Kikkawa (Transphorm), Jose Jimenez (Qorvo)

### System Reliability

WS.4 – Design for Reliability for Internet of Things - Moderator: Shalabh Tandon, Edmund Lee, Intel

### Advanced CPI

WS.5 – 2.5/3D Packaging - Moderator: Chandrasekara Kothandaraman, IBM

### Memory

WS.6 – Memory Reliability for Automotive Application - Moderator: Ben Schmid, NXP

WS.7 – MOL Reliability - Moderator: Richard Southwick, Ernest Wu, IBM

## Year In Review

Yuan Chen, Chair

Dielectric Breakdown – FEOL and BEOL - Jim Stathis, IBM

Metallization Reliability - Jeff Gambino, ON Semiconductor

Transistor Technologies - Tanya Nigam, Globalfoundries

## Poster Session

See Appendix – Full Program for Poster Sessions

## Abstract Highlights

- 2A.2 Hot Carrier Reliability Characterization in Consideration of Self-Heating in FinFET Technology, M. Jin, C. Liu, S. Pae, Samsung
- 3A.4 A New Aspect of Time-dependent Clustering Model for Non-uniform Dielectric TDDB, T. Shimizu, Renesas Electronics Corporation
- 3B.4 Investigation of Logic Circuit Soft Error Rate (SER) in 14nm FinFET Technology, T. Uemura, S. Lee, S. Pae, J. Park, Samsung Electronics
- 3B.5 Bidirectional NPN ESD Protection in Silicon Photonics Technology, R. Boschke, S.-H. Chen*, M. Scholz*, G. Hellings*, P. Verheyen*, J. Van Campenhout**, D. Linten*, G. Groeseneken, KU Leuven, *IMEC, **Ghent University-IMEC
- 3B.6 Systematic Transient Characterization of Graphene Interconnects for on-Chip ESD Protection, Qi Chen*, Rui Ma, Fei Lu, Chenkun Wang, Ming Liu and Albert Wang, University of California, Riverside
- 4A.1 Negative-Bias Temperature Instability of GaN MOSFETs, Alex Guo and Jesús A. del Alamo, Massachusetts Institute of Technology
- 4C.1 Timing Characterizations of Device and CPU-like Circuit to Ensure Process Reliability, M.-H. Hsieh, TSMC
- 5A.1 Reliability of Single-LayerMoS2 Field-Effect Transistors with SiO2 and hBN Gate Insulators, Yu.Yu. Illarionov*,+, M. Waltl*, M.M. Furchi*, T. Mueller* and T. Grasser* *TU Wien, Austria +Ioffe Physical-Technical Institute, Russia
- 5B.2 Multi-Segment Electromigration Failure Mechanism in Cu/Low-k Dual Damascene Interconnects, M.-H. Lin, A. Oates, TSMC

- 5C.1 Muon-Induced Soft Errors in 16-nm NAND Flash Memories, M.Bagatin, S. Gerardin, A. Paccagnella, A. Visconti, S. Beltrami, M> Bertuccio, K. Ishida, C. Frost, A. Hillier, V. Ferlet-Cavrois, University of Padova, Micron TEchnology, RIKEN Nishina Center, Rutherford Appleton Laboratory, ESA ESTEC, TEC-QEC
- 7A.1 The Physical Mechanism Investigation between HK/IL Gate Stack Breakdown and Time-dependent Oxygen Vacancy Trap Generation in FinFET Devices, C. H. Yang, S. C. Chen, Y. S. Tsai, R. Lu, Y.-H. Lee,TQRD, TSMC

## Exhibits & Exhibit Events

Exhibits are an integral part of the International Reliability Physics Symposium. Don't miss this opportunity to showcase your company's products and services.

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# Appendix - Abstracts, Bios & Technical Program

# TUESDAY MORNING

## April 19, 2016

General Session
Section D/E
8:00 a.m.

Welcome Remarks
Chris Henderson, Semitracks

8:10 a.m.
Introduction to Technical Program

8:30 a.m.
Keynote 1

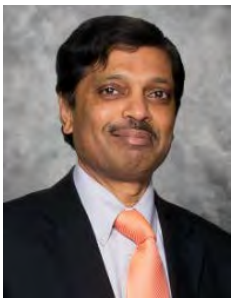
"Implications for System Reliability in Future Industrial and Automotive Designs", *Scott Roller, Vice President Systems Engineering and Marketing, Texas Instruments*

There have been significant advances in the Industrial, Automotive and Power Management market segments over the last 5 years and this presentation addresses key developments in these three related areas and its implications to reliability.

The promise of Industry 4.0 and Industrial IOT has finally arrived with innovative sensors, analog and embedded semiconductor based system designs that help companies deliver smarter and safer networked systems. Real-time communication in manufacturing and customization of produced goods will increase productivity and efficiency in many industrial and automotive markets. This presentation will cover the key tenets of Industry 4.0 and its implications for systems reliability.

Automotive electronic content has steadily grown and have found their way into heavy duty applications like turbo-charging and electronic steering. This talk will cover some of these automotive trends including the 48V power distribution and the new standards required for semiconductor components. Finally, novel wide-band gap power devices to support emerging power management markets will be discussed along with their reliability challenges.

9:15 a.m.
Keynote 2



"Driverless Vehicles? The Journey Ahead", Raj Rajkumar, George Westinghouse Professor, Carnegie Mellon University

Self-driving vehicles seem to have become quite the rage in popular culture over just the past few years, triggered in good part by the DARPA Grand Challenges. Self-driving vehicles indeed hold the potential to revolutionize modern transportation. This talk will provide some insights on many basic questions that, need to be addressed for the revolution to take place in practice. What are the technological barriers that currently prevent vehicles to be driverless? What can or cannot be sensed or recognized? Can vehicles recognize and comprehend as good as, if not better than, humans? Does connectivity play a role? Will the technology be affordable only for the few? How do issues like liability, insurance, regulations and societal acceptance impact adoption? The talk will be based on road experiences and will add some speculation.

10:00 a.m.
Awards

10:15 a.m.
Break

## *Session 2A - Transistor Reliability*

Session Co-Chairs: *Jason Campbell, NIST, Barry Linder, IBM*
*Section D*

*10:45 a.m.* - Session Introduction

*10:50 a.m.*
**2A.1 The "Permanent" Component of NBTI Revisited: Saturation, Degradation-Reversal, and Annealing**
*T. Grasser, M. Waltl, G. Rzepa, W. Goes, Y. Wimmer, A.-M El-Sayeed*, A. L. Shluger*, H. Reisinger**, B. Kaczer***, TU Wien, *University College London, **Infineon, ***imec*

While the defects constituting the recoverable component R of NBTI have been very well analyzed recently, the slower defects forming the more "permanent" component P are much less understood. Using a pragmatic definition for P, we study the evolution of P at elevated temperatures to accelerate these very slow processes. We demonstrate for the first time that P not only clearly saturates, with the saturation value depending on the gate bias, but also that the degradation at constant gate bias can also slowly reverse. Furthermore, at temperatures higher than about 300C, a significant amount of additional defects is created. Our new data are consistent with a recently suggested hydrogen release model which will be studied in detail using newly acquired long-term data.

*11:15 a.m.*

**2A.2 Hot Carrier Reliability Characterization in Consideration of Self-Heating in FinFET Technology**

*M. Jin, C. Liu, J. Kim, S. Choo, Y. Kim, H. Shim, L. Zhang, K. Nam, J. Park, S. Pae, . Lee, Samsung Electronics*

The severity of hot carrier injection (HCI) in PFET becomes worse than NFET under higher temperatures. This new observation is further found to be due to the coupled self-heating effects (SHE) during DC HCI stress (also the larger Ea in PFET HCI), rather than the negative bias temperature effect (NBTI) mixed components. Furthermore, in order to guarantee the precise estimation of HCI under circuit level AC condition, a new empirical HCI lifetime model with decoupling the SHE is proposed, which is further verified by the Si data from nanosecond pulsed waveform HCI stress and Ring Oscillator level stress.

*11:40 a.m.*

**2A.3 Characterization of Self-heating Leads to Universal Scaling of HCI Degradation of Multi-Fin SOI FinFETs**

*H. Jiang, S. Shin, X. Liu*, Xing Zhang*, A. Alam, Purdue University, *Peking University*

SOI FinFETs and other Gate-all-around (GAA) transistors topologies have excellent 3-D electrostatic control and therefore, have been suggested as potential technology options for sub-14 nm technology nodes. Unfortunately, the narrow gate geometry and reduced gate pitch suppress heat dissipation and increase thermal cross-talk, leading to severe self-heating of these transistors. Self-heating degrades performance and makes the classical reliability theories based on $T_L \sim T_{sub}$ irrelevant. In this paper, first, we propose a physicsbased thermal circuit compact model for multi-fin SOI FinFETs to characterize self-heating and validate the results by AC conductance method. Next, we analyze HCI radation varying with the number of fin ($N_{FIN}$), chuck temperature ($T_{sub}$) and AC frequency ($f$). The results show that HCI degradation dependent variables ($N_{FIN}$, $T_{sub}$, $f$) can be correlated to the lattice temperature ($T_L = g(N_{FIN}, T_{sub}, f)$ ) and obey the universal degradation curve ( $\Delta V_{th}(T_L) = f(S(T_L) \times t)$ ). Si-O bond-dispersion model explains the universal curve; therefore, the model can be used for a long term reliability projection with arbitrary combination $N_{FIN}$, $T_{sub}$, $f$, etc.

## *Session 2B - System Reliability*

Session Co-Chairs: *Kingsuk Maitra, Microsoft, Werner Kanert, Infineon*
Section E

*10:45 a.m.* - Session Introduction

*10:50 a.m.*

**2B.1 Software-based Dynamic Reliability Management for GPU Applications**

*S. Li, V. Sridharan*, S. Gurumurthi*, S. Yalamanchili, Georgia Institute of Technology, *Advanced Micro Devices, Inc*

In this paper we advocate a framework for dynamic reliability management (DRM) for GPU applications based on the idea of plug-n-play software-based reliability enhancement (SRE). The approach entails first assessing the vulnerability of GPU kernels to soft errors in program visible structures. This assessment is performed on a low level intermediate program representation rather than the application source. Second, this assessment guides selective injection of code implementing SRE techniques to protect the most vulnerable data. Code injection occurs transparently at runtime using a just-in-time (JIT) compiler. Thus, reliability enhancement is selective, transparent, on-demand, and customizable. We argue this flexible, automated software based DRM framework can provide an important, cost-effective approach to scaling reliability of large systems. We present the results of a proof of concept implementation on NVIDIA GPUs demonstrating the ability to traverse a range of performance reliability tradeoffs.

*11:15 a.m.*

**2B.2 Time Ordered Events CPU Reliability Assessment**

*I. Sauciuc, R. Kwasnick, R. Akhter, M. Ojha, M. Tse, D. Mani, C. Beas, G. Kaur, Intel Corporation*

IC product use conditions (UCs) are needed to enable accurate reliability modeling in the context of knowledge-based qualification. We describe a method of use condition development which is based on the sequence of user foreground events from field surveys. Events are converted to temperature and voltage use condition traces accounting for lab data on representative workloads and thermal modeling. The temperature and voltage data are paired for client CPU UC data and used to estimate the reliability risks for both silicon and thermo-mechanical failure mechanisms. The new approach are validated using field consumer data. We also describe the future work needed on how to account for concurrent vents and the implications on TOE methodology.

*11:40 a.m.*

**2B.3 Power-Supply Imapct on the Reliability of mid-1X TLC NAND Flash Memories**

*C. Zambelli, P. King, P. Olivo, L. Crippa*, R. Micheloni*, Università degli Studi di Ferrara, *Microsemi Corporation*

NAND Flash memories are complex systems that include many heterogeneous blocks that must work together to ensure a high reliability of the information storage. Many efforts in the reliability community are devoted to investigate the reliability-loss of this storage medium from a cell device physics point of view, whereas little importance is given to the other blocks that constitute such a system. In this work we present a reliability threat related to NAND Flash memories that is present on the high voltage circuitry of the memory: the dependence on the power supply. Through the experimental characterization of TLC mid-1X samples and thanks to the SPICE simulations of the high voltage blocks we have investigated the possible sources of this new reliability issue.

# TUESDAY AFTERNOON

# April 19, 2016

## *Session 3A - Dielectric Reliability (Front-end and Back-end)*

Session Co-Chairs: *Shou-Chung Lee, TSMC, Shinji Yokogawa, Polytechnic University of Japan*
Section D

*1:55 p.m.* - Session Introduction

*2:00 p.m.*

**3A.1 Fundamental Statistical Properties of Reconstruction Methodology for TDDB with variability (BEOL/MOL/FEOL) Applications**

*E. Wu, J. Stathis, B. Li*, A. Kim*, B. Linder*, R. Bolam*, G. Bonilla, IBM Research, *IBM System Division*

Recently, a sampling-based technique has received a great deal of attention as a methodology for the reconstruction of the Weibull distribution [1-3] to solve variability issues [4-7] related to breakdown (BD) statistics. While this method has been successful in SiO2 with small thickness (TOX) variation [1,3], its applicability remains questionable [3] for MOL/BEOL dielectrics with substantial spacing variation and intrinsic line-edge roughness (LER) [4-6]. A sampling-number dependence of Weibull slope is recently reported but its root-cause is not understood yet [3]. Thus, a large sampling number (n) is required to obtain an accurate beta value. Moreover, it has been shown that the reconstructed distribution with a small n can be misleading as it masks the non-Weibull/non-Poisson area-scaling nature of underlying in-die TBD distributions [3]. This suggests a lack of fundamental understanding of this methodology can lead to its incorrect usage. In this work, we show statistical scaling property of the Beta-sampling curve, along with new results of sampling-number dependence of the T63 variation. For the first time, we report a fundamental mathematical formulation for these two sampling-number dependencies of beta and Simga_T63. Finally, we propose a quantitative criterion for the applicability of reconstruction method for its correct usage.

*2:25 p.m.*

**3A.2 New Breakdown Mechanism Investigation: Barrier Metal Penetration Induced Soft Breakdown in Low-k Dielectrics**

*C. Wu, Y. Li, J. Bömmels, I. De Wolf, Z. Tőkei, K.Croes, imec*

A Soft Breakdown (SBD) phenomenon happening in porous low-k dielectrics during time dependent dielectric breakdown measurements was investigated. The early formation of local conductive paths was identified by monitoring leakage currents and capacitance data in the SBD phase. The nature of this conductive path was demonstrated to be related to intrinsic dielectric degradation. By comparing samples with different process conditions, we found that barrier metal penetration is an important root cause of SBD initiation. Our study of the voltage and temperature acceleration of the SBD phenomenon shows that these acceleration factors, $m$=22 and $Ea$=0.2eV, are at a reasonable level. However, further investigations on large size devices illustrate that the difference in barrier metal penetration depth between different samples could lead to a large decrease of Weibull slopes and degrade the overall reliability performance. Therefore, innovations of metal barrier deposition on porous low-k dielectrics to avoid barrier metal penetration are required for advanced technology nodes.

*2:50 p.m.*

**3A.3 On Why Dielectric Breakdown Strength Reduces With Dielectric Thickness,** *J. McPherson, McPherson Reliability Consulting LLC*

A fundamental-physics reason is presented for why the dielectric breakdown strength Ebd reduces with increases in dielectric thickness tdiel. Through the extensive use of planar dipolar summations, it is shown that the Lorentz factor L tends to increase with dielectric thickness. The increase in L with dielectric thickness produces a higher local electric field (Eloc) in thicker dielectrics. This higher Eloc produces more polar-bond distortion (stretching, compressing, bending, etc.) and this leads to a reduction in bond strength. A reduction in bond strength causes Ebd and TDDB reductions regard-less of the actual bond breakage mechanism (standard Boltzmann processes, current driven processes, or hydrogen release processes). This work shows that, while thicker SiO2 has lower Ebd, all SiO2 thicknesses tend to breakdown at roughly the same local electric field (Eloc)bd ≈ 40MV/cm.

*3:15 p.m.*

**3A.4 A New Aspect of Time-dependent Clustering Model for Non-uniform Dielectric TDDB**

*T. Shimizu, N. Suzumura, K. Ohgata, H. Tsuchiya, H. Aono, M. Ogasawara, Renesas Electronics Corporation*

In this study, we developed the theory of the time-dependent clustering (TDC) model for time-dependent dielectric breakdown (TDDB) of non-uniform dielectrics and shed light on a new aspect. We found that TDC model can be derived from the Weibull model with scale parameter variation and that the corresponding electric field distribution is a kind of extreme value distributions. Using Metal-Insulator-Metal (MIM) capacitor TDDB data, we demonstrated the distributions of electric filed and space variations can be obtained from lifetime data by our approach.

*Break*
*3:40 p.m.*

*4:10 p.m.*

**3A.5 Time-Dependent Series Resistance and Implications for Voltage Acceleration Models in BEOL TDDB**

*A. Kim, B. Li, P. McLaughlin, C. J. Christiansen*, E. Wu**, IBM Research, *GlobalFoundries*

A continuous down-scaling of BEOL pitch for advanced process technologies has drastically increased the resistance of Cu interconnects. A concern of the voltage drop of TDDB stress voltage along resistive metal electrodes due to a series resistance effect or IR drop has been reported [1,2]. Such an IR drop is believed to cause non-Poisson area scaling [1], lower-than-expected voltage acceleration parameter values and erroneous choice of models for TDDB

lifetime projections [2]. For accurate TDDB lifetime projections at operating voltages, it is of a critical importance to understand the series resistance effect in BEOL devices under high voltage stresses to accurately estimate the voltage acceleration parameter of a chosen TDDB model. Our results show that IV characteristics of BEOL ILD changes drastically over time due to charge trapping and defect creation under voltage stresses, rather than assumed to be constant as reported in [1,2]. In contrast to previous work, we present four independent experiments and fully transient simulation results to show that IR drop due to series resistance has a negligible effect on voltage acceleration models. Finally, our long-term TDDB results along with a long-term TDDB results (> 2 years) of 64-pitch interconnect made of Cu/ULK (k=2.55, SiCOH) with IR drop corrections on high stress voltages show that the power law model best describes the voltage acceleration behavior of the ULK dielectric material used for our studies.
*4:35 p.m.*

**3A.6 A New Model for Dielectric Breakdown Mechanism of Silicon Nitride Metal-Insulator-Metal Structures**
*K. Okada, Y. Ito, S. Suzuki, TowerJazz Panasonic Semiconductor*

For the further advance of Si RF devices and also GaAs/GaN MMIC devices, highly reliable silicon nitride MIM structure has to be realized on the basis of deeper understandings of its degradation/breakdown mechanisms. Through the study on TDDB reliability of MIM structures with silicon nitride films having various thicknesses by three deposition processes, it has been revealed that QBD (charge to breakdown) strongly depends on the stress condition and film deposition process and that the electric field shift until breakdown is constant independent of deposition process, stress condition, thickness, and temperature. Furthermore, the field shift at the anode is the key for breakdown. Based on these results, a new TDDB model for silicon nitride MIM structure has been proposed.

## *Session 3B- Joint Soft Errors/ESD and Latch-up*

Soft Errors Session Chairs: *Balaji Narasimham, Broadcom, Ethan Cannon, Boeing*
ESD and Latch-up Session Chairs: *Teruo Suzuki, Socionext, Dimitri Linten, imec*
Section E

*1:55 p.m.* - Session Introduction
*2:00 p.m.*
**3B.1 Extreme Scale and Bleeding Edge Technology Lead to a Need for Resilient High Performance Computing Systems (Invited)**
*N. DeBardelebren, Los Alamos National Laboratory*

High Performance Computing (HPC) and supercomputing are an important sector of the computing field. Distinguishing itself from cloud computing, HPC systems are sized to run extremely large and important calculations such as tightly coupled numerical simulations. These often run for days to weeks on supercomputers and are used to inform scientific discovery and national security. It comes as no surprise then that reliable HPC systems are integral to producing believable scientific results. In this paper we build on years of experience studying supercomputers around the U.S. Department of Energy (DOE) and bring together insights about challenges and needs for HPC reliability. First, we discuss the state of the practice in HPC reliability. We look at a sampling of results from previous work and how reliability telemetry data is used by vendors, system architects, and end users. Finally, we discuss some changes coming in the next decade for HPC systems and how the technology we depend on will drive new reliability challenges that must be addressed and monitored.

*2:25 p.m.*

**3B.2 SE Performance of a Schmitt-Trigger-Based-D-Flip-Flop Design in a 16-nm Bulk FinFET CMOS Process** *H. Jiang, H. Zhang, D. R. Ball, L. Massengill, B. Bhuva, T. Assis*, B. Narasimham**, Vanderbilt University, *Robust Chip, Inc., **Broadcom Corporation*

A har+I130:AJ143dened Flip-Flop (FF) design using Schmitt trigger circuits for improved soft error (SE) performance is presented. The Schmitt-trigger DFF (STDFF) design along with conventional DFF in a 16-nm bulk FinFET CMOS process were tested using alpha particles and heavy-ions. The STDFF design shows 162× improvement in the alpha SER and upto 30× improvement in heavy-ion cross-section compared with conventional DFF at nominal supply voltage.

*2:50 p.m.*

**3B.3 Hardware Based Empirical Model for Predicting Logic Soft Error Cross-section**

*S. Jagannathan, N. Mahatme, N. J. Gaspard*, B. Bhuva*, L. Massengill*, Thomas Loveless**, Freescale Semiconductor, *Vanderbilt University, **University of Tennessee*

This work presents a technique to estimate logic cross-section using measured single-event transient pulse widths from radiation experiments. The results are verified by comparing against direct measurement of logic cross-section using C-CREST circuit. Since the logic cross-section is extracted based on experimentally measured transients, it includes device level effects and could be used by existing software-based methods to accurately predict logic soft error rate.

*3:15 p.m.*

**3B.4 Investigation of Logic Circuit Soft Error Rate (SER) in 14nm FinFET Technology**

*T. Uemura, S. Lee, S. Pae, J. Park, H. Lee, Samsung Electronics*

This paper presents characterization results of soft error rate (SER) on logic circuits manufactured with 14 nm High-k/metal gate bulk FinFET technology. The FinFET SER advantage seen on SRAM was also validated on logic circuits (5-10X improvement). Adding NMOS on low critical charge can increase error rate, yet it can be easily mitigated by the design change. Design schemes for low-power has little impact to the SER. Single event transient on clock-line in 14 nm FinFET was substantially improved from planer-MOS.

*Break*
*3:40 p.m.*

*4:10p.m.*

**3B.5 Bidirectional NPN ESD Protection in Silicon Photonics Technology**

*R. Boschke, S.-H. Chen*, M. Scholz*, G. Hellings*, P. De Heyn*, P. Verheyen*, J. Van Campenhout*, D. Linten*, A. Thean*, G. Groeseneken, KU Leuven, *IMEC*

Silicon photonics technologies are used for low power, high bandwidth signal transfer between CMOS chips. Silicon waveguides transfer the optical signal while Silicon modulators (Si MOD) and Germanium photodetectors (Ge PD) convert the electrical into an optical signal and vice versa. Ge PDs and Si MOD need ESD protection to survive S20.20 controlled assembly. A NPN transistors, that was integrated into the technology, can provide an effective and transparent ESD protection. TLP IV of the NPN show a snapback and an S-bent that is explained and verified with TCAD.

*4:35 p.m.*
**3B.6 Systematic Transient Characterization of Graphene Interconnects for on-Chip ESD Protection**
*Q. Chen, R. Ma, F. Lu, C. Wang, M. Liu, A. Wang, W. Zhang*, M. Xia*, Y.-H. Xie*, Y. Cheng**, University of California, Riverside, *University of California, Los Angeles, **Peking University*

We report comprehensive transient characterization of graphene ribbons (GR) for ESD protection circuits by TLP testing with varying ESD pulse rise time and duration across -10ºC to 110ºC. Practical GR dimensions and large number statistics provide practical design guidelines for on-chip ESD circuits using robust GR interconnects.

## *Session 3C – Photovoltaics Reliability/ESREF Best Paper*

Photovoltaics Reliability Session Chairs: *Andrea Cester, University of Padova , Michael Daenen, University of Hasselt*
Section F/G

*1:55 p.m.* - Session Introduction

*2:00 p.m.*
**3C.1 Predictive Simulation of Defect Migration and Metastabilities in CdTe Solar Cells**
*D. Guo, R. Akis, D. Brinkman, D. Vasileska, A. Moore*, Arizona State University, *Colorado State University*

Performance of CdTe solar cell, similarly to performance of any other semiconductor device is uniquely defined by device geometry and properties of semiconductor regions such as band parameters, distribution and parameters of doping and trapping/recombination centers. However, when the above variables cannot be measured precisely, predictive simulation of device performance becomes rather challenging, and CdTe PV devices exemplify such situation. Moreover, predictive simulation of CdTe devices becomes even more challenging due to low temperature diffusion and reaction of Cu-related centers, phenomena that is known to strongly affect the device causing both short-term metastabilities and permanent changes in device performance. In this work, we present a self-consistent diffusion-reaction simulation scheme that was developed to overcome these challenges by accurate simulation of electrically active centers in the device structure, and the evolution of these centers under stress conditions to support our hypotheses that explains rapid changes in atomic concentration of Cu in CdTe as function of stress conditions.

*2:25 p.m.*
**3C.2 Effects of Current Stress and Thermal Storage on polymeric heterojunction P3HT:PCBM Solar Cell**
*A. Rizzo, A. Cester, L. Torto, M. Barbato, N. Wrachien, N. Lago, M. Corazza*, F. Krebs*, S. Gevorgyan*, University of Padua,*University of Denmark*

Polymeric solar cells have attracted the attention of many research groups as a low-cost and eco-sustainable alternative to conventional solar cells [1-2]. In this work, we investigated the effects of accelerated electrical stress in forward bias condition and thermal storage. We employed the Impedance Spectroscopy technique to obtain a more comprehensive picture of the cell degradation phenomena.

*2:50 p.m.*

**3C.3 Improvement of Solar Cell Performance and Reversibility of Ageing Effects in Hydrogenated Amorphous Silicon Solar Cells under Illumination and Electric Field Stress: Role of TCO and Substrate**

*A. Scuto, M. Foti*, C. Gerardi**, A. Battaglia***, S. Lombardo, IMM CNR, *STMicroelectronics, **Enel Green Power, ***3SUN*

In this work we discuss about the hydrogenated amorphous silicon (a-Si:H) photovoltaic improvement performance caused by the application of an external electric fields to the cells under illumination. The effects, clearly visible on the series resistance, on the open circuit voltage, and on the overall power conversion efficiency have been investigated discussing the key impact of tempera-ture, electric field intensity and illumination level. Showing the evident reversibility effects visible in complete solar cells, but also in individual doped a-Si:H thin films, we demonstrate that such phenomenon is due principally to the motion of some ions/molecular species from the oxide to the a-Si:H films (or vice-versa) driven mainly by the electric field. Finally, to further investigate on the possible species that migrates causing a reduction of recombination current, we discuss some exper-iments based on different substrates analysis, various types of TCO and double-junction/micromorph solar cells comparison.

*3:15 p.m.*

**3C.4 Reconfigurable Power Management for Monolightic CMOS-on-Photovoltaic under Partial and Complete Shading,** *R. Mahto, P. Zarkesh-Ha, O. Lavrova*, University of New Mexico, *Sandia National Laboratory*

The Photovoltaic (PV) cells of a module can be made to operate in various load and lighting condition by using switches to connect in series or parallel for various load requirements in the field, such as high voltage and low current versus high current and low voltage. Compared to having external switches monolithic CMOS-on-PV cells improves the module efficiency by providing better reliability and lifetime. In this paper, a partial and complete shading detection algorithm is presented. Also, a model for calculating the output current and voltage equation for the monolithic CMOS-on-PV cell is presented.

*Break*
*3:40 p.m.*

*4:10 p.m.*

**3C.5 System-level Process-voltage-temperature Variation-aware Reliability Simulator using a Unified Novel Gate-delay Model for BTI, HCI and GOBD (ESREF Best Paper)**

*T. Liu, C.-C. Chen, S. Cha, L. Milor, Georgia Institute of Technology*

# TUESDAY EVENING

# April 19, 2016

**Workshops**
Tuesday, April 20, 6:30 p.m – 9:30 p.m.

WS.1
***Transistor/Circuit: Advanced CMOS Nodes (FDSOI, FinFET) usage for High Reliability Markets from Device and Design Perspective,*** Puneet Gupta, UCLA

WS.2
***BEOL: Challenges for EM and SM / Test Time / Power Management,*** Ki-Don and Gavin Hall, OnSemi

WS.3
***Compound: GaN Reliability – What is Missing? What Should be Looked at Beyond What's Already Known?,*** Jungwoo Joh, Texas Instruments, Toshi Kikkawa, Transphorm, and Jose Jimenez, Qorvo

WS.4
***System Reliability: Design for Reliability for Internet of Things,*** Shalabh Tandon, Edmund Lee, Intel

WS.5
***Advanced CPI: 2.5/3D Packaging,*** Chandrasekara Kothandaraman, IBM

WS.6
***Memory: Memory Reliability for Automotive Application,*** Ben Schmid, NXP

WS.7
***MOL Reliability,*** Richard Southwick, Ernest Wu, IBM

# WEDNESDAY MORNING

# April 20, 2016

## *Session 4A - Compound/Opto Electronics*

Session Co-Chairs: *Jungwoo Joh, Texas Instruments, Toshi Kikkawa, Transphorm*
Section D

*8:30 a.m.* - Session Introduction

*8:35 a.m.*
**4A.1 Negative-Bias Temperature Instability of GaN MOSFETs**
*A. Guo, J. del Alamo, MIT*

GaN high-electron-mobility transistors with insulated-gate (MIS-HEMTs) are attractive alternatives to Si for power electronics. Compared to the traditional HEMT structure with Schottky gate, GaN MIS-HEMTs offer low gate leakage current, higher breakdown voltage, and possible enhancement-mode operation, all desirable attributes for power electronics. However, reliability issues surrounding GaN-HEMTs, especially the threshold voltage instability under high voltage stress, represent a major roadblock for technology commercialization. The origin of this problem in GaN MIS-HEMTs is not well understood because the gate stack has many layers and interfaces that present many opportunities for trapping and complex dynamics. We isolate the contribution of the gate dielectric and its interfaces by studying a simple GaN MOSFET structure. This device approach, in its own right, is also a strong candidate for power electronic applications. We identified three degradation mechanisms that are responsible for NBTI in oxide/GaN MOSFETs. Under benign stress, recoverable electron detrapping from pre-existing oxide traps close to the oxide/GaN interface takes place shifting VT negative. Under moderate stress, an additional transient positive VT shift is caused by electron trapping into defects in the buffer layer. Under harsh stress conditions there is also a permanent negative VT shift and permanent degradation in gm and S that is the result of interface state generation. These studies should be instrumental in understanding the more complex instability issues of GaN MIS-HEMTs. The full-length paper will present the model and experimental procedures in more detail.

*9:00 a.m.*
**4A.2 Positive Bias Temperature Instability Evaluation in Fully Recessed Gate GaN MIS-FETs**
*T.-L. Wu, J. Franco, D. Marcon, B. De Jaeger, B. Bakeroot, X. Kang, S. Stoffels, M. Van Hove, G. Groeseneken, S. Decoutere, imec*

GaN-based devices are promising candidates for power switching applications. D-mode AlGaN/GaN MIS-HEMTs or e-mode recessed gate GaN MIS-FETs attract a lot of attentions recently. However, the reliability remains a big challenge on such architectures due to an non-native gate dielectric on top of the AlGaN barrier or GaN channel, leading to VTH hysteresis after a forward-reverse gate bias sweep or VTH shift during a positive gate bias stress, which is generally called positive bias temperature instability (PBTI). In this paper, we study PBTI in fully recessed gate GaN MIS-FETs. Unlike similar PBTI studies in GaN literature, we use the eMSM (extended-Measurement-Stress-Measurement) technique to perform a set of stress/recovery tests to evaluate the PBTI phenomena with collecting the maximum information during the stress and relaxation period. Furthermore, we propose a physical model to explain the results.

*Break*
*9:50 a.m.*

*9:55 a.m.*
**4A.3 Product Reliability of GaN Devices (Invited)**
*S. Bahl, D. Ruiz, D. S. Lee, Texas Instruments*

To enable the widespread adoption of GaN products, the industry needs to be convinced of product-level reliability. The difficulty with product-level reliability lies with the diverse range of products and use conditions, a limited ability for system-level acceleration, and the complication from non-GaN system failures. For power management applications, however, it is possible to identify fundamental switching transitions. This allows the device to be qualified in an application-relevant manner. In this paper, we explain how hard-switching can form a fundamental switching transition for power management products. We further show that the familiar double-pulse tester is a good hard-switching qualification test vehicle. The methodology is explained in the context of the existing qualification framework for silicon transistors.

*10:20 a.m.*
**4A.4 Impact of Buffer Charge on the Reliability of Carbon Doped AlGaN/GaN-on-Si HEMTs**
*I. Chatterjee, M. Uren, S. Karboyan, S. M. Horcajo, A. Pooth, K. B. Lee*, Z. Zaidi*, P. Houston*, D. Wallis**, I. Guiney**, C. Humphreys**, M. Kuball, University of Bristol, *The University of Sheffield, **University of Cambridge*

Charge trapping and transport in the carbon doped GaN buffer of an AlGaN/GaN-on-Si HEMT has been investigated. Back-gating and dynamic RON experiments show how the onset of leakage in the strain relief layer at a lower field than that through the upper part of the structure can result in serious long-term trapping leading to current collapse under standard device operating conditions. Controlling current-collapse requires control of not only the layer structures and its doping, but also the precise balance of leakage in each layer.

*10:45 a.m.*
**4A.5 Understanding the Degradation Sources Under ON-state Stress in AlGaN/GaN-on-Si SBD: Investigation of the Anode-Cathode Spacing Length Dependence**
*A. N. Tallarico, P. Magnone*, S. Stoffels**, S. Lenci**, D. Marcon**, E. Sangiorgi, S. Decoutere**, C. Fiegna**, University of Bologna, *University of Padova, **imec*

In this paper, we report an analysis of the degradation induced by ON-state stress in Au-free AlGaN/GaNon- Si Schottky barrier diodes (SBDs). When the device operates in ON-state mode, the combined effect of large currents and moderate electric fields may cause a shift of the turn-on voltage (VTON) and ON-resistance (RON) because of the charge carrier trapping/de-trapping, occurring in different regions and related to different types of defects. In particular, the influence of the anode-cathode spacing length on the ON-state degradation has been investigated and the degradation sources, attributable to ΔVTON and ΔRON, have been understood. Moreover, thanks to this approach, a critical electric field for the RON degradation has been reported.

*11:10 a.m.*
**4A.6 Progressive Breakdown in High-Voltage GaN MIS-HEMTs**
*S. Warnock, J. del Alamo, Massachusetts Institute of Technology*

As the demand for more energy efficient electronics increases, GaN Field-Effect Transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN power transistors are ready for commercial deployment. Our work focuses on gate dielectric reliability and in particular, in contributing fundamental understanding behind the physics of time-dependent dielectric breakdown (TDDB) of the gate dielectric in GaN MIS-HEMTs. In this work we investigate progressive breakdown (PBD). We have found classic features resembling those observed in silicon devices. That is, we see evidence to support the percolation model of defects, both in the breakdown

statistics but also in the distribution of breakdown location throughout the dielectric. We also see an increase in gate leakage in current-voltage characterization after PBD has occurred, with voltage and temperature dependences that are consistent with observed behavior in silicon. This classic TDDB behavior gives hope that a lifetime model for TDDB in GaN MIS-HEMTs can be developed.

## *Session 4B -Process Integration*

Session Co-Chairs: *Bill McMahon, Intel, Siddarth Krishnan, Applied Materials*
Section E

*8:30 a.m.* - Session Introduction

*8:35 a.m.*
**4B.1 Process Optimizations for NBTI/PBTI for Future Replacement Metal Gate Technologies**
*B. Linder, A. Dasgupta, T. Ando, E. Cartier, U. Kwon, R. Southwick, M. Wang, S. Krishnan, M. Hopstaken, M. Bajaj, R. Pandey, W. Chang, T. Yamashita, O. Gluschenkov, V Narayanan, J. Stathis, S. Ray*, J. Liu*, IBM, *Global Foundries*

Bias Temperature Instability (BTI) continues to be a major reliability concern and is the limiting mechanism for inversion thickness (Tinv) scaling for future technologies. Replacement Metal Gate (RMG) technologies present unique challenges for improving NBTI and PBTI as compared to traditional Gate First technologies, where the gate stack is exposed to the high temperature source/drain (s/d) anneal. We have identified four methods for improving BTI in RMG technologies: structural optimization of the gate stack within RMG thermal constraints, layer thicknesses optimization, defect control by introducing dopants into the dielectric stack, and metal workfunction (WF) modulation that provides BTI-benefits which exceed predictions by a simple effective field consideration.

*9:00 a.m.*
**4B.2 NBTI in Replacement Metal Gate SiGe core FinFETs: Impact of Ge Concentration, Fin Width, Fin Rotation and Interface Passivation by High Pressure Anneals**
*J. Franco, B. Kaczer, A. Chasin, H. Mertens, L.-Å. Ragnarsson, R. Ritzenthaler, S. Mukhopadhyay, H. Arimura, P. Roussel, E. Bury, N. Horiguchi, D. Linten, G. Groeseneken, A. Thean, Imec*

We report a broad study of NBTI in RMG SiGe core FinFETs, focusing on the impact of Ge concentration (0%, 25% and 45%), fin width (1um-->20nm), fin side-wall orientation (<110> and <100>, obtained by 45° fin rotation), and interface passivation by high pressure anneals (HPA). We focus on Si-cap-free gate stacks which offer simplified FinFET integration. Direct oxidation of SiGe yields poor interface quality, which can be restored by HPA. Despite a wide distribution of defect levels in the interfacial layer due to Ge suboxide formation, SiGe reliability still benefits of a reduced bulk oxide trapping thanks to favorable energy decoupling of channel carriers to dielectric defect levels. Further NBTI improvement is observed thanks to oxide field reduction in fully depleted fins. Fin rotation does not improve NBTI in SiGe fins, while some improvement, particularly of the near-channel degradation, was obtained by HPA. Based on these results we conclude that Si-cap-free RMG SiGe gate stacks with properly optimized HPA can offer a simplified FinFET integration, with a limited NBTI reliability penalty compared to best-in-class Si-passivated SiGe devices.

*9:25 a.m.*

**4B.3 Study of Oxygen Vacancy in High-k Gate Dielectric by Charge Injection Technique**

*J. Liao, S.-H. Gao, K. Joshi, Y.-H. Lee, T.L. Lee, H.S. Wang, S.Y. Chien, J.-S. Wang, J.-R. Shih, K. Wu, Taiwan Semiconductor Manufacturing Company*

A new technique by charge injection is introduced to investigate the charging effect on weak oxide in the gate stack of high-k metal gate process. The oxide with extra oxygen vacancy are more vulnerable to process charging, as verified by the correlation of Vt vs. subthreshold swing degradation, SILC spectrum, and chemical bonding state analysis using X-ray photoelectron spectroscopy (XPS) and electron energy loss spectroscopy (EELS). Degradation of pFET threshold voltage (Vt) shift by gate injection under Source/Drain (S/D) floating condition is observed, this is attributed to the oxide damage by the accelerated hot carriers from S/D reverse bias. The convolution of "random dopant fluctuation (RDF) + charging effect" is expected to magnify devices Vt shift, especially for those worse bit cells with high Vt as verified by the Monte-Carlo simulation. We further demonstrate that process with tighten Vt distribution, such as FinFET technology with less implant process and better charge release immunity, is less vulnerable to the charging induced Vt shift.

*Break*
*9:50 a.m.*

*10:20 a.m.*

**4B.4 Hot-carrier Analysis on nMOS Si FinFETs with Solid Source Coped Junction**

*A. Chasin, J. Franco, R. Ritzenthaler, G. Hellings, M. Cho, Y. Sasaki, A. Subirats, P. Roussel, B. Kaczer, D. Linten, N. Horiguchi, G. Groeseneken, A. Thean, imec*

We report extensive experimental results of the Channel Hot Carrier (CHC) and Positive Bias Temperature Instability (PBTI) reliability of nMOS Si bulk-FinFETs with extension doping by PEALD Phosphorus doped Silicate Glass (PSG). Device performance improvements with PSG doping are achieved without substantial device reliability degradation even for short channel FinFETs. PSG results in less damage in the junctions and lower Gate Induced Drain Leakage (GIDL) current than standard Phosphorous Ion Implantation process (P I/I).

*10:45 a.m.*

**4B.5 Transistor Reliability Characterization and Comparisons for a 14 nm Tri-gate Technology Optimized for System-on-Chip and Foundry Platforms**

*C. Prasad, K. W. Park, P. Bai, H.-Y. Chang, M. Chahal, N. Dias, W. Hafez, C.-H. Jan, I. Meric, N. Nidhi, S. Novak, R. Olac-vaw, R. Ramaswamy, S. Ramey, C. Tsai, Intel Corporation*

The transistor reliability characterization of a 14nm SoC node optimized for low power operation is described. In-depth assessment of reliability vs. performance benefit for Core and I/O devices are performed on Logic and SoC nodes, and clear trends with scaling are identified. Insight is provided into hot carrier and off-state aging, and self-heat. The 14nm SoC node is shown to be robust for all transistor reliability modes. Process monitor data are used to demonstrate a stable line in high-volume manufacturing.

## *Session 4C - Design for Circuit Reliability*

Session Co-Chairs: *Kevin Cao, Arizona State University, Jim Tschanz, Intel*
Section F/G

*8:30 a.m.* - Session Introduction

*8:35 a.m.*
**4C.1 Timing Characterizations of Device and CPU-like Circuit to Ensure Process Reliability**
*M.-H. Hsieh, T.-Y. Yew, Y.-C. Huang, W. Wang, N. H. Tseng, W. S. Chou Lee, Y.-H. Lee, TSMC*

Existing methodology and stress conditions are ideal for process benchmarking but might not be sufficient under fierce competition between advanced technology development approaches. In this paper, the importance of timing delay characterization in both device and circuit level is demonstrated and emphasized. Due to the difficulties of having accurate aging model for product level simulation during early stage of process development, silicon to simulation (S2S) correlation should be established in circuit level. Experiments in this study cover from discrete device, ring oscillator (RO) and a circuit block from ARM CPU. Based on the extensive results, the characterization of timing margin is highly recommended. So, early warnings of circuit reliability risk can be obtained to save major detours during technology development.

*9:00 a.m.*
**4C.2 Budget-Based Reliability Management to Handle Impact of Thermal issues in 16nm Technology**
*J.-G. Ahn, J. Cooksey, N. Navale, N. Lo, P.-C. Yeh, J. Chang, Xilinx*

We handle the thermal impact on FEOL and BEOL reliability by using new aging simulation flow and EM checking flow which is considering thermal coupling effects. We demonstrated how the budget-based reliability check works with thermal issues and showed that it checks product risk more rigorously. It leads to huge benefit to circuit designers by allowing higher temperature increase both for FINFET SHE and metal wire JHE.

*9:25 a.m.*
**4C.3 Mission Profile Recorder: An Aging Monitor for Hard Events**
*S. Mhira, V. Huard, A. Jain, F. Cacho, D. Meyer, S. Naudet, A. Bravaix*, C. Parthasarathy, STMicroelectronics, *IM2NP-ISEN*

Overall, in this work, we have demonstrated the fundamental as-pects of Mission Profile Recording as an alternative to intrusive, aging monitoring systems to cope with oxide breakdown and elec-tromigration. We have designed, implemented and fully tested on several wafers a functional prototype to achieve a full proof-of-concept. The key element for accurate lifetimes is the accuracy of the Analog-to-Digital Conversion including the process variations and across the temperature and voltage product range. This study offers new perspectives towards product hardening and qualification with respect to an adaptive approach to real user-based workloads.

*Break*
*9:50 a.m.*

*10:20 a.m.*
**4C.4 Analog-circuit NBTI Degradation and Time-dependent NBTI Variability: An Efficient Physics-Based Compact Model**
*K.-U. Giering, G. Rott*, G. Rzepa*, H. Reisinger**, A. K. Puppala, T. Reich, W. Gustin**, T. Grasser*, R. Jancke, Fraunhofer IIS/EAS, *TU Wien, **Infineon*

We experimentally and theoretically investigate the NBTI degradation of pMOS devices due to analog stress voltages and thus go beyond existing NBTI studies for digital stress. As a result, we propose a physics-based compact model for analog-stress NBTI which builds upon the extensive TCAD analysis of our ultra-short-delay experimental data. The numerical efficiency of the compact model allows its direct coupling to electric circuit simulators and permits to accurately account for NBTI degradation already during circuit design. Our model enables the calculation of the time-dependent NBTI variability of single device parameters and of circuit performance parameters. We demonstrate the NBTI model on an operational amplifier and calculate the mean drift and variability of its offset voltage.

*10:45 a.m.*
**4C.5 New Methodology for On-Chip RF Reliability Assessment**
*L. Heiß, A. Lachmann*, R. Schwab*, G. Panagopoulos*, P. Baumgartner*, M. Y. Virupakshappaa, D. Schmitt-Landsiedel, Technical University of Munich, *Intel Deutschland GmbH*

On-chip self-stressing circuits are gaining increasing interest to study frequency dependency of transistor reliability. Thereby observation of frequency dependent degradation in experimental results can have two origins: (1) A physical root cause, i.e. the considered degradation mechanism is indeed frequency dependent. (2) Insufficient signal integrity, particularly at high frequencies. Former work mainly focused to explain experimental results in the sense of (1), but has neglected (2). This work presents a new approach which uses an advanced test structure to investigate the signal integrity of on-chip stress circuits. Experimental results from a 28nm HKMG technology show that this method considerably supports the interpretation of RF reliability data which can otherwise easily be misinterpreted.

*11:10 a.m.*
**4C.6 Reliability vs. Secuirty: Challenges and Opportunitues for Developing Reliable and Secure Integrated Circuits (Invited)**
*F. Rahman, D. Forte, M. Tehranipoor, University of Florida*

As technology further scales, devices offer better performance with faster speed and lower power albeit at the cost of reliability. Advanced technology nodes introduce higher variations in manufacturing processes, and devices experience greater aging and environmental degradation. Although such reliability issues should be suppressed for the sake of performance in both CMOS and post-CMOS devices, researchers have leveraged them for a variety of applications and unique primitives for hardware-oriented security. In this paper, we present a comprehensive study on device reliability and security, and make a qualitative assessment of different variability and degradation sources based on their impact on performance, reliability and security. We conclude that reliability and security both play vital roles for respective applications and must be treated in a holistic manner. Hence we urge the reliability and security communities to work together to develop new technologies for designing high performance, reliable and secure integrated circuits.

**Luncheon**
Wednesday, April 20, 12:20 p.m. – 2:15 p.m.

***The Future of Machine Brain Interfaces,*** Sanjay Natarajan, Vice President Technology and Manufacturing Group, Intel Corporation

For the past 40 years, the phenomenon known as Moore's Law has brought us some amazing technology today, such as self-driving cars, a supercomputer in every pocket, and access to the world's knowledge just a few keystrokes away. If, 25 years ago, someone told you all of these would be possible, many of you would have labeled them as crazy. And yet here we are.

Unfortunately Moore's Law is dying. We don't know yet whether it's with a whimper or a bang, but all signs point to dying nonetheless. Which begs the important question, *"when Moore's Law dies, what will we all do for living*"?

That is the topic of this lunchtime keynote speech. We will try to shine a light another 25 years out and talk about some emerging technologies which look as crazy today as self-driving cars did 25 years ago, but which could in fact be keys to the next technological revolution.

One of these emerging technologies is the field of man/machine interface. This field has been around for a while, but in many ways is still in its infancy. Forget about keyboards and mice as your interface to the computer. Forget about talking to Siri. In 25 years, the technology will exist so that you can simply ***think*** to your computer.

Another emerging technology is the field of 3D printing, particularly 3D *bioprinting*. In 25 years, the technology will exist to print usable tissues and organs, incorporating your individual DNA sequence and your own stem cells. Printed body parts will be part of our future.

These ideas seem crazy today, just as other ideas did 25 years ago. They raise a host of ethical issues, not to mention new reliability concerns. And there is a lot of work to be done to make these a reality. But many of the fundamental barriers to making these a reality have already been overcome.

**Biography**
Sanjay Natarajan spent over 22 years in Intel's Technology Development organization. Most recently, as a Vice President in Intel's Technology and Manufacturing Group, he led the development of Intel's 14nm process technology, today's leading state-of-the-art process worldwide. In July of 2015, Sanjay left Intel to pursue other interests. One of those interests is advising semiconductor companies around the world on how to navigate the choppy waters of the semiconductor business. Another interest -- as a Professor in the College of Engineering at Portland State University -- is in exploring emerging technology options for well past the Moore's Law Era.

# WEDNESDAY AFTERNOON

# April 20, 2016

## *Session 5A – Transistor Reliability*

Session Co-Chairs: *Jason Campbell, NIST, Barry Linder, IBM*
Section D

*1:55 p.m.* - Session Introduction

*2:00 p.m.*
**5A.1 Reliability of Single-Layer $MoS_2$ Field-Effect Transistors with $SiO_2$ and hBN Gate Insulators**
*Y. Illarionov, M. Waltl, M. M. Furchi, T. Mueller, T. Grasser*, TU Wien*

We perform a detailed study of both hysteresis and bias-temperature instabilities (BTI) in single-layer MoS2 FETs with SiO2 and hBN insulators and capture the correlation between these phenomena. We show that our transistors exhibit a better hysteresis and BTI stability than similar devices reported previously. Moreover, we demonstrate that using of hBN as a gate insulator reduces the impact of slow traps and improves the BTI reliability, while the hysteresis for MoS2/hBN FETs is dominated by ultra-fast traps. However, at higher temperature the BTI reliability of hBN gate insulator is reduced due to thermally activated charge trapping.

*2:25 p.m.*
**5A.2 Nondiffusive Heat Dissipation from a Pulse-Heated Conductive Filament in RRAM (Invited)**
*K. Regner, J. A. Malen Carnegie Mellon University*

Here, we discuss experimental and theoretical studies of nondiffusive thermal transport, which occurs when geometrical length scales are comparable to energy carrier mean free paths (MFPs). We expand upon a previous study that emphasizes the importance of nondiffusive thermal transport in resistive-switching random access memory (RRAM). To model this behavior, an approximate solution to the Boltzmann transport equation (BTE), under the relaxation time approximation in the cylindrical geometry, is derived for the case of an arbitrary, temporally periodic surface temperature boundary condition. This boundary condition coupled with the BTE more realistically models switching stimuli in an RRAM device.

*2:50 p.m.*
**5A.3 Fundamental Study of the Apparent Voltage-dependence of NBTI Kinetics by Constant Electric Field Stresses in Si and SiGe Devices**
*S. Mukhopadhyay, J. Franco, A. Chasin, P. Roussel, B. Kaczer, G. Groeseneken, N. Horiguchi, D. Linten, A. Thean, imec*

The standard BTI time-to-failure (TTF) extrapolation used in industrial R&D is based on simple power-law acceleration models for both time- and voltage-dependences. This approach implicitly assumes the time- and voltage-dependences to be mutually uncorrelated, i.e., the time acceleration exponent (n) is assumed to be a constant, independent of the considered stress voltage range, and vice versa, the voltage acceleration exponent is independent of the considered stress test duration. However, for Ge,SiGe and even for Si, for both planar and finFET devices, the NBTI time exponent has been observed to reduce for increasing stress voltages. This poses concerns for device lifetime extrapolation and for correct reliability benchmarking across different gate stacks.This work brings out the challenges

of the standard BTI TTF extrapolations based on simple power-laws for cross comparison of different technologies. When standard constant voltage stress are performed, field reduction effect can be more severe in some technologies, and voltage dependent time evolutions can cause anomaly in TTF prediction. A novel constant-field experiment has been implemented. This approach revealed an intrinsic uncorrelated nature of time-dependence with stress voltage. This approach can be used for a fair cross-comparison of different technology, avoiding the different impact of field reduction on different device families.

*3:45 p.m.*
**5A.4 Hot Carrier Stress: Aging Modeling and Analysis of Defect Location**
*G. Torrente; X. Federspiel, D. Rideau, F. Monsieur, C. Tavernier, J. Coignus*, D. Roy, G. Ghibaudo**, STMicroelectronics, *CEA, LETI, **IMEP-LAHC*
In this paper a complete TCAD model addressing Hot Carrier Degradation for Flash technology is presented and its validity range extended respect to our previous work. Using electrical parameter correlation, a simple technique for the analysis of trap distribution location is presented and insights at different stress conditions are provided.

## *Session 5B - Interconnect Metallization Reliability*

Session Co-Chairs: *Feng Xia, Intel, Ki-Don Lee, Samsung*
Section E

*1:55 p.m.* - Session Introduction

*2:00 p.m.*
**5B.1 Thermal Characterization and Challenges of Advanced Interconnects (Invited)**
*B. Li, A. Kim, C. Christiansen*, R. Dufresne*, C. Burke*, D. Brochu*, IBM Systems, *Globalfoundries*

Technology scaling and driving to high performance have led to more joule heating in both devices and interconnects. Since temperature is one of the most sensitive factors impacting interconnect reliability, this paper focuses on the thermal characteristics of metal lines with different geometries and surroundings to accurately assess local temperature of different circuit designs. The experimental results reported can be used as basic input parameters and calibration baseline for thermal model development and simulations.

*2:25 p.m.*
**5B.2 Electromigration Failure of Circuit Interconnects**
*M.-H. Lin, A. Oates, TSMC*

The analysis of steady-state stress can accurately predict the locations of electromigration vulnerabilities in multi-segment. The presence of active sinks and reservoirs significantly reduce failure times of short-length conductors. Electromigration failures are found at either the first cathode via in sink/reservoir segments or common-via region, where is correlated with locations of maximum stress.

*2:50 p.m.*

**5B.3 1/f Noise Measurements for Faster Electromigration Characterization**

*S. Beyne, K.Croes, I. De Wolf, Z. Tőkei, IMEC*

The application of 1/f noise measurements to speed up electromigration (EM) testing and provide a better understanding of the underlying mechanisms of electromigration in advanced microelectronics interconnects is investigated. It is shown that 1/f noise measurements can be used for early EM damage detection during EM stress, before any changes in the resistance of the sample are observable. Also, the temperature dependence of the low frequency noise is used to calculate activation energies, which are then demonstrated to be similar to values found for electromigration using standard EM tests. Furthermore, the 1/f noise technique is used to assess and compare the EM properties of various advanced integration schemes and different materials. The 1/f noise measurements provide new evidence for the importance of grain boundary diffusion as a dominant EM failure mechanism in highly scaled interconnects.

*3:45 p.m.*

**5B.4 Engineering the Failure-Free Lifetime for Cu Vias**

*G. Hall, D. Allman, M. Eda, T.F. Long, II, *ON Semiconductor*

Ensuring the reliability of dual-damascene/low-k back-endof- line (BEOL) metallization requires predictive accelerated failure time (AFT) models of stress migration (SM) and stress induced voiding (SIV). High Temperature Storage (HTS) tests have indicated that competing rates of diffusion and stress build-up leads to a generalized Eyring model, of the AFT. While the model describes SM qualitatively well, it cannot predict quantitatively the inverse-bathtub shape of the distribution of SIV failures in experiment, and the impact of factors such as linewidth, microstructure, and the non-local nature of void interactions and vias. A more complete model is discussed here, which addresses the shortcomings of all previous approaches to SIV, and can be used to model SIV failures to identify design and process conditions which have a failure-free lifetime (FFL). A surprising novelty of the approach is that the physics of stress relaxation leads us to scaling functions which focus on the right-hand side of the distribution, rather than the usual left/early failures.

*4:10 p.m.*

**5B.5 Influence of Metallization Layout on Aging Detector Lifetime under Cyclic Thermo-Mechanical Stress**

*G. Pham, M. Ritter, M. Pfost*, Reutlingen University, *University of Innsbruck*

The influence of the layout on early warning detectors in BCD technologies for metallization failure under cyclic thermo-mechanical stress was investigated. Different LDMOS transistors, with narrow or wide metal fingers and with or without embedded detectors, were used. The test structures were repeatedly stressed by pronounced self-heating until failure (a short circuit) was detected. The results show that the layout of the on-chip metallization has a large impact on the lifetime. A significant influence of the detectors on the lifetime was also observed, in our case causing a reduction of more than a factor of two, but only for the test structure with narrow metal fingers. The experimental results are explained by an efficient numerical thermo-mechanical simulation approach, giving detailed insights into the strain distribution in the metal system. These results are important for aging detector design and, morever, for LDMOS on-chip metal layout in general.

## *Session 5C - Soft Errors*

Session Co-Chairs: *Balaji Narasimham, Broadcom, Ethan Cannon, Boeing*
Section F/G

*1:55 p.m.* - Session Introduction

*2:00 p.m.*
**5C.1 Muon-induced Soft Errors in 16-nm NAND Flash Memories**
*M. Bagatin, S. Gerardin, A. Paccagnella, A. Visconti*, S. Beltrami*, M. Bertuccio*, K. Ishida**, C. Frost, A. Hillier***, V. Ferlet-Cavrois^, University of Padova, *Micron Technology Inc., **RIKEN Nishina Center, ***STFC Rutherford Appleton Laboratory, ^ESA ESTEC, TEC-QEC*

Flash memories based on the floating gate architecture are sensitive to ionizing radiation at sea level, including atmospheric neutrons and alpha particles. No data in the literature are available on the sensitivity of Flash memories to muons. These particles, although very lightly ionizing, are the most abundant at sea level and have been reported to cause upsets in advanced SRAMs through direct ionization. The purpose of this contribution is to present the first experimental investigation of single event upsets induced by muons in 16-nm NAND Flash memories, using accelerated tests. The experimental results are discussed in terms of threshold voltage shifts and raw bit errors, showing that muon-induced upsets are indeed possible also in Flash memories.The threshold LET value for advanced samples is finally analyzed.

*2:25 p.m.*
**5C.2 Impact of Alpha-Radiation on Power MOSFETs**
*G. Schindler, K.-H. Bach, P. Nelle, M. Deckers, A. Knapp, K. Ermisch, C. Feuerbaum, W. v. Emden*, Infineon Technologies, *Robert Bosch GmbH*

In this paper it is shown how the impact of alpha particles in the gate oxide of a power MOSFET leads to a local reduction of the threshold voltage Vth. Evidence is presented that radioactive impurities in the mold compound or solder material of the package indeed are the root cause for such effects observed in long term measurements with electrical gate bias. Furthermore the influence of alpha impacts on application and reliability is investigated.

*2:50 p.m.*
**5C.3 Temperature Dependence of Soft-Error Rates for FF designs in 20-nm Bulk Planar and 16-nm Bulk FinFET Technologies**
*H. Zhang, H. Jiang, T. Assis*, D. Ball, K.Ni, J. S. Kauppila, R. Schrimpf, L. Massengill, B. Bhuva, B. Narasimham**, S. Hatami**, A. Anvar**, A. Lin**, J. K Wang**, Vanderbilt University, *Robust Chip, Inc, **Broadcom Corporation*

Alpha particle-induced flip-flop soft-error rates (SER) for 20-nm bulk planar and 16-nm bulk FinFET technologies are characterized over temperature with different supply voltages. Experimental results indicate that the 16-nm FinFET SER show negligible change with temperature while the 20-nm planar SER increase ~2x over the same temperature range.

# POSTER PRESENTATIONS

# WEDNESDAY, April 20, 2016

### 6:30 p.m. – 9:30 p.m.
### Exhibit Hall C

## *Compound/Opto Electronics*

**CD-1 On Conduction Mechanisms through SiN/AlGaN based Gate Dielectric and Assessment of Intrinsic Reliability**
*A. Banerjee, P. Vanmeerbeek, L. De Schepper, S. Vandeweghe, P. Coppens, P. Moens, ON Semiconductor*

The first section of this article focuses on the investigations of the gate leakage conduction mechanisms under forward and reverse bias conditions using temperature dependent Jg-Eg characteristics on a Silicon Nitride (SiN)/AlGaN based Metal-Insulator-Semiconductor (MIS) structure. TCAD study under forward bias conduction show majority of the voltage drop on the SiN layer only. The model fitting the electrical characteristics was observed to be Poole- Frenkel (PF) emission. Under reverse bias condition, the entire voltage drop occurs on the entire SiN/AlGaN/GaN. The conduction mechanism responsible for the leakage was found to be Fowler-Nordheim (FN) tunneling along with a thermionic emission component. Second section of this article focuses on the Time Dependent Dielectric Breakdown (TDDB) measurements and lifetime extrapolation of the SiN/AlGaN based di-electric stack. TDDB measurements were done under constant field stress for different temperatures. Normalization of the data exhibited only field accelerated degradation with no influence from the temperature.

**CD-2 Correlation Between Dynamic $R_{DSon}$ Transients and Carbon Related Buffer Traps in AlGaN/GaN HEMTs**
*F. Iucolano, A. Parisi, S. Reina, A. Patti, S. Coffa, G. Meneghesso*, G. Verzellesi**, F. Fantini**, A. Chini**, STMicroelectronics, *University of Padova, **University of Modena and Reggio Emilia*

The on resistance increment observed when the device is operated at high drain-source voltages is one the topics that limits the performance of the AlGaN/GaN HEMT devices. In this paper, the physical mechanisms responsible of the RDSon degradation are investigated. The dynamic RDSon transient method is used in order to get insight to characterize the traps states. By calculating the Arrhenius plot associated with the RDSon transients an activation energy of 0.86eV was extracted, that can be correlated to the traps due to the incorporation of Carbon inside the buffer. This hypothesis was further supported by the analyses performed on a simpler structure (TLM). By applying a negative substrate bias the effect of only the buffer traps was studied. A fairly close value of the activation energy (0.9eV) to the one extracted when analyzing the RDSon transient was obtained.

**CD-3 Investigation of Trapping Effects on AlGaN/GaN HEMT under DC Accelerated Life Testing**
*W. Sun, C. Lee*, P. Saunier*, S. Ringel, A. Arehart, Ohio State University, *Qorvo Inc*

GaN-based high electron mobility transistors (HEMTs) were subjected to DC-based accelerated life testing to determine which defect levels form or are activated, and how they impact the static and dynamic HEMT performance. The primary static changes were a negative shift of the threshold voltage and an increase in knee walkout/onresistance. The primary dynamic effect of the stressing appeared in the form of a time-dependent increase in the onresistance, and this was found to correlate to first order with formation and/or activation of traps at EC-0.57 and EC-0.72 eV traps that contributed to the dynamic changes, and the EC-1.5 eV trap was likely responsible for the static change in onresistance. Trapping kinetics analysis revealed that the physical sources for the EC-0.57 and EC-0.72 eV states are not simple, ideal, non-interacting point defects, but instead are associated with physically extended defects, such as dislocations, and/or defect complexes.

**CD-4 Evaluations of Threshold Voltage Stability on COTS SiC DMOSFETs Using Fast Measurements**
*D. Habersat, R. Green, A. Lelis, US Army Research Laboratory*

Threshold voltage (*VT*) stability of commercial SiC DMOSFETs during bias-temperature stressing was evaluated using the fast-*ID* and fast *ID-VGS* measurement techniques at both room and elevated temperatures. Unipolar bias stress results confirmed that there is a rapid recovery of *VT* and that all vendors' devices showed the same basic charge-trapping behavior, although some differences were observed in negative bias response at high temperatures. In situ *VT* measurements during 10 kHz gate switching showed stable device operation at room temperature but accelerating *VT* drift and increasing switching oxide trap densities when operated at 175 °C. *VT* hysteresis during high temperature gate switching indicates the presence of a mobile ion or polarization effect in addition to the expected interface- and oxide-trap charging mechanisms.

**CD-5 Device Breakdown Optimization of Al2O3/GaN MISFETs,** *X. Kang, S. Yamazaki, K. Takeuchi, Chuo University*

In this paper we demonstrate a solution to achieve robust enhancement-mode Al2O3/GaN MISFETs with a high breakdown voltage and suggest a possible model for the device off-state breakdown. It is found that the device breakdown exhibits different gate voltage dependence for different surface treatments before the gate dielectric deposition. The device performance is greatly improved by using an in-situ surface plasma treatment. The improved device performance is explained by a reduction of traps at the Al2O3/GaN interface, which finally leads to a reduction in the amount of trapped positive charges and associated with that a reduction of the effective electric field across the gate dielectric when the device isin off-state. Several experimental results support this hypothesis: (1) The recoverable negative threshold voltage shift after reverse gate bias depends on the interface clean before gate dielectric deposition, (2) The reverse bias gate dielectric breakdown voltage is improved by this interface plasma treatment, although the forward bias gate dielectric breakdown voltage is identical.

## *Design for Circuit Reliability*

**CR-1 The Impact of Process Variation and Stochastic Aging in Nanoscale VLSI**
*S. Kiamerh, P. Weckx*, M. Tehoori, B. Kaczer*, H. Kukner*, P. Raghavan*, G. Groeseneken**, F. Catthoor*, Karlsruhe Institute of Technology, *IMEC, **KU Leuven*

With the down-scaling of CMOS technology into deep nano-scale era, negative-bias temperature instability (NBTI) effect becomes stochastic due to its widely distributed defect parameters. As a result, the delay degradation due to intrinsic variability of NBTI becomes also stochastic and the matter is aggravated when it is combined with process variation (PV). Accurate stochastic timing analysis of the circuit becomes very important in this case since over and under margining can lead to significant performance or yield loss (timing failure), respectively. This paper proposes a scalable flow and investigates the combined effect of stochastic NBTI and process variation on the performance of the VLSI design at the circuit level in a 7 nm FinFET technology node by abstracting atomistic NBTI models (for the stochastic behavior) to the circuit timing analysis flow.

**CR-2 Mismatch Circuit Aging Modeling and Simulations for Robust Product Design and Pre-/Post-Silicon Verification**
*H. Shim, Y. Kim, J. Jeon, Y. Cho, J. Park, S. Pae, H. Lee, Samsung Electronics*

As technology scales down, PMOS NBTI-induced mismatch, in addition to the NBTI mean-shifts and time0-Vt variation, is critical for designing circuitry having matched pair transistors, such as OP amplifier. This paper covers mismatch aging models incorporated into design simulation tool for PMIC products and used the Monte-Carlo simulation to consider process and systematic variations for robust design. Circuit simulation for PMIC OP Amp and its output characteristics were investigated and then further validated through the post-silicon HTOL stress. The pre-silicon simulation further enables to optimize HTOL stress conditions.

**CR-3 Aging of IO Overdrive Circuit in FinFET Technology and Strategy for Design Optimization**
*S.-E. Liu, M.-H. Yu, Y.-J. Chen, J.-Y. Jao, M.-Z. Lin, Y.-H. Fang, M.-J. Lin, MediaTek*

We investigated aging property of FinFET-based I/O overdrive circuits (IP) and proposed design strategies of optimization among performance/area/reliability. Aging behavior of I/O overdrive IP with 16nm FinFET process has been extracted and compared with 20nm planar-transistor process. Both pulldown and pull-up driving degradation are worse in the FinFET than planar IP. An aging simulation framework was built from transistor-level aging databases and further calibrated by an empirical equation and IP-level measurements. Finally, a design guideline was discussed and proposed to pursue balance of performance/ area/reliability, which is thus improved 13%/8%/37% respectively in our optimized design.

**CR-4 Robustness of Timing in-situ Monitors for AVS Management**
*A. Benhassain, F. Cacho, V. Huard, S. Mhira, L. Anghel*, C. Parthasarathy, A. Jain, A. Sivadasan, STMicroelectronics, *Grenoble University*

This paper deals with the fundamental aspects of the introduction of aging sensor in digital circuit, describing a new In-situ Timing Monitor (ISM), insertion flow and experimental results .

## *Dielectric Reliability (Front-end and Back-end)*

**DI-1 Moisture Impact on Dielectric Reliability in Low-k Dielectric Materials**
*K.-D. Lee, Q. Yuan, A. Patel, Z. Mai, L. Brown, S. English, Samsung Austin Semiconductor*

With intentional moisture uptake and removal, we modulate the moisture level in porous low-k dielectric materials, and investigate the moisture impact on dielectric reliability at a wide range of stress conditions. From this study, we confirm moisture can cause a significant degradation in dielectric reliability (i.e., x1.0E-06 in TDDB lifetimes) . Interestingly, the moisture impact is not permanent (with good Cu-diffusion barrier) and can be restored effectively with a high temp annealing at ≥ 350°C. Different from previous studies, moisture does not always increase the leakage currents nor change the TDDB modeling parameters, indicating there are at least two moisture states in porous low-k dielectric materials. In this paper, we will discuss the moisture-induced reliability degradation mechanisms.

**DI-2 Impact of Trap Creation at $SiO_2$/Poly-Si Interface on Ultra-thin $SiO_2$ Reliability**
*Y. Mitani, M. Suzuki, Y. Higashi, R. Takaishi, Toshiba Corporation*

The relationship between TDDB characteristics of the devices having ultrathin SiO2 as gate dielectrics and the hydrogen-related trap creation have been re-investigated from the viewpoint of the oxidation process dependence. In order to study the influence of hydrogen on the reliability, deuterium isotope effect has been used. As a result, the Weibull distributions of time-to-breakdown (tBD) depends on the oxidation process condition even under the same oxidation temperature. Trap creation at gate oxide interface strongly correlates to the dielectric breakdown in ultra-thin gate oxides However, this oxidation process dependence could not be explained only by the amount of hydrogen release from SiO2/Si substrate interface From the experimental results of low-voltage SILC, it can be concluded that not only the released hydrogen from SiO2/Si substrate interface but also those from Poly-Si/SiO2 interface correlates to the breakdown mechanisms.

**DI-3 A Fast Reliability Screening Technique for Identification of Trap Generation**
*K. Joshi, Z.-R. Xiao, S.-H. Gao, C. Huang, T.-M. Shen, P.J. Liao, Y.-H. Lee, J-R. Shih, Taiwan Semiconductor Manufacturing Company*

SILC spectrum technique is used to identify trap generation location in both PMOSFETs and NMOSFETs under BTI stress. It is validated using SILC spectrum technique that BTI stress in PMOSFETs leads to trap generation in IL/HK intermix whereas in NMOSFETs leads to trap generation in HK layer. Atomistic simulations are further performed to calculate formation energy for oxygen vacancies in various gate oxide layers. It has been validated that it is easy to generate hole traps in IL/HK intermix region under NBTI stress in PMOSFETs and easy to generate electron traps in HK layer in NMOSFETs under PBTI stress. The advantage of this technique is its ease of use and higher throughput thus making it an ideal tool for a quick scanning of trap generation locations and to understand the reliability strength of each layer under different processing conditions.

**DI-4 Correlation between the Variation in the Initial Current at Stress and the Variation in the Failure Time During TDDB Testing of BEOL Structures**
*R. Filippi, C. Christiansen, A. Kim*, B. Li*, P-C. Wang, Globalfoundires, *IBM*

A novel approach for estimating variation in the TDDB failure time is reported. The results for various test structures reveal that variation in the initial current at stress reasonably predicts variation in the TDDB failure time. The approach is a non-destructive method that only requires a current measurement, making it an efficient monitor of the expected TDDB lifetime behavior during manufacturing of an established process.

**DI-5 Towards an Appropriate Accelerate Model for BEOL TDDB**
*R. Muralidhar, E. Linger, T. Shaw**, A. Kim, G. Bonilla*, IBM TJ Watson Research Center*

We have evaluated the veracity of BEOL acceleration models using the largest set of data spanning 3 pitches. The raw data indicates same acceleration trends in the 3 pitches enabling them to fall into a universal curve by re-normalization to account for different areas. While the Root-E (RE), Impact Damage and Power-Law (PL) models fit data over entire range well, it is seen that only the Impact Damage and Power Law models predict the low field data when high field data alone is used to fit the models. This ability to extrapolate and the constancy of acceleration factors at low and high fields makes these models more appropriate for determining lifetime at operating conditions from a fit of high field data alone. While the ID model has 3 parameters and presents fitting challenges, the PL model is a good practical alternative and may have its physical basis on arguments based on scaling theory. The paper will additionally discuss in detail statistical analysis including clustering model, fitting aspects of ID model and physical basis of the power-law model from scaling point of view.

**DI-6 Evaluation of Inter and Intra Level TDDB of Cu/Low-k Interconnect for High Voltage Application**
*M. Lin, C. Yang, H.-Y. Chen, A. Juan, K.C. Su, United Microelectronics Corp.*

The conduction current and TDDB of intra and two kinds of inter level low-k dielectric structures for high voltage application are studied. Electrical field distributions are different on the different structures and impact the TDDB results. Failure analysis shows the Cu ion diffusion and SiCN interface are the dominant impact factor of the low-k dielectric breakdown. An inter level layout design principle to improve dielectric reliability under high voltage operation is suggested.

**DI-7 Effect of $H_2O$ on TDDB for a Range of ULK ILD Materials with Varying Damage Resistance for Robust and Weak Liners**
*E. Linger, R. Laibowitz*, T. Shaw, S. Cohen, A. Raja*, IBM TJ Watson Research Center, *Columbia University*

In this study we look at the correlation between TDDB lifetime, in the presence of intentionally introduced H2O and top surface damage for different ILD materials using a robust liner. The activation energy for the movement of loosely bound physi-adsorbed H2O has been obtained using AC loss measurements. We also explore the role of moisture in drawing Cu out of metal lines through an intentionally fabricated thin/weak liner under prolonged stress at a relatively low voltage. AC loss, I-V, triangular voltage sweep (TVS) and TDDB measurements all provide evidence that Cu is migrating out of the lines into the ILD.

**DI-8 Reliability-Performance Trade-off For Work- Function Optimization In Advanced Node Replacement Metal Gate Technology**
*R. Ranjan, T. Nigam, B. Parameshwaran, Y. Liu, S.F. Yap, Globalfoundries*

In this work, we explore the complex interaction of the gate stack process and time-dependent-dielectric breakdown (TDDB) in high-K (HK) replacement metal gate (RMG) technology. TDDB is a key reliability metric governing the product lifetimes under long-term operation. Based on this study, it is observed that TDDB is greatly modulated by the proximity of Al to the MG/HK interface. The key parameter modulated by gate stack optimization is voltage acceleration exponent (VAE) for TDDB. All observations indicate higher VAEs can be achieved by keeping the Al away from the MG/HK interface.

## *ESD and Latch-up*

**EL-1 ESD Self-Protection Design on 2.4-GHz T/R Switch for RF Application in CMOS Process**
*C.-Y.Lin, R.-H. Liu*, M.-D. Ker*, National Taiwan Normal University, *National Chiao Tung University*

The RF transceiver front-end for 2.4-GHz applications realized by a fully integrated T/R switch with ESD self-protection capability is presented in this work. Experimental results show that the proposed design can provide enough ESD self-protection capability with good RF performances.

**EL-2 Failure Mechanism of High-Voltage Isolated Lateral Diffused NMOS under High-Current Events**
*C.-H. Wu, J.-H. Lee*, C.-H. Lien, National Tsing Hua University, *Globalfoundries*

In this study, the mechanism of the effect of a high-voltage (HV) NWell guardring (NW-GR) on the electrostatic discharge (ESD) robustness of the HV isolated lateral diffused NMOS (HV ISO-LDNMOS) is investigated. The device fails on low-voltage ESD zapping events when the HVNW-GR is connected to the drain, whereas the device passes these events once it is floated.

**EL-3 Optimization of PESD Implant Design for ESD Robustness of 5V Drain-Back N-LDMOSFET**
*C. Chiang, P.C. Chang, P.-S. Tseng, P.-Y. Lai, H. Tang, K.C. Su, UMC*

An N-LDMOS ESD protection device with drain back and PESD optimization design is proposed. With PESD layer enclosing the N+ drain region, a parasitic SCR is created to achieve high ESD level. When PESD is close to gate, the turn-on efficiency can be further improved (Vt1: 11.2V reduced to 7.2V) by the punch-through path from N+/PESD to PW. The proposed ESD N-LDMOS can sustain over 8KV HBM with low trigger behavior.

**EL-4 On-Chip Protection in Precision Integrated Circuits Operating at High Voltage and High Temperature**
*J. Salcedo, J.-J. Hajjar, J. Zhao, Analog Devices*

A new high voltage swing bipolar ESD (electrostatic discharge) protection device for enabling low leakage precision mixed-signal interface circuits (ICs) operating at high voltage (~ 40V to 60V) and high temperature (~125°C to 200°C) is presented. Under these operating conditions, parasitic structures in junction-isolated high voltage process technologies induce unexpected shift in the leakage current over time, leading to malfunction in the precision high voltage input/output interface circuit. A proposed device design addresses the low leakage targets at the mentioned operating conditions, while achieving the required ESD robustness of the high voltage interface for industrial applications.

**EL-5 Improving the Long Pulse Width Failure Current of NPN in BiCMOS Technology**
*Y. Xiu, A. Appaswamy, Z. Chen*, A. Salman, M. Dissegna, G. Boselli, E. Rosenbaum*, Texas Instruments, *University of Illinois at Urbana-Champaign*

The pulse width dependency of the failure current for NPN structures in a 0.18-µm BiCMOS technology is studied using measurements and TCAD simulation. The desired "Wunsch-Bell" behavior is not observed due to formation of current filaments in this device; however, the failure current for long pulse widths can be increased by layout changes.

**EL-6 Analysis of ESD Effects on Organic Thin-Film-Transistors by Means of TLP Technique**
*N. Wrachien, M. Barbato, A. Cester, A. Rizzo, G. Meneghesso, R. D'Alpaos*, G. Turatti*, G. Generali*, M. Muccini**, University of Padova, *ETC srl, **CNR-ISMN*

We analyzed the effects of Electrostatic Discharge events on large area high voltage Organic Thin Film Transistors, using the transmission line pulsing technique. These transistors survived ESD events exceeding 500V. A partial dielectric breakdown occurred at voltage higher tan 600V. Small mobility and threshold voltage variations are observed, prior breakdown.

**EL-7 Unique ESD Behavior and Failure Modes of AlGaN/GaN HEMTs**
*B. Shankar, M. Shrivastava, Indian Institute of Science*

Present experimental study reports various failure modes under ESD stress conditions and distinct ESD behavior of AlGaN/GaN HEMTs for the first time. Effect of MESA isolation and gate finger on the ESD behavior of HEMTs is analyzed. Effect of pulse width on ESD robustness and trigger voltage is observed and a unique power law like behavior is found. Cumulative nature of device degradation under ESD stress condition is discovered. Correlation between depth of snapback and failure threshold with % device degradation is found. Finally, impact of inverse piezoelectric effect in AlGaN/GaN system, fringing electric field, role of contact resistivity, temperature and field induced contact metal migration and premature breakdown of parasitic MESA Schottky junction are studied in context to AlGaN/GaN HEMT failure ESD conditions.

**EL-8 New Insights on the ESD Behavior and Failure Mechanism of Multi Wall CNTs**
*A. Mishra, M. Shrivastava, Indian Institute of Science*

ESD conditions, through inner and outer shells of MWCNT is explored. ESD time scale current annealing behavior of outer and inner shells was discovered, which is unique to MWCNTs. Shells - by - shell failure was confirmed to be the universal failure mode of MWCNTs. Failure behaviors of suspended and collapsed (tubes resting on dielectric surface) tubes in single and bundled configuration are discussed.

## *System Reliability*

**ES-1 Long-Term Reliability of a Hard-Switched Boost Power Processing Unit utilizing SiC Power MOSFETs**

*S. Ikpe, J.-M. Lauenstein, G. Carr*, D. Hunter*, L. Ludwig, W. Wood, C. Iannello, L. Del Castillo*, F. Fitzpatrick, M. Mojarradi, Y. Chen, NASA, *Jet Propulsion Laboratory California Institute of Technology*

With the expedient maturation of Silicon-Carbide (SiC) device technology, a great deal of interest has been generated in the development of switching power applications capable of harnessing the inherent wide-bandgap (WBG) properties of the material. SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) in particular, offer significant benefit over their Silicon counterparts. The potential for lower total switching losses, higher breakdown field tolerance and superior thermal performance make SiC devices highly attractive for both high temperature and extreme environment applications. Though successful power conversion implementations show promise [1], these noteworthy device innovations have yet to directly translate into pragmatic power conversion systems. Therefore, it is still necessary to evaluate the application-specific performance of these devices to fully understand thermal limitations as well as estimate the overall device reliability. This paper describes a design-for-reliability approach for an innovative power processing architecture intended for in-space solar electric propulsion (SEP) systems. The work herein also presents reliability data on CREE's commercially available N-channel enhancement mode SiC MOSFETs.

## *Failure Analysis*

**FA-1 Dynamic Avalanche in Charge-Compensation MOSFETs Analyzed with the Novel Single Pulse EMMI-TLP Method**

*T. Chirila, T. Reimann*, M. Rüb, University of Applied Science Jena, *Technische Universität Ilmenau*

As a main switch in a broad range of applications, the Charge-Compensation MOS Transistor must be able to withstand the avalanche multiplication regime. Using the classical rating method for avalanche robustness, two destruction limits have been identified – thermal and current limit. However, up to date there is no complete understanding of current induced failure mechanisms. In this paper we combine single transmission line pulses with emission microscopy in order to bring more insight into these kinds of destruction modes. We identify three different avalanche regimes and observe the occurrence of current filaments. We provide an interpretation for filament formation.

**FA-2 Fast 3D Electro-Optical Frequency Mapping and Probing in Frequency Domain**

*K. Melendez*, K. Sanchez*, P. Perdu*, K. Melendez, D. Lewis, Bordeaux University, *CNES*

The main goal of this paper is to show the capability of extracting several frequencies at one electro-optical scanning in order to reconstruct few 512 by 5 12 pixels images. With these 3D data (X and Y are pixels and Z is the frequency locked), it is possible to study several frequencies in one time and to reconstruct the original signal waveform at each pixel.

**FA-3 Direct Photo Emission Monitoring for High Power IGBT during Avalanche Operation**

*T. Matsudai, K. Endo, T. Ogura, T. Matsumoto*, K. Uchiyama*, K. Koshikawa*, Toshiba Corporation, *Hamamatsu Photonics K.K.*

IGBTs have been developed extensively to improve trade-off relation between on state losses and switching losses. Therefore the reliability enhancement of IGBTs is very important technology. For the past failure analyses, only the final destruction point have been observed under testing. With this way, it is difficult to perform physical analysis,

because the process of the destruction phenomenon is unknown. In this work, our target is investigating the avalanche phenomenon of IGBTs, directly. During avalanche operation, it is well known that the formation of current filament appears and visible light is emitted in the device. For the first time, we have succeeded observing the photo emission directly from avalanche phenomena under UIS (Unclamped Inductive Switching) condition of IGBTs using the streak camera. We have also measured moving the emission region in edge termination area.

## *Interconnect Metallization Reliability*

**IT-1 Optimizing Cu Barrier Thickness for Interconnects Performance, Reliability and Yield**

*T. Shen, B. Rajagopalan, M.C. Silvestre, E. Ramanathan, A.S Mahalingham, W. Zhang, K.B. Yeap, P. Justison, Globalfoundries*

Cu barrier thickness optimization on our 90nm pitch Vx/Mx layers with porous ULK SiCOH ($\kappa$=2.55) was systematically investigated. Both via resistance and intrinsic EM performance favors thinner TaN and Ta films, however, the robustness of the plating requires thicker Ta to improve seed quality that withstand dissolution during plating. Overall, a thin TaN barrier with moderate thick Ta provides the optimum solution for performance, reliability and yield.

**IT-2 Semi-empirical Interconnect Resistance Model for Advanced Technology Nodes: A Model Apt for Materials Selection Based upon Test Line Resistance Measurements**

*P. Roussel, I. Ciofi, R. Degraeve, V. Vega, N. Jourdan, R. Baert, D. Linten, J. Bömmels, Z. Tőkei, G. Groeseneken*, A. Thean, IMEC, *KU Leuven*

As the dimensions of interconnects shrink into the nanoscale for the NX node, their electrical conductivity becomes dependent on their size, even at room temperature. This paper presents a semi-empirical interconnect resistance model apt for fitting wire resistance data. The model combines grain boundary and sidewall scattering effects with the impact of Line Edge Roughness (LER). It allows subsequent selection of interconnect metallization material candidates through extrapolation to target widths of future technology nodes on the basis of their wire resistance, while still considering other performance metrics like yield, electromigration and TDDB. A refined model parameter calibration procedure, that accounts for interconnect height and width variability between the test structures is demonstrated for two Cu metallization schemes, employing Co and Ru as a metal liner, respectively. The model allows inclusion of more accurate, geometry dependent interconnect resistance estimators in higher abstraction level simulators, enabling a more realistic assessment of the impact of BEOL parasitics on circuit delay at advanced technology nodes.

**IT-3 Electromigration: Multiphysics Model and Experimental Calibration**

*G. Marti, W.H. Zisser, L. Arnaud*, Y. Wouters**, STMicroelectronics, *CEA-Leti Minatec, **SIMAP, ***Technische Universität Wien*

Electromigration (EM) is one of the main reliability failure mechanism of integrated circuit interconnects. The result of EM in copper interconnects is void nucleation and growth close to the cathode. For EM tests, most commonly elementary structures are stressed under accelerated conditions (high current and temperature) until degradation occurs. The understanding of the main mechanism governing the reliability of copper interconnects is mandatory to develop lifetime predictive laws and allows architecture optimizations of future MOS technologies. Thus more accurate and less pessimistic full-chip EM assessment and mean-time-to-failure (MTTF) prediction will require a development of new methods that deal with the design of the grid structure and take redundancy into account. We describe in this work a new methodology to calibrate an existing EM numerical model. The effective charge (Z*) of this technology has been extracted experimentally. Furthermore, the proposed post-processing method allowed us to find the critical tensile stress of void nucleation. This method allows to answer design requests about void nucleation

which may depend upon geometry and process conditions. Taking into account these parameters will increase the accuracy of reliability prediction at design level and help designers with high current density needs.

## *Memory*

**MY-1 The Complete Time/Temperature Dependence of I-V drift in PCM Devices**
*M. Le Gallo, A. Sebastian, D. Krebs, M. Stanisavljevic, E. Eleftheriou, IBM Research - Zurich*

Phase-change memory (PCM) devices are expected to play a key role in future computing systems as both memory and computing elements. Hence, a comprehensive understanding of the change in the current/voltage (I-V) characteristics of these devices with time and temperature is of considerable importance. Here, we present a unified drift model to predict the I-V characteristics at any instance in time and at any temperature. The model was validated on large sets of experimental data for an extensive range of time (10 orders of magnitude) and temperatures (180 - 400 K), different phase-change materials and a collection of 4k cells from a PCM chip.

**MY-2 Reliability-Performance Tradeoff between 2.5D and 3D-Stacked DRAM Processors**
*S.M Hassan, W. Song, S. Mukopadhyay, S. Yalamanchili, Georgia Institute of Technology*

MY-3 Root cause of degradation in novel HfO2-based Ferroelectric Memories M. Pešić, F. Fengler, S. Slesazeck, U. Schröder, T. Mikolajick, L. Larcher*, A. Padovani*, NaMLab gGmbH, *University of Modena and Reggio EmiliaSummary:HfO2-based ferroelectrics reveal full scalability and CMOS integrability compared to perovskite-based ferroelectrics that are currently used in non-volatile ferroelectric random access memories (FeRAMs). Up to now, the mechanisms responsible for the decrease of the memory window have not been revealed. Thus, the main scope of this study is an identification of the root cause for the endurance degradation. Utilizing trap density spectroscopy for examining defect evolution with cycling of the device studied together with modeling of the degradation resulted in an understanding of the main mechanisms responsible for degradation of the ferroelectric behavior.

**MY- 3 Root Cause of Degradation in Novel $HfO_2$-based Ferroelectric Memories**
*Milan Pešić, Franz P. G. Fengler, Stefan Slesazeck, Uwe Schroeder, Thomas Mikolajick**
*NaMLab gGmbH*

HfO2-based ferroelectrics reveal full scalability and CMOS integratability compared to perovskite-based ferroelectrics that are currently used in non-volatile ferroelectric random access memories (FeRAMs). Up to now, the mechanisms responsible for the decrease of the memory window have not been revealed. Thus, the main scope of this study is an identification of the root causes for the endurance degradation. Utilizing trap density spectroscopy for examining defect evolution with cycling of the device studied together with modeling of the degradation resulted in an understanding of the main mechanisms responsible for degradation of the ferroelectric behavior.

**MY- 4 Voltage Acceleration and Pulse Dependence of Barrier Breakdown in MgO Based Magnetic Tunnel Junctions**
*S. Van Beek, K. Martens, P. Roussel, G. Donadio, J. Swerts, S. Mertens, A. Thean, G. Kar, A. Furnemont*, G. Groeseneken, KU Leuven, *IMEC*

Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is a promising non-volatile memory for high speed applications. The Magnetic Tunnel Junction (MTJ), the key element, contains a thin crystalline MgO dielectric

sandwiched in between two ferromagnetic layers. One of these magnetic layers retains a magnetic memory state, that can be altered by nanosecond current pulses. The nanometer thin MgO dielectric should show sufficient reliability at used switching voltages. For DRAM applications 1000FIT is required. The lifetime prediction is largely influenced by a voltage acceleration model. For MgO there is no consensus about this acceleration model however. Moreover, large dependencies on pulse width and duty cycle are reported. In this paper we study barrier breakdown time over a range of 11 orders of magnitude. With a maximum likelihood ratio method, we test the statistical significance of fits for different voltage acceleration models on 855 devices. We find that the power law best describes voltage acceleration with a p-value less than 1e-10. In addition we observe no significant influence of duty cycle (1% - 77%) and pulse widths (10ns - 1us) down to 30ns.

**MY-5 A Compact Model for RRAM Including Random Telegraph Noise**

*B.Guan, J. Li*, Sun Yat-sen University, *University of Wisconsin*

Read instability in resistive random access memory (RRAM) devices, mainly caused by random telegraph noise (RTN), needs to be fully addressed before its wide commercial adoption. To fulfill the increasing need for circuit level reliability study, it is desirable to develop a compact model to account for RTN effect. In prior art, several analytical compact models have been developed to simulate resistive switching behavior . However, none of them are capable of capturing current fluctuation caused by RTN. In this paper, we develop a RRAM compact model for circuit simulation, which for the first time takes into account the RTN effect. The model is validated using different sets of experimental data. Our simulation fits well with measurements both in high resistance state (HRS) and low resistance state (LRS).

**MY-6 System-Level Error Correction by Read-Disturb Error Model of 1Xnm TLC NAND Flash Memory for Read-Intensive Enterprise Solid-State Drives (SSDs)**

*Y. Deguchi, T. Tokutomi, K. Takeuchi, Chuo University*

Read-disturb Modeled LDPC (RDM-LDPC) ECC is proposed. Conventional Advanced Error-Prediction LDPC (AEP-LDPC) corrects data-retention errors of data-storage-purpose SSDs storing photos, movies, etc. but cannot correct read-disturb errors. For read-intensive computing-purpose enterprise SSDs, this paper analyzes the read-disturb errors, develops the error model of 1Xnm TLC NAND Flash memory and proposes ECC suitable for read-disturb errors. It is experimentally demonstrated that proposed RDM-LDPC extends the read cycle of SSDs by 5000-times.

**MY-7 On the Variability of Threshold Voltage Window in Gate-Injection Versatile Memories with Sub-60mV/dec Subthreshold Swing and $10^{12}$-Cycling Endurance**

*Y. Chiu, C. Cheng*, M.-H. Lee, C. Liu*, P.-W. Chen*, P.-C. Chen*, C. Chang, S.Yen, C. Fan, H. Hsu, G. Liou*, C. Chang, C. Liu*, W.-C. Chou*, National Chiao Tung University, *National Taiwan Normal University*

Incorporating a charge-trapped ZrSiO with ferroelectric HfZrO dielectrics, we demonstrated a gate-injection versatile memory with sub-60mV/dec subthreshold swing (SS) and large threshold voltage window ($\Delta$VT) of >2V under a fast 20-ns speed. Moreover, it is revealed that the local defects at ZrSiO/HfZrO interface affect the ferroelectric negative capacitance tuning and thus increases the variability of VT and SS during 1E12 cycling endurance.

**MY-8 Random Telegraph Noise in $HfO_x$ Resistive Random Access Memory: from Physics to Compact Modeling**

*F.M. Puglisi, L. Larcher, P. Pavan, University of Modena and Reggio Emilia*

As RRAM technology is entering the industrial phase, compact models accounting for variability and RTN effects at circuit level are essential to evaluate the technology potential. Variability and RTN represent major concerns for HfOx RRAM applications such as non-volatile memory, neuromorphic computing, and Physical Unclonable Function (PUF). In this paper, starting from the physics of charge transport and RTN, we develop a physics-based compact model for RTN in RRAM, valid in both high-(HRS) and low-resistance state (LRS). The proposed model is validated on a wide data set and well reproduces also data from the literature. The RTN model can be easily integrated in compact RRAM device models and can describe I-time traces in both resistive states.

## *Packaging and 3D Assembly*

**PA-1 Optimum Filler Geometry for Suppression of Moisture Diffusion in Molding Compounds**

*W. Ahn, S, Shin, R. Asadpour, L. Nguyen*, D. Varghese*, S. Krishnan*, M. Alam, Purdue University, *Texas Instruments*

Inorganic fillers, such as fused silica or organic clay, help tailor/co-optimize the mechanical toughness, thermal conductivity, and moisture diffusivity of polymer mold compounds used to package microelectronic integrated circuits. Despite long history and wide-spread current use, the optimization of filler-infused composites is generally empirical and therefore time-consuming. A physics-based predictive modeling will improve application-specific design of composites that would offer optimum performance and reliability. As an illustrative example, in this paper, we develop a general theory of polymer composites that anticipates the suppression of moisture diffusion as a function of fill-fraction, size-dispersion, shape, and topology of filler nanoparticles. Our results show that the best performance is obtained by incorporation rod-shaped fillers, randomly closed packed at maximum density (~60%). Our numerical results are succinctly captured by the analytical model based on generalized Maxwell Garnett effective medium theory. The analytical model can be used for initial optimization of mold compounds before large-scale numerical modeling is invoked and characterization experiments are designed.

**PA-2 A Finite Element Method Study of Delamination at the Interface of the TSV Interconnects**

*S. Papaleo, H. Ceric, TU Wien*

Through Silicon Vias (TSVs) are the interconnections in three dimensional integrated circuits responsible for the vertical lines inside the dies. In particular, the open TSV has been developed in order to reduce thermo-mechanical issues. This interconnect structure has interfaces where the possibility of a device failure due to delamination needs to be considered. The Critical Energy Release Rate Gc determines the condition for a fracture to propagate. When the Energy Release Rate G exceeds Gc, a fracture will propagate. Experimental measurements were used to calculate Gc. The experimental Gc, was calculated at the interface between silicon dioxide and tungsten; materials used for Open TSVs. We have developed a model to calculate the G and compared the experimental data with our results. The results obtained are in good agreement with experimental measurements. Therefore, the model developed provides a convenient tool for the study of delamination issues in TSVs.

**PA-3 Electromigration Induced Thermomigration in Microbumps by Thermal Cross-talk Across Neighboring Chip in 2.5D IC**

*M. Li, D.W. Kim*, S. Gu*, K.-N. Tu, University of California, Los Angeles, *Qualcomm*

This paper investigates the thermal cross-talk between the powered microbumps under one chip and the unpowered microbumps under the neighboring chip. Both chips were on a Si interposer for 2.5D IC. The Joule heating from the powered chip was found to be transferred laterally along the interposer to the unpowered chip and produced a temperature gradient in the microbumps in the unpowered chip. Void formation is observed in both the powered and the unpowered microbumps. The latter is due to thermomigration (TM), and the former is due to electromigration (EM). The amount of voids is bigger by TM than by EM. The void nucleation and growing is studied by examining the un-powered microbumps at different stages during electromigration tests. The nucleation of voids at the cold end in TM is observed, which indicates that Sn atoms diffuse from cold end to hot end. The current-enhanced surface electromigration of Sn along the side walls of Cu pillars to form intermetallic compound is observed in the powered microbumps that were subjected to a 5.3×104 A/cm2 current density at 150 ℃ for a period of time. The depletion of Sn will cause serious void formation in these powered microbumps.

## *Process Integration*

**PI-1 Resolution of Poly Gate to Substrate Contact Short Reliability Failures on Non-Volatile Memory**

*S. Chandrasekaran, P. Jowett, T. Mishra, C. Shafer, R. Cruz, K. Noronha, S. Bhosle, V. R. Sanivarapu, N. Rangaraju*, D. Kapoor*, Intel Micron Flash Technologies LLC, *Intel Corporation*

Due to continual scaling of CMOS device dimensions, the dielectric spacing between poly gate (PG) and contact to substrate (Con) has been drastically reduced. This reduction in gate to substrate contact spacing has challenged the dielectric breakdown between poly gate and substrate contact. Several studies involving the breakdown of dielectric between gate and substrate contact have been reported in the past. In this paper, we report the elimination of poly gate to substrate contact shorts on 90 nm Non-Volatile Memory technology with the help of process optimizations in pre-metal dielectric stack. This led to a significant improvement in wafer level reliability metric to the tune of ~1.7X.

**PI-2 Highly-Accelerated WLR Learning Cycles for Development of a Trench MOSFET: Method and Case Study**

*G. Hall, D. Moore, P. Burke, M. Suzuki, ON Semiconductor*

ON Semiconductor Trench MOSFET integration process is designed to be manufacturable with high yields and world-class reliability. Power MOSFET discrete devices are required to pass a number of packaged level reliability (PLR) tests based on IEC guidelines [1], which involve very long time horizons -e.g. High Temperature Gate Bias (HTGB), and Reverse Bias (HTRB) have 1000+ hour time-on-test. When developing a new integration or design, it is of high value to have an expedient methodology for providing fast results on design-of-experiments (DOE), which lead to process or design paths with a high likelihood of passing qualification. In this study we describe the use of WLR methodology to identify an optimized Trench MOSFET gate salicidation scheme. The DOE splits were evaluated using a highly accelerated wafer level bias temperature instability test (WLBTI), and Wafer Level Time Dependent Dielectric Breakdown (WLTDDB). The process conditions which had acceleration factors predicting optimal results at PLR and use conditions were selected for qualification using the standard PLR program. The business case for using WLR methodology to evaluate cycles of learning is clear when one considers the impact to time-to-market of innovative technologies.

## *Product IC Reliability*

**PR-1 Modelling of 1T-NOR Flash Operations for Consumption Optimization and Reliability Investigation**
*J. Coignus, G. Torrente*, A. Vernhet, S. Renard*, D. Roy*, G. Reimbold, CEA, LETI, *STMicroelectronics*

Based on novel experimental capabilities, Flash NOR memory consumption, scalability and reliability trade-off is addressed, by mean of programming and erase operation schemes modelling. A fine tuning of programming energy and max. current is provided, together with an extended description of Flash programming dynamics along device ageing. Optimized cycling conditions are shown to reduce power consumption without any detrimental impact on device reliability.

**PR-2 Near Neighbor Sort Yield & Wafer Sort Yield Impact on Product Burn-In and a Time-Dependent Reliability Study**
*R. Heller, Jr., Advanced Micro Devices*

Local Yield is the yield of near neighbor die to a central die at wafer sort (excluding the results of the central die). It has been shown in literature that the local yield of a die can estimate the future reliability of the die. Die that come from regions of other passing die pose less reliability risks than faulty regions. This is due to defect clustering and the fact that same killer defects that cause sort fails are the same types of defects that cause latent defects only differing in size and location. Based on information we can gather at Wafer Sort, does it make sense to have a "one size fits all" approach for a downstream production burn-in screen? What techniques can we use to better identify potentially unreliable die? Can we use Local Yield and Wafer Sort Yield to better determine burn-in durations? This paper examines all of these questions and the relationship between yield and reliability using both Local Yield and Wafer Sort Yield and production burn-in using a production dataset of AMD CPU. This paper also examines the time-dependent reliability fallout during production burn-in by near neighbor sort bin.

**PR-3 Machine Learning-Based Proactive Data Retention Error Screening in 1Xnm TLC NAND Flash**
*Y. Nakamura, T. Iwasaki, K. Takeuchi, Chuo University*

A screening method to proactively reduce data retention error, based on screening of PD-weak cells, where PD-weak cells have high program disturb error frequency. Repeated measurement of program disturb (P.D.), indicates that 25% of P.D. errors are concentrated in 3.5% of the memory cells, called PD-weak cells. PD-weak cells have 4× worse data retention (D.R.) than non- PD-weak cells, therefore retention errors can be reduced by PD-weak cell screening. Proactive D.R. detection is a new capability, because conventional retention testing times are not practical during product test. In 1Xnm TLC NAND flash, removal of PD-weak cells with <2% overhead extends D.R. by 30%. The method to measure PD-weak cells is described, as well as machine learning to model and detect PD-weak cells. Finally, detection rate vs. false detection cost is compared for 3 learning algorithms.

## *Photovoltaics Reliability*

### PV-1 Study of the Potential-Induced Degradation Kinetics

*J. Bengoechea, M. Ezquer, J. Diaz, A.R. Lagunas, National Renewable Energy Centre*

A dedicated set-up which allows a real-time characterization of the PV modules, while being subjected to the Potential-Induced Degradation (PID) test, was developed and tested. This real-time characterization includes the measurement of the dark I/V curve and the acquisition of electroluminescence (EL) images at different biasing levels. By means of this realtime characterization it is possible to early identify the PID presence and its kinetics during the total duration of the test.This set-up allowed the investigation of the influence of salt as an impurity in module packaging with regard to PID. To this aim, a mini-module contaminated with salt including on the surface of one of its solar cells and in the glass-EVA interface was laminated. This mini-module showed an increased susceptibility to PID, which developed also in the uncontaminated solar cells. Repetitions of the PID test showed that its influence diminished with the number of cycles.

### PV-2 Potential Induced Degradation in High-Efficiency Bifacial Solar Cells

*M. Barbato, M. Meneghini, A. Cester, A. Barbato, G. Tavernaro*, M. Rossetto*, G. Meneghesso, University of Padova, *MegaCell S.r.l.*

This paper presents an analysis of the degradation of Bifacial Solar Cells submitted to potential induced degradation (PID) stress. We report the results obtained on cells with two different encapsulation materials: ethylene-vinyl-acetate (EVA) and polyolefin elastomer (POE). Results show that the use of different encapsulation materials may result in a better robustness towards PID in Bifacial Solar Cells.

### PV-3 Improvement of DSSC Performance by Voltage Stress Application

*A.Scuto, G. Di Marco*, G. Calogero*, I. Citro*, F. Principato**, C. Chiappara**, S. Lombardo,, CNR IMM, *CNR IPCF, ** Università degli Studi di Palermo*

Dye-sensitized solar cells (DSSCs) are promising third generation photovoltaic devices given their potential low cost and high efficiency. Some factors still affect DSSCs performance, such structure of electrodes, electrolyte compositions, nature of the sensitizers, issues of power conversion efficiency and stability under prolonged electrical cycles, etc. In this work we discuss the effect of electrical stresses, which allow to improve DSSC performance. We have investigated the outcomes of forward and reverse DC bias stress as a function of time, voltage, and illumination level in the DSSCs sensitized with the N719, Ruthenium complex based dye. We demonstrate that all the major solar cell parameters, i.e., open circuit voltage (VOC), short circuit current (ISC), series resistance (ROC), fill factor (FF), and power conversion efficiency are strongly influenced by the stress conditions and a clear reversibility of the parameters on the stress type is shown. In this context we examined the possible effects that emerge from the electrolyte composition. Our study suggests that under proper biasing the DSSCs noticeably improve in terms of efficiency and long-term stability.

### PV-4 Adhesion Requirements for Photovoltaic Modules of Polymeric Encapsulation

*J. Zhu, G. Surier, D. Wu, D. Montiel-Chicharro, T. Betts, R. Gottschalg, Longborough University*

This paper addresses the delamination issue and investigates the adhesion requirement and failure of packaging material at the different interfaces. Lamination condition has significant impacts on the adhesion stability and failure modes, which will be further investigated too.

## *Soft Errors*

**SE-1 Alpha-Particle and Neutron-Induced Single-Event Transient Measurements in Subthreshold Circuits**
*M. Gadlage, J. Albhin*, P. Gadfort**, S. Stansberry***, A. Roach, A. Duncan, M. Kay, NSWC Crane, *MDA, **Army Reseach Lab, ***USC-ISI*

Experimental data from alpha particle testing are dis-cussed and analyzed from a sub-threshold voltage SET characterization circuit. Using a Schmitt trigger inverter target chain fabricated in a 28-nm bulk CMOS process, SET pulse widths are captured from an operating voltage down to 0.32 V. These results show that alpha particles can induce SET pulse widths that range up to hundreds of nanoseconds when operating at voltages well below the nominal voltage. Additionally, the alpha particle results show that sub-Vt circuits are significantly more susceptible, as compared to circuits operating at nominal voltages, to low-energy particles inducing SETs that have a high probability of being latched as errors in a combinatorial logic design.

**SE-2 Error Characterization and Mitigation for 16nm MLC NAND Flash Memory under Total Ionizing Dose Effect**
Y. Li, D. Sheldon*, A. Ramos, J. Bruck, California Institute of Technology, *NASA Jet Propulsion Laboratory

This paper investigates the system-level reliability that 16nm MLC NAND flash can offer to SSDs under total ionizing effect for storage in space. Measurements show that blocks that carried less than 3k program/erase cycles (PECs) only survived up to 10k rad total doses under the protection of standard ECCs. We characterize errors at the levels of threshold voltage Vt, cell logical state, and binary bit, respectively, and study error mitigation schemes for reliability enhancement. We adopt a novel data representation where data are read using the relative order of cell voltages.

Experimental results show that the new representation reduced bit errors by 60% on average. We propose a new memory scrubbing (MS) scheme that refreshes cells without block erasure and operates under lower voltage. Measurements show that flash blocks survived up to 8k PECs and 57k rad total doses using the new scrubbing scheme. Both schemes were implemented as parts of a flash controller, and significantly outperform existing methods in various aspects.

**SE-3 Investigating the Single-Event-Transient Sensitivity of 65 nm Clock Trees with Heavy Ion Irradiation and Monte-Carlo Simulation**
*V. Malherbe, G. Gasiot, S. Clerc, F. Abouzeid, J.-L. Autran*, P. Roche, STMicroelectronics, *Aix-Marseille Université*

We present a study of single-event transients in clock tree structures in 65 nm bulk silicon technology. Shift registers are irradiated with heavy ions over a large range of linear energy transfers representative of both terrestrial and space environments. By attributing large error clusters in the flip-flop shifters to clock tree events, we derive experimental cross sections for the clock tree cells. Monte-Carlo irradiation simulations performed on the same structures are in good agreement with these data, allowing to assess the radiation robustness of other clock-tree configurations.

**SE-4 Exploiting Low Power Circuit Topologies for Soft Error Mitigation**
*N. Mahatme, S. Jagannathan, N. Gaspard,III*, B. Bhuva**, S. Wen***, R. Wong***, I. Chatterjee^, T. Assis**, NXP Semiconductor, *Altera Corporation, **Vanderbilt University, ***Cisco, ^University of Bristol*

Alpha particle experimental results for arithmetic circuits implemented using transmission gate logic in 20-nm bulk technology node are shown to have 35% lower soft error rate as well as 30% lower power consumption compared to standard CMOS circuits. Analytical models confirm the experimental trends and help optimize and predict the power-SER trade-off.

**SE-5 Estimation of Single-Event Transient Pulse Characteristics for Predictive Analysis**
*T. Assis, J. Kauppila, B. Bhuva, R. Schrimpf, L. Massengill, R. Wong*, S. Wen*, Vanderbilt University, *Cisco*

Estimate the Single Event Transient (SET) pulse width of standard cells is challenge task requiring hundreds of spice simulations for the library characterization. In this work analytical models are used to estimate the SET pulse width for multiple standard cells considering both different hit node locations and charge sharing. By using the Ambipolar-Diffusion-Cutoff (ADC) model extension this methodology is also able to properly model the SET Pulse Quenching effect. The model requires a simple characterization step performed only once for 3 simple circuits. Comparison with electrical simulations (SPICE) for 4 technologies shows great model accuracy. Heavy ion experiments in a 65nm bulk technology Test Chip also show good accuracy. The simple model formulation and low computational requirements make this methodology ideal to be used by Electronic Design Automation (EDA) tools.

**SE-6 Predicting the Vulnerability of Memories to Muon-Induced SEUs with Low-Energy Proton Tests Informed by Monte-Carlo Simulations**
*J. Trippe, R. Reed, B. Narasimham*, B. Sierawski, R. Weller, R. Austin, L. Massengill, B. Bhuva, K. Warren, Vanderbilt University, *Broadcom Corporation*

Low-energy terrestrial muons have been shown to induce single-event upsets (SEUs) in complementary metal-oxide semiconductor (CMOS) static random access memories (SRAM). Only a handful of facilities produce surface muon beams, and these facilities have limited access to muon beamtime. As a result, it is difficult to carry out experiments to evaluate and/or characterize vulnerability to muons. To address the lack of muon beam availability, this work presents a method for determining a design's vulnerability to muon-induced upsets by performing tests at a readily available, low energy proton facility. It is shown that low-energy protons have similar characteristics as muons for soft error effects. This will allow test engineers to use proton test results to determine if a device is vulnerable to muon induced upsets.

## *Transistor Reliability*

**XT-1 Alteration of Oxide-Trap Switching Activity at Operating Condition By Voltage-Accelerated Stressing**
*Z.Y.Tung, D.S. Ang, Nanyang Technological University*

It is found that voltage-accelerated stressing can change the switching activity of a time-zero oxide defect measured under operating condition. The defect can be rendered either less active or more active by the applied stress, implying a possible modification of its atomic structure. With the impact of oxide trapping on MOSFET channel conduction becoming increasingly important as device dimension decreases, the observed stress-induced alteration of trap-switching behavior under operating condition should be a consideration in the reliability assessment of small-area devices.

**XT-2 Nano-Scale Evidence for the Superior Reliability of SiGe High-k pMOSFETs**
*M. Waltl, A. Grill, G. Rzepa, W. Goes, J. Franco*, B. Kaczer*, J. Mitard*, T. Grasser, TU Wien, *imec*

It has recently been demonstrated that the susceptibility of conventional Si channel pMOSFETs to the negative bias temperature instability (NBTI) is a serious threat to further scaling. One possible solution to this problem is the use of SiGe quantum-well devices, which not only offer high mobilities but also superior NBTI reliability. It has been speculated that the latter is due to the band offset of the SiGe channel with respect to Si, which increases the energetic separation between the defect bands in the high-k gate stack and the channel. We investigate this claim by comparing single-defects in nano-scale devices to the behavior of the large number of defects visible in large-area devices. Using detailed TCAD simulations we determine the energetic and spatial locations of the traps in the gate stack and confirm that the previously developed picture correctly explains the significant reliability benefits of SiGe channel devices.

**XT-3 Negative Bias Temperature Instability Lifetime Prediction: Considering Frequency, Voltage and Activation Energy via Novel Methodology of MSM-SFMF**
*C.H. Chiang, N. Ke, S. N. Kuo, C. J. Wang, K. C. Su, United Microelectronics Corporation*

The reliability of pMOSFETs is limited by NBTI. Recent NBTI studies for aggressive scaling CMOS technology found the recoverable component. According to the present observation, the recoverable component is contributed by hole trapping while the permanent component is explained by the creation of interface. It implies that NBTI results from two tightly coupled mechanisms. This paper discusses a new measuring skill that helps us to realize characteristic of traps via frequency, voltage and temperature [4]. After considering activation energy (Ea), traps can be divided into three types. It includes simple concept of Reaction-Diffusion (RD) and two-stage models, and doesn't need complicated mathematics operations. Consequently, it benefits the study of transistor NBTI behavior.

**XT-4 Device-Level Jitter as a Probe of Ultrafast Traps in High-k MOSFETs**
*D. Veksler, J. Campbell, J. Zhong*, H. Zhu*, C. Zhao*, K. Cheung, National Institute of Standards and Technology, *Chinese Academy of Sciences, *IMECAS*

We developed the methodology to quantify ultra-fast interface traps using jitter measurements as a probe. This methodology was applied to study the effect of PBTI stress in high-k/Si MOSFET on density of fast interface traps (500ps to 5ns timescale). It was shown that increase of jitter of 2Gbt/s signal caused by stress is solely related to the degradation of a FET threshold voltage, while density of fast interface traps is not affected by PBTI stress. The developed methodology can be used for evaluation of the interface quality and quantification of fast interface traps in MOSFET and HEMT devices, built using different technologies and material systems. It can be used to study interface degradation induced by different type of stresses, including electric, thermal, and radiation effects.

**XT-5 Spatio-Temporal Mapping of Device Temperature due to Self-Heating in Sub-22nm Transistors**
*M.A. Wahab, S. Shin, M.A. Alam, Purdue University*

With the increase of transistor density and adoption of novel geometries, such as, FinFET, ETSOI, and gate-all-around (GAA) transistors, self-heating has emerged as a persistent concern for modern ICs. Various reliability issues, such as, NBTI, HCI, PBTI, and TDDB depend sensitively on channel temperature, 〖ΔT〗_C (x,y,z;t), due to self-heating. An accurate spatio-temporal map of channel temperature is essential for Fin-resolved reliability/lifetime of sub-22 nm technology nodes. In this paper, we demonstrate that (i) none of the existing techniques, in isolation, can map the Fin-resolved channel temperature of modern transistors, and (ii) only a collection of orthogonal techniques (multiprobe approach) or novel test structures (material approach), integrated/interpreted through self-consistent electro-thermal simulation, can map the temperature in sufficient detail necessary for reliability prediction.

**XT-6 Surface-Potential-Based Compact Modeling of BTI**

*I.S. Esqueda, H. Barnaby*, University of Southern California, *Arizona State University*

Characterization and modeling of bias temperature instability (BTI) is conventionally based on time-dependent shifts in threshold voltage (*Vth*) resulting from stress and relaxation conditions. Contributions of oxide near-interfacial (i.e., border) and interface traps are not independently captured in these conventional methods. By considering the effects of charge trapping dynamics on MOSFET operation, we present new techniques for characterizing and modeling the contributions of oxide and interface traps. Characterization is based on the rapid response of interface traps to high-frequency measurements of inverse subthreshold slope (*S*), for which slower oxide traps do not contribute, as their occupancy does not change at high frequencies. The modeling approach uses calculations of surface potential ($\psi s$) to describe the distinct contributions of oxide and interface traps on BTI. Combined with capture/emission time maps, this approach describes BTI induced $\Delta S$, and $\Delta Vth$ stress/recovery characteristics.

**XT-7 Width and Layout Dependence of HC and PBTI Induced Degradation in HKMG nMOS Transistors**

*N. Mahapatra*, P. Duhan, V. Rao, Indian Institute of Technology Bombay, *Indian Institute of Technology Gandhinagar*

In this abstract, we have studied the width dependence of HC and PBTI induced degradation in HKMG nMOS transistors. It is clearly shown that the oxygen vacancies play a major role in the long term reliability of the HKMG nMOS transistors and this could be improved by dividing the active into multiple active fingers and by increasing the active-to-active spacing.

**XT-8 Characterization and Modeling of NBTI Permanent and Recoverable Components Variability**

*D. Nouguier, X. Federspiel, G. Ghibaudo*, M. Rafik, D. Roy, STMicroelectronics, *University of Grenoble Alpes*

In this paper we use a statistical analysis of NBTI recoverable and recoverable component measured on Pfet device issued from ST Microelectronics 28nm FDSOI technology. From measurement of NBTI degradation and recovery measured at µs time scale, resulting from AC and DC stress, we performed statistical analysis of the permanent and recoverable components and analyzed it separately. Accordingly, we proposed a Dual Defect Centric Model (DDCM) to account for differences of these two components.

**XT-9 Temperature Sense Effect in HCI Self-heating de convolution - Application to 28nm FDSOI**

*X. Federspiel, G. Torrente, W. Arfaoui, V. Huard, F. Cacho, STMicroelectronics*

Hot carrier injection (HCI) remained a major reliability concern for advanced CMOS nodes due to lateral field increase with device scaling but also due to increase of power dissipation [1,2,3,4]. HCI was reported as a wear-out mechanism that induces interface traps and oxide traps which cause in turn MOS device parameter drift. Parameter drift models were published to take into account lateral field, impact ionization, carrier energy distribution as well as local channel temperature. Recently, the need to deconvolute self-heating from HCI apparent voltage acceleration was pointed out to obtain accurate reliability modeling [5,6,7]. We will show here, that calculating temperature activation as if only depicting defect generation activation is an incomplete description of temperature dependency and that parameter drift temperature sensitivity factor must also be taken into account to correctly model HCI out. In the following, sense effect will refer to sensitivity of MOS parameter drift to temperature for a constant number of defect.

**XT-10 Comparative Experimental Analysis of Time-dependent Variability using a Transistor Test Array**
*M. Simic, A. Subirats*, P. Weckx*, B. Kaczer*, J. Franco*, P. Roussel*, D. Linten*, A. Thean*, G. Groeseneken, G. Gielen, KU Leuven, *IMEC*

As the transistors dimension reach the deca-nanometer scales, time-zero and time-dependent variability, which includes Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI), become a great concern for IC design. Accurate statistical models describing these two variability sources are necessary in order to design reliable circuits and systems. This paper gives insights in the geometry scaling of these variabilities and studies time-dependent variability through three different measurement techniques: the 2-point Measure-Stress-Measure, the Time Dependent Defect Spectroscopy, and the precise IdVg. Advantages and downsides of each technique are discussed.

# THURSDAY MORNING

# April 21, 2016

## *Session 6A - ESD and Latch-up*

Session Co-Chairs: *Dimitri Linten, imec, Teruo Suzuki, Socionext*
Section D

*8:30 a.m.* - Session Introduction

*8:35 a.m.*
**6A.1 FinFET SCR Structure Optimization for High-Speed Serial Links ESD Protection**
*L.-W. Chu, Y.-F. Chang, Y.-T. Su, K.-J. Chen, M.-H. Song, J.-W. Lee, TSMC*

We proposed here is a low capacitance SCR optimized for turn-on speed and parasitic capacitance in FinFET CMOS process. Experimental results indicate that our proposed optimal FinFET SCR structure delivers the best known results among the literatures (140mA/fF). By adopting the structure, a high-speed transceiver for operating at multi Gb/s can be easily realized.

*9:00 a.m.*
**6A.2 Interposer FPGA with Self-protecting ESD Design for Inter-die Interfaces and its CDM Specification**
*J. Karp, M. Hart, M. Fakhruddin, V. Kireev, P. Tan, D. Tsaggaris, M. Rawatt, Xilinx, Inc.*

ESD protection of inter-die interfaces is discussed for the second generation of 20nm interposer FPGA, where ESD elements are optimized to reduce die cost. Self-capacitance is used to estimate the CDM exposure of bare die in the interposer assembly flow. A 50V CDM passing voltage of inter-die interfaces is related to the 200V CDM S20.20-2014 specification.

*9:25 a.m.*
**6A.3 Investigation of Reverse Recovery Effects on the SOA of Integrated High Frequency Power Transistors**

*K. Rajagopal, A. Concannon, P. Hower, F. Farbiz, A. Salman, J. Arch, P. Elo, Texas Instruments*

Switching frequency and switching losses are the dominating factors in power conversion applications. These factors can be controlled at technology development or at IC design with different trade-offs. In this paper we introduce a technique to measure safe operating area (SOA) under high frequency switching conditions - primarily, when the power LDMOS body diode is undergoing reverse-recovery. We show that this new SOA is more conservative than the electrical SOA and defines a diminished boundary for high frequency and high reverse injection operations. With this technique we look at the impact on specific design parameters in commonly used LDMOS topologies in an advanced BCD technology. Furthermore with the help of numerical simulations and careful metrological observations we discuss the phenomena leading to device performance limits useful for IC and device designers. Failure analysis of devices at product level and controlled failures created in standalone devices at wafer-level are examined.

*Break*
*9:50 a.m.*

*10:20 a.m.*
**6A.4 Modeling Feedback Effects in Metal Under ESD Stress**
*T. Maloney, Intel Corporation*

The feedback model of on-chip interconnect metal heating during electrostatic discharge (ESD) is extended to capture and simplify overall behavior of the metal. Of greatest interest to risk assessment is the peak temperature Tmax reached during an ESD event, and it is discovered that Tmax for Human Body and Charged Device Model (HBM, CDM) events follows its own simplified feedback equation with constant parameters. These constants are a function of the electrical and thermal properties of the metal layer. The result is a simple relation between Tmax and current density for the HBM or CDM event under consideration, a valuable aid to risk assessment and design rule checks. The summary equations capture the results of many detailed finite element and numerical convolution calculations of heat flow for on-chip metal.

*10:45 a.m.*
**6A.5 Latchup Holding Voltages and Trigger Currents in a SOI Technology,** *G. Quax, T. Smedes, *NXP Semiconductors*

This paper investigates holding voltages and trigger currents in a Silicon-on-Insulator technology. These parameters can be used in automated layout checks. Via a new measurement method, where the well-bias of the test structures is varied with regard to the bias of the emitters of the thyristor, a strong dependency on the emitter distance, and a weak dependency on the well tap distance is observed. The holding voltages are compared to a low-Ohmic and high-Ohmic variant of the same technology node. Trigger currents of a layout with a variable well tap length are investigated. A model for the effective resistance is developed, incorporating the increased resistance for longer current paths by segmenting the current flow area. The performance of the model and possible applications are discussed.

*11:10 a.m.*
**6A.6 Experimental Study of Supply Voltage Stability during ESD (Late News)**
*Y. Xiu, R. Mertens, N. Thomson, E. Rosenbaum, University of Illinois at Urbana-Champaign*

On-chip power supply integrity may be compromised during a power-on ESD event, e.g. system-level ESD. Experimental data are provided to show that the supply integrity is a function of the rail clamp gain, its speed of response to ESD, and the amount of on-chip supply decoupling capacitance. It is also demonstrated that just a few nH of package inductance can cause the on-chip supply to briefly collapse, regardless of the rail clamp response speed.

## *Session 6B - 3D Assembly*

Session Co-Chairs: *Chandrasekara Kothandaraman, IBM, Kangwook Lee, Tohoku University*
Section E

*8:30 a.m.* - Session Introduction

*8:35 a.m.*
**6B.1 Impact of Local Stress in 3D Stacking Process on Memory Retention Characteristics in Thinned DRAM Chip**
*S. Tanikawa, H. Kino, T. Fukushima, K. Lee, M. Koyanagi, T. Tanaka, Tohoku University*

The influence of local stress on memory retention characteristics has been characterized. The retention time of memory cells in the DRAM chip with 200-µm thick was largely changed after under-fill and curing of epoxy layer especially near and between Cu/Sn bumps. Meanwhile, after thinned down to 40-µm thick, the retention time of memory cell was not significantly changed on the whole even regardless of the positions of Cu/Sn bump. We assumed that the local stress generated by under-fill of epoxy adhesive gave larger effects on the memory retention characteristics than the stress generated by Si thinning until 40-µm-thick.

*9:00 a.m.*
**6B.2 Impact of Wafer Thinning on Front-end Reliability for 3D Integration**
*A. Chasin, M. Scholz, W. Guo, J. Franco, G. Potoms, A. Jourdain, D. Linten, G. Van der Plas, P. Absil, E. Beyne, Imec*

The impact of wafer thinning down to 5 µm Si thickness is assessed in advanced planar and finFET CMOS technologies. Both Bias Temperature Instability (BTI) and Electrostatic Discharge (ESD) reliability are not impacted by the reduction of the substrate thickness.

*9:25 a.m.*
**6B.3 Triangular Voltage Sweep (TVS) Characterisation for Through-Silicon-Via (TSV) Reliability**
*C. Kothandaraman, S. Cohen, IBM Research*

We demonstrate the use of TVS for reliability characterization of TSV. TVS complements conventional methods of dielectric reliability characterization such as VBD and TDDB. TVS is used to study copper diffusion out of the TSV and the impact of TSV process on neighboring devices.

*Break*
*9:50 a.m.*

*10:20 a.m.*
**6B.4 The Projection of the Incidence of Dielectric Cracking During Chip Joining with Lead Free Solder Bumps**
*T. Shaw, E. Misra*, D. Questad*, X. H. Liu, G. Bonilla, T. Wassick*, H. Shobha**, K. Smith*, G. Osborne*, D. Koiussis*, J. Wright*, R. Bisson**, I. Paquin***, M. Lamorey*, S. Bouchard***, S. Tetreault***, D. Stone*, C. Muzzy*, B. Sundolf*, T. Daubenspeck*, IBM T.J. Watson Research Center, *IBM Microelectronics, **IBM at Albany Nano-Technology Center, ***IBM Canada Ltd 23*

This study examines different approaches to determining the chip failure rate that occurs due to dielectric cracking under C4 sites during chip joining. We show that testing of the strength of individual C4s by a single bump shear technique gives a strength distribution that is well described by a Weibull distribution with a Weibull modulus that lies in the range 10-20. Simulations of the spatial distribution of failing C4s during a chip joining test using this distribution, however, are found to be inconsistent with those observed experimentally. From this observation we conclude that the observed fails arise from a defect population that is not well characterized by single bump shear tests. We propose an alternative to SBS testing in which we directly count the number of fails that occur at a given stress level by comparing the location of the fails observed in multiple sonoscan images of chips to the C4 stress map calculated from a finite element model. An example is presented where the strength distribution of the defect tail is characterized from the analysis of C4 fails induced by an accelerated chip joining test. From this distribution we show how it is possible to project chip failure rates that arise from a manufacturing chip joining process.

*10:45 a.m.*
**6B.5 Key Metrics for the Electromigration Performance for Solder and Copper-based Package Interconnects,** *C. Hau-Riege, Y.-W. Yau, K. Caffey, Qualcomm Technologies, Inc.*

This paper presents EM results over a wide spectrum of far backend interconnects, including microbump, thermal compression flip chip bump, copper pillar, lead free bump and solder ball, in order to identify the unifying themes for electromigration failure modes and performance enhancement. In all cases, CuSn is formed in the solder region. For structures with high solder-to-Cu ratios (e.g., solder balls, lead-free bumps, or Cu pillars on narrow traces), failure occurred along the interface of the CuSn and solder on the cathode-side. For structures with low solder-to-Cu ratios (e.g., Cu pillars and TCFC bumps on wide traces or pad, and microbump), solder totally transforms into CuSn during EM test. In this steady-state (or near steady-state) configuration, no further evolution occurs; that is, there are no significant EM voids and the resistance is relatively stable. Based on our studies, the transition between "high" and "low" regimes occurs in the range of solder-to-Cu ratios of 2.5 to 3.

*11:10 a.m.*
**6B.6 The State of Pb-free Solder – A Joint Reliability Overview (Late News)**
*V. Vasudevan, T. Schulz, M. Pei, F. Toth, A.E. Lucero, B. Zhou, S. Mukherjee, Intel Corporation*

Over the past decade the electronics components industry successfully transitioned from the use of leaded solder to lead-free (Pb-free) solders in response to growing environmental health concerns related to heavy metals and other substances. Pbfree components in general are in compliance to meet the European restriction of hazardous substances (RoHS) directives. During the transition period to Pb-free surface mount, numerous issues were raised about the selected alloys, the board assembly process and reliability. Early Pb-free reliability concerns were due to incomplete analytical understanding of the Tin-Silver-Copper solder creep-fatigue behavior, difficulty in computing the magnitude of ball grid array (BGA) relative displacements or strains and lack of product field history. Since then the failure mechanisms were characterized and many models are in common use for reliability estimation and design. This manuscript revisits the initial concerns, reliability model use evolution and summarizes the current understanding that has resulted in a decade of reliable field operation for the Pb-free SAC solders selected.

## *Session 6C – Memory*

Session Co-Chairs: *Robin Degraeve, imec, Christian Monzio Compagnoni, Polytechnico di Milano*
Section F/G

*8:30 a.m.* - Session Introduction

*8:35 a.m.*
**6C.1 Quantitative Model for Post-program Instabilities in Filamentary RRAM**
*R. Degraeve, A. Fantini, G. Gorine*, P. Roussel, S. Clima, M. Chen, B. Govoreanu, L. Goux, D. Linten, M. Jurczak, A. Thean, imec, *University of Pavia*

Filamentary vacancy-based RRAM devices show post-program instability, making Incremental Step Pulse Program (ISPP) algorithms highly ineffective. This is because after the verify step, both the Low and High Resistive State distributions always evolve towards a wider natural distribution. In this paper, we describe this instability in the context of the hourglass model. Both HRS and LRS distributions have two variability sources: (i) number variations of the amount of vacancies in the filament constriction and (ii) constriction shape variations. The shape variations show a log(time)-dependent relaxation behavior after each programming pulse, resulting in program instability. This is mathematically described as an auto-correlated step process of the shape parameters in the QPC conduction model.

*9:00 a.m.*
**6C.2 Extensive Reliability Investigation of a-VMCO Nonfilamentary RRAM: Relaxation, Retention and Key Differences to Filamentary Switching**
*S. Subhechha*, B. Govoreanu, Y. Chen, S. Clima*, K. De Meyer*, J. Van Houdt*, M. Jurczak, imec, *also with KU Leuven*

Vacancy Modulating Conductive Oxide resistive switching devices use electrical modulation of the defect profile to vary the conductance of tunneling barrier, thereby operating with self-rectification and self-compliance. They have been demonstrated to show low switching current with area scalability, indicating non-filamentary switching, and thus making them very promising candidates for high density memory applications. In this work, we report on room temperature and higher temperature retention, with extensive study on parametric dependence – the impact of electrical, material, and process parameters. In addition, we highlight differences with respect to filamentary switching, and suggest directions for improvement.

*9:25 a.m.*
**6C.3 A Step Ahead Toward a New Microscopic Picture for Charge Trapping/detrapping in Flash Memories**
*D. Resnati, C. M. Compagnoni, G. Paolucci*, C. Miccoli*, J. Barber*, M. Bertuccio*, S. Beltrami*, A. Lacaita, A. Spinelli, A. Visconti*, Politecnico di Milano, *Micron Technology Inc.*

Scaling of integrated MOS technologies into the deca-nanomenter regime represented a historic moment for the reliability community, opening the possibility of observing long-debated issues from the new perspective of charge and matter granularity. In the last years, this resulted in a fundamental revision of the physical understanding of Negative Bias Temperature Instability (NBTI) and Random Telegraph Noise (RTN). Following this path, in this work we present clear experimental results leading to a new microscopic picture for charge trapping/detrapping in Flash memories, representing one of the most relevant constraints to the operation of state-of-the-art arrays. The gathered experimental evidence is implemented in a statistical model able to reproduce the charge trapping/detrapping dynamics along the memory array lifetime.

*Break*
*9:50 a.m.*

*10:20 a.m.*
**6C.4 Channel and Near Channel Defects Characterization in Vertical $In_xGa_{1-x}As$ High Mobility Channels for Future 3D NAND Memory**
*A. Subirats, E. Capogreco, R. Degraeve, A. Arreghini, D. Linten, G.Van den bosch, J. Van Houdt, A. Furnemont, imec*

In this paper, we present a first characterization of the charge trapping in vertical 3D SONOS with InxGa1-xAs channel using IV hysteresis and RTN measurements. We show that III-V devices have a high density of border traps leading to an important variability its electrical parameters. Finally, individual trap analysis show that the III-V devices also possess traps in the channel region and their behavior is similar to the one measured in silicon technology.

*10:45 a.m.*
**6C.5 Data-Retention Time Prediction of Long-term Archive SSD with Flexible-nLC NAND Flash**
*T. Takahashi, S. Yamazaki, K. Takeuchi, Chuo University*

This paper proposes a new method to predict the data-retention time of long-term archive SSD with flexible-nLC NAND flash. This paper first reports that the conventional prediction overestimates the data lifetime. Then, a more precise prediction is proposed. By using the proposal, the most reliable and lowest cost memory architecture is determined. As a result, over 100-year data-retention is achieved, which is 25-times longer than the conventional TLC NAND flash memory.

*11:10 a.m.*
**6C.6 Data Archiving in 1x-nm NAND Flash Memories: Enabling Long-Term Storage using Rank Modulation and Scrubbing**
*Y. Li, E. En Gad, A. A. Jiang*, J. Bruck, California Institute of Technology, *Texas A&M University*

Archival data once written are rarely accessed by user, and need to be reliably retained for long periods of time (e.g., 10 ~ 100 years). The challenge of using inexpensive NAND flash to archive cold data was posed recently for saving data center costs. However, high density flash is vulnerable to charge leakage over time, and a recent study shows that flash will be cost-competitive to HD in archival systems if longer retention periods (RPs) can be achieved. This paper investigates the system-level reliability of archival storage that uses the cheapest 1x-nm NAND flash. We analyze retention error behavior, and show that 1x-nm MLC and TLC flash do not immediately qualify for archival storage. We then implement the rank modulation (RM) scheme and memory scrubbing (MS) in flash controller for RP enhancement. RM takes advantage of the asymmetric threshold voltage drift for higher reliability, and provides a new data representation using the relative order of cell voltages. Measurements show that the new representation reduces raw bit error rate (RBER) by 45% on average, and using RM and MS together provides up to 58, 128 and 196 years of RPs at ECC code rates 0.84, 0.82 and 0.80, which outperforms conventional methods by 480%, 49% and 18%, respectively.

## *Session 7A - Dielectric Reliability (Front-end and Back-end)*

Session Co-Chairs: *Ernest Wu, IBM, Bonnie Weir, Avago*
Section D

*1:25 p.m.* - Session Introduction

*1:30 p.m.*
**7A.1 The Physical Mechanism Investigation between HK/IL Gate Stack Breakdown and Time-dependent Oxygen Vacancy Trap Generation in FinFET Devices**
*C.-H. Yang, S.-C. Chen, Y.-S. Tsai, R. Lu, Y.-H. Lee, Taiwan Semiconductor Manufacturing Company*

In this paper, the detailed TDDB models of HK/IL gate stack were well established through the analysis of the oxide trap generation in FinFET technology. We systematically characterized gate oxide traps of HK and IL layers by AC admittance and SILC spectrum methodologies. We found that NMOS TDDB is sensitive to HK traps, while PMOS TDDB is mostly attributed by IL traps and HK deep traps. In addition, the gate oxide deep traps were found to be highly responsible for the permanent damage during stress. Such that, the physical mechanisms of HK/IL gate stack breakdown in FinFET devices can be successfully explained through the scenario of time-dependent HK and IL trap generations. Through the trap studies, TDDB reliability of FinFET technology can be successfully improved.

*1:55 p.m.*
**7A.2 Multiphysics based 3D Percolation Framework Model for Multi-Stage Degradation and Breakdown in High-κ / Interfacial Layer Stacks**
*S. Mei, N. Raghavan, K. Shubhakar, M. Bosman*, K.-L. Pey, Singapore University of Technology and Design, *A*STAR*

Softer stages of dielectric degradation and breakdown deserve in-depth studies given their relevance and finite probability of occurrence in the 14 nm and sub-10 nm CMOS technology nodes of the future. This study presents a multi-physics based percolation framework model to simulate the dynamics of the sequential and competitive evolution of soft breakdown (SBD) spots during degradation of a dual-layer high-κ interfacial layer (HK-IL) dielectric stack. The presented model leverages on the combined use of Kinetic Monte Carlo (KMC) routine to describe the microstructural variations and stochastics of defect nucleation and growth as well as the finite element model (FEM) to quantify the spatio-temporal evolution of the potential, field and temperature distributions in the stack. The results point to IL being the first to breakdown and confirm physical and atomistic evidences that suggest the preferential nucleation of SBD spots beneath the grain boundary regions in the HK layer. Furthermore, our model enables visualization of multiple SBD paths in the IL layer before HK eventually percolates, which supports earlier statistical studies.

*2:20 p.m.*
**7A.3 Layout Dependence of Gate Dielectric TDDB in HKMG FinFET Technology**
*W. Liu, E. Wu*, F. Guarin, C. Griffin, R. Dufresne, D. Badami, M. Shinosky, D. Brochu, GLOBALFOUNDRIES, *IBM TJ Watson Research Center*

In this work, we report for the first time the experimental evidence of layout dependence on gate dielectric time-dependent-dielectric-breakdown TDDB in a leading edge HKMG FinFET technology. Structures with identical total effective gate area but various Fin and finger configurations per unit cell exhibit more than 10X difference in Tbd and Qbd. Fin number per unit cell is the major impact factor based on leakage / stress current comparisons and Fin number scaling conversion. The implication of these findings on technology qualification methodology is that one needs to evaluate layout sensitivity for a given process under development to confirm that reliability assessment are valid for structures with various layout configurations. Processes with strong layout dependence should be optimized before technology qualification.

*2:45 p.m.*

**7A.4 CAFM Based Spectroscopy of Stress-Induced Defects in $HfO_2$ with Experimental Evidence of the Clustering Model and Metastable Vacancy Defect State**

*A. Ranjan, N. Raghavan, K. Shubhakar, R. Thamankar, J. Molina*, S.J. O'Shea*, M. Bosman*, K.L. Pey, Singapore University of Technology and Design, *NIAOE, **A*STAR*

In this study, we perform random telegraph noise (RTN) spectroscopy on ultra-thin HfO2 dielectric films using a conductive atomic force microscope (CAFM), enabling accurate assessment of single or few defect kinetics in very small area regions spanning 40 × 40 nm2. Our characterization results show that bias-dependent RTN trends can be clearly detected at high spatial resolution using the CAFM system. Experimental evidence of the metastable nature of oxygen vacancy defects is presented and the nanoscale BD results provide further support to the time-dependent defect clustering model that is recently proposed for oxide breakdown [1, 2]. Statistics of CAFM breakdown voltage also show a trimodal distribution that corresponds to percolation nucleation at grain (G), grain boundary/triple point (GB/TP) sites and G-GB interfaces.

## *Session 7B - Failure Analysis*

Session Chair: *Abdullah Yassine, AMD*
Section E

*1:25 p.m.* - Session Introduction

*1:30 p.m.*

**7B.1 Spontaneous Photon Emission from 32 nm and 14 nm SOI FETs**

*F. Stellari, A. Ruggeri, A. B. Shehata, H. Ainspan, P. Song, IBM TJ Watson Research Center*

The very faint spontaneous near-infrared photon emission of scaled SOI FETs (32 nm planar and 14 nm FinFET) is characterized and modeled for the first time. Novel higher sensitivity detectors are leveraged to measure emission at low operating voltages including sub-threshold and linear regions that are extremely faint. Furthermore, the effect of device threshold was studied for the first time and a model explaining the data is presented.

*1:55 p.m.*

**7B.2 Dynamical Observation of H-induced Gate Dielectric Degradation through Improved Nuclear Reaction Analysis System**

*Y. Higashi, R. Takaishi, M. Suzuki, Y. Nakasaki, M. Tomita, Y. Mitani, M. Matsumoto*, K. Kato*, S.Ogura*, K. Fukutani*, Toshiba Corporation, *University of Tokyo*

The Nuclear Reaction Analysis (NRA) system was successfully improved in terms of the control of dynamic hydrogen migration and reducing background noise. The proposed new system achieved nondestructive measurements of the hydrogen depth profile with a detection limit of less than 3×1019 atoms/cm3. Secondary Ion Mass Spectrometry and NRA with this system were compared in the analysis of the hydrogen depth profile in gate dielectric for the first time and superiority of NRA was demonstrated. In addition, we successfully demonstrated that dynamic hydrogen migration in gate dielectric is strongly correlated with generation of both bulk defects and interface defects of gate dielectrics.

*2:20 p.m.*

**7B.3 Transient Thermometry and HRTEM Analysis of RRAM Thermal Dynamics during Switching and Failure**

*J. Kwon, A. Sharma, C.-Y. Chen*, A. Fantini*, M. Jurczak*, Y. Picard, J. Bain, M. Skowronski, Carnegie Mellon University, *imec*

We investigate RRAM thermal dynamics during resistive switching and endurance failure by using transient thermometry and HRTEM analysis. The filament size was estimated to ~1 nm with 7-15 nm crystalline region, having experienced local temperatures of > 1600 K at the filament core and > 850 K in the heat affected zone. The devices that underwent cold switching show no change in the HfAlOx microstructure, postprogramming. However, such devices show preferential templated growth of HfAlOx crystallite, extending from the polycrystalline Hf layer after 107 switching cycles, eventually culminating in a RESET failure.

*2:45 p.m.*

**7B.4 NVM Cell Degradation Induced by Femtosecond Laser Backside Irradiation for Reliability Tests**

*V. Della Marca, M. Chambonneau*, S. Souiki-Figuigui**, J. Postel-Pellerin**, P. Canet**, P. Chiquet**, D. Grojo*, F. Yengui^, R. Wacquez^, E. Kussener, J.-M. Portal**, M. Lisart^^, IM2NP-ISEN, CNRS, UMR, *Aix-Marseille Université, CNRS, LP3, **Aix-Marseille Université, IM2NP,CNRS, ^CEA-Tech, ^^STMicroelectronics*

The market of the smart connected objects is growing up driven by the incessant ideas of the new worldwide startuppers and developers. The silicon founders need to find new very reliable and low costs solutions in order to provide high performance electronic circuits for the embedded applications. In this context the nonvolatile memories play a key role for the systems on chip (SoC). In this paper we show for the first time, to our knowledge, the effects of a femtosecond laser beam on a single isolated nonvolatile Flash floating gate memory cell. We show here the possibility to program and damage a memory cell by a contactless injection of free charges. This technique can be used in the failure analysis in-line tests, or after the fabrication as a parametric measurement, improving the investigation time, or to emulate radiative effects on NVM.

## *Session 7C - Product IC Reliability*

Session Co-Chairs: *Jerry Lee, Cisco, Brian Pedersen, Intel*
Section F/G

*1:25 p.m.* - Session Introduction

*1:30 p.m.*

**7C.1 BTI Induced Dispersion: Challenges and Opportunities for SRAM Bit Cell Optimization**

*F. Cacho, A. Cros, X. Federspiel,V. Huard, C.Roma*, STMicroelectronics, *MunEDA*

A One major CMOS reliability concern for advanced nodes is the Bias Temperature Instability (BTI) mechanism. In addition to the native local process dispersion, the BTI induced dispersion is a field under intensive research. Important works [1, 2] focus on the distri-bution tail of the Vth shift and efforts are deployed to high-sigma accurate modeling (defect centric, skellam). In most applications influ-enced by devices matching (ADC, SRAM…), it is important to understand how the initial Vth distribution evolves in time. In this paper some key results of spread induced by BTI are reviewed for 14FDSOI and 28FDSOI from STMicroelectronics. Analysis between initial Vth and aged Vth correlation is presented. Then, measurement of fresh and post HTOL memory VDDmin is presented for different conditions of temperature and process centering. Finally, an innovative algorithm of yield optimization is presented. It enables to optimize the centering and yield (through devices sizing or process centering) including ageing, under constraint of foot print.

*1:55 p.m.*

**7C.2 Aging-aware Adaptive Voltage Scaling of Product Blocks in 28nm Nodes**

*V. Huard, F. Cacho, A. Benhassain, C. Parthasarathy, STMicroelectronics*

In this work, we have demonstrated the fundamental elements towards an Aging-aware AVS scheme of digital circuits. First, we have demonstrated that a new generation of aging monitors, named IS2M, is needed to accurately track the aging-induced delay degrada-tions. In a second time, Aging-aware AVS voltage regulation has been experimentally assessed on two different testcases. Overall, 6-7% power reduction has been demonstrated at the beginning of the life and 2-3% at the end-of-life situation. Even though the regulated voltage increases, most of the power reduction is maintained over the whole mission profile. This study offers new perspectives towards product hardening and qualification with respect to an adaptive approach to real user-based workloads.

*2:20 p.m.*

**7C.3 Scenario-based Set-level HTOL Test (ASH III) for Product Quality and Reliability Qualifications on High-Speed Aps**

*J. Park, J. Kim, M. Choe, H. Shim, W. Kim, S. Park, S. Shin, Y. Kim, J. Jeong, H. Shin, H. Lee, S. Pae, Samsung Electronics Co., Ltd.*

In a streak of the set level stress test for high speed mobile application processor (AP) reliability [1], At-Speed HTOL (ASH) incorporated by user conditions was employed to realistically project the field failure rate of product. Using the worst case scenario test with different frequency and operation duty, the failure modes veiled behind the conventional HTOL can be surfaced and then reconciled, which is further evolved as a failure screening technique during volume production. In addition, the simulation methodology to determine product Vmin-GB in pre-silicon phase is also developed and compared to the Product Vmin-GB results. The results of ASH with scenario test can extend our understanding of an effective methodology to ensure robust design from design for test (DFT) and to achieve decent field failure target.

*2:45 p.m.*

**7C.4 Reliability Characterizations of Display Driver IC on High-k / Metal-Gate Technology**

*D. Kim, J. Kim, K. Bae, H. Kim, L. Hwang, S. Shin, H.-N. Park, I.-T. Ku, S. Pae, J. Park, H. Lee, Samsung Electronics Co., Ltd.*

Display Driver IC is used to operate the display panel of mobile devices, such as handheld smartphones and tablets. Recently, High-k (HK)/ metal-gate (MG) process was used to fabricate DDI products for low power applications. We'll discuss the abnormal leakage increase observed during HTOL and explain the physical mechanism and process fixes implemented. As result, final DDI product showed an excellent reliability results through 1500hrs of HTOL exceeding product EOL.

# IRPS 2016 Poster Sessions

# Compound/Opto Electronics

## Compound/Opto Electronics

### CD-1 On Conduction Mechanisms through SiN/AlGaN based Gate Dielectric and Assessment of Intrinsic Reliability

A. Banerjee, P. Vanmeerbeek, L. De Schepper, S. Vandeweghe, P. Coppens, P. Moens, ON Semiconductor

The first section of this article focuses on the investigations of the gate leakage conduction mechanisms under forward and reverse bias conditions using temperature dependent Jg-Eg characteristics on a Silicon Nitride (SiN)/AlGaN based Metal-Insulator-Semiconductor (MIS) structure. TCAD study under forward bias conduction show majority of the voltage drop on the SiN layer only. The model fitting the electrical characteristics was observed to be Poole- Frenkel (PF) emission. Under reverse bias condition, the entire voltage drop occurs on the entire SiN/AlGaN/GaN. The conduction mechanism responsible for the leakage was found to be Fowler-Nordheim (FN) tunneling along with a thermionic emission component. Second section of this article focuses on the Time Dependent Dielectric Breakdown (TDDB) measurements and lifetime extrapolation of the SiN/AlGaN based di-electric stack. TDDB measurements were done under constant field stress for different temperatures. Normalization of the data exhibited only field accelerated degradation with no influence from the temperature.

### CD-2 Correlation Between Dynamic RDSon Transients and Carbon Related Buffer Traps in AlGaN/GaN HEMTs

F. Iucolano, A. Parisi, S. Reina, A. Patti, S. Coffa, G. Meneghesso*, G. Verzellesi**, F. Fantini**, A. Chini**, STMicroelectronics, *University of Padova, **University of Modena and Reggio Emilia

The on resistance increment observed when the device is operated at high drain-source voltages is one the topics that limits the performance of the AlGaN/GaN HEMT devices. In this paper, the physical mechanisms responsible of the RDSon degradation are investigated. The dynamic RDSon transient method is used in order to get insight to characterize the traps states. By calculating the Arrhenius plot associated with the RDSon transients an activation energy of 0.86eV was extracted, that can be correlated to the traps due to the incorporation of Carbon inside the buffer. This hypothesis was further supported by the analyses performed on a simpler structure (TLM). By applying a negative substrate bias the effect of only the buffer traps was studied. A fairly close value of the

activation energy (0.9eV) to the one extracted when analyzing the RDSon transient was obtained.

**CD-3 Investigation of Trapping Effects on AlGaN/GaN HEMT under DC Accelerated Life Testing**

W. Sun, C. Lee*, P. Saunier*, S. Ringel, A. Arehart, Ohio State University, *Qorvo Inc

GaN-based high electron mobility transistors (HEMTs) were subjected to DC-based accelerated life testing to determine which defect levels form or are activated, and how they impact the static and dynamic HEMT performance. The primary static changes were a negative shift of the threshold voltage and an increase in knee walkout/onresistance. The primary dynamic effect of the stressing appeared in the form of a time-dependent increase in the onresistance, and this was found to correlate to first order with formation and/or activation of traps at EC-0.57 and EC-0.72 eV traps that contributed to the dynamic changes, and the EC-1.5 eV trap was likely responsible for the static change in onresistance. Trapping kinetics analysis revealed that the physical sources for the EC-0.57 and EC-0.72 eV states are not simple, ideal, non-interacting point defects, but instead are associated with physically extended defects, such as dislocations, and/or defect complexes.

**CD-4 Evaluations of Threshold Voltage Stability on COTS SiC DMOSFETs Using Fast Measurements**

D. Habersat, R. Green, A. Lelis, US Army Research Laboratory

Threshold voltage (VT) stability of commercial SiC DMOSFETs during bias-temperature stressing was evaluated using the fast-ID and fast ID-VGS measurement techniques at both room and elevated temperatures. Unipolar bias stress results confirmed that there is a rapid recovery of VT and that all vendors' devices showed the same basic charge-trapping behavior, although some differences were observed in negative bias response at high temperatures. In situ VT measurements during 10 kHz gate switching showed stable device operation at room temperature but accelerating VT drift and increasing switching oxide trap densities when operated at 175 °C. VT hysteresis during high temperature gate switching indicates the presence of a mobile ion or polarization effect in addition to the expected interface- and oxide-trap charging mechanisms.

**CD-5 Device Breakdown Optimization of Al2O3/GaN MISFETs**

X. Kang, S. Yamazaki, K. Takeuchi, Chuo University

In this paper we demonstrate a solution to achieve robust enhancement-mode Al2O3/GaN MISFETs with a high breakdown voltage and suggest a possible model for the device off-state breakdown. It is found that the device breakdown exhibits different gate voltage dependence for different surface treatments before the gate dielectric deposition. The device performance is greatly improved by using an in-situ surface plasma treatment. The improved device performance is explained by a reduction of traps at the Al2O3/GaN

interface, which finally leads to a reduction in the amount of trapped positive charges and associated with that a reduction of the effective electric field across the gate dielectric when the device isin off-state. Several experimental results support this hypothesis: (1) The recoverable negative threshold voltage shift after reverse gate bias depends on the interface clean before gate dielectric deposition, (2) The reverse bias gate dielectric breakdown voltage is improved by this interface plasma treatment, although the forward bias gate dielectric breakdown voltage is identical.

# Design for Circuit Reliability

## Design for Circuit Reliability

### CR-1 The Impact of Process Variation and Stochastic Aging in Nanoscale VLSI

S. Kiamerh, P. Weckx*, M. Tehoori, B. Kaczer*, H. Kukner*, P. Raghavan*, G. Groeseneken**, F. Catthoor*, Karlsruhe Institute of Technology, *IMEC, **KU Leuven

With the down-scaling of CMOS technology into deep nano-scale era, negative-bias temperature instability (NBTI) effect becomes stochastic due to its widely distributed defect parameters. As a result, the delay degradation due to intrinsic variability of NBTI becomes also stochastic and the matter is aggravated when it is combined with process variation (PV). Accurate stochastic timing analysis of the circuit becomes very important in this case since over and under margining can lead to significant performance or yield loss (timing failure), respectively. This paper proposes a scalable flow and investigates the combined effect of stochastic NBTI and process variation on the performance of the VLSI design at the circuit level in a 7 nm FinFET technology node by abstracting atomistic NBTI models (for the stochastic behavior) to the circuit timing analysis flow.

### CR-2 Mismatch Circuit Aging Modeling and Simulations for Robust Product Design and Pre-/Post-Silicon Verification

H. Shim, Y. Kim, J. Jeon, Y. Cho, J. Park, S. Pae, H. Lee, Samsung Electronics

As technology scales down, PMOS NBTI-induced mismatch, in addition to the NBTI mean-shifts and time0-Vt variation, is critical for designing circuitry having matched pair transistors, such as OP amplifier. This paper covers mismatch aging models incorporated into design simulation tool for PMIC products and used the Monte-Carlo simulation to consider process and systematic variations for robust design. Circuit simulation for PMIC OP Amp and its output characteristics were investigated and then further validated through the post-silicon HTOL stress. The pre-silicon simulation further enables to optimize HTOL stress conditions.

### CR-3 Aging of IO Overdrive Circuit in FinFET Technology and Strategy for Design Optimization

S.-E. Liu, M.-H. Yu, Y.-J. Chen, J.-Y. Jao, M.-Z. Lin, Y.-H. Fang, M.-J. Lin, MediaTek

We investigated aging property of FinFET-based I/O overdrive circuits (IP) and proposed design strategies of optimization among performance/area/reliability. Aging behavior of I/O overdrive IP with 16nm FinFET process has been extracted and compared with 20nm planar-transistor process. Both pulldown and pull-up driving degradation are worse in the FinFET than planar IP. An aging simulation framework was built from transistor-level aging databases and further calibrated by an empirical equation and IP-level measurements. Finally, a design guideline was discussed and proposed to pursue balance of performance/ area/reliability, which is thus improved 13%/8%/37% respectively in our optimized design.

**CR-4 Robustness of Timing in-situ Monitors for AVS Management**

A. Benhassain, F. Cacho, V. Huard, S. Mhira, L. Anghel*, C. Parthasarathy, A. Jain, A. Sivadasan, STMicroelectronics, *Grenoble University

This paper deals with the fundamental aspects of the introduction of aging sensor in digital circuit, describing a new In-situ Timing Monitor (ISM), insertion flow and experimental results .

# Dielectric Reliability (Front-end and Back-end)

## Dielectric Reliability (Front-end and Back-end)

**DI-1 Moisture Impact on Dielectric Reliability in Low-k Dielectric Materials**

K.-D. Lee, Q. Yuan, A. Patel, Z. Mai, L. Brown, S. English, Samsung Austin Semiconductor

With intentional moisture uptake and removal, we modulate the moisture level in porous low-k dielectric materials, and investigate the moisture impact on dielectric reliability at a wide range of stress conditions. From this study, we confirm moisture can cause a significant degradation in dielectric reliability (i.e., x1.0E-06 in TDDB lifetimes) . Interestingly, the moisture impact is not permanent (with good Cu-diffusion barrier) and can be restored effectively with a high temp annealing at ≥ 350°C. Different from previous studies, moisture does not always increase the leakage currents nor change the TDDB modeling parameters, indicating there are at least two moisture states in porous low-k dielectric materials. In this paper, we will discuss the moisture-induced reliability degradation mechanisms.

**DI-2 Impact of Trap Creation at SiO2/Poly-Si Interface on Ultra-thin SiO2 Reliability**

Y. Mitani, M. Suzuki, Y. Higashi, R. Takaishi, Toshiba Corporation

The relationship between TDDB characteristics of the devices having ultrathin SiO2 as gate dielectrics and the hydrogen-related trap creation have been re-investigated from the viewpoint of the oxidation process dependence. In order to study the influence of hydrogen on the reliability, deuterium isotope effect has been used. As a result, the Weibull distributions of time-to-breakdown (tBD) depends on the oxidation process condition even under the same oxidation temperature. Trap creation at gate oxide interface strongly correlates to the dielectric breakdown in ultra-thin gate oxides However, this oxidation process dependence could not be explained only by the amount of hydrogen release from SiO2/Si substrate interface From the experimental results of low-voltage SILC, it can be concluded that not only the released hydrogen from SiO2/Si substrate interface but also those from Poly-Si/SiO2 interface correlates to the breakdown mechanisms.

**DI-3 A Fast Reliability Screening Technique for Identification of Trap Generation**

K. Joshi, Z.-R. Xiao, S.-H. Gao, C. Huang, T.-M. Shen, P.J. Liao, Y.-H. Lee, J-R. Shih, Taiwan Semiconductor Manufacturing Company

SILC spectrum technique is used to identify trap generation location in both PMOSFETs and NMOSFETs under BTI stress. It is validated using SILC spectrum technique that BTI stress in PMOSFETs leads to trap generation in IL/HK intermix whereas in NMOSFETs leads to trap generation in HK layer. Atomistic simulations are further performed to calculate formation energy for oxygen vacancies in various gate oxide layers. It has been validated that it is easy to generate hole traps in IL/HK intermix region under NBTI stress in PMOSFETs and easy to generate electron traps in HK layer in NMOSFETs under PBTI stress. The advantage of this technique is its ease of use and higher throughput thus making it an ideal tool for a quick scanning of trap generation locations and to understand the reliability strength of each layer under different processing conditions.

**DI-4 Correlation between the Variation in the Initial Current at Stress and the Variation in the Failure Time During TDDB Testing of BEOL Structures**

R. Filippi, C. Christiansen, A. Kim*, B. Li*, P-C. Wang, Globalfoundires, *IBM

A novel approach for estimating variation in the TDDB failure time is reported. The results for various test structures reveal that variation in the initial current at stress reasonably predicts variation in the TDDB failure time. The approach is a non-destructive method that only requires a current measurement, making it an efficient monitor of the expected TDDB lifetime behavior during manufacturing of an established process.

**DI-5 Towards an Appropriate Accelerate Model for BEOL TDDB**

R. Muralidhar, E. Linger, T. Shaw**, A. Kim, G. Bonilla*, IBM TJ Watson Research Center

We have evaluated the veracity of BEOL acceleration models using the largest set of data spanning 3 pitches. The raw data indicates same acceleration trends in the 3 pitches enabling them to fall into a universal curve by re-normalization to account for different areas. While the Root-E (RE), Impact Damage and Power-Law (PL) models fit data over entire range well, it is seen that only the Impact Damage and Power Law models predict the low field data when high field data alone is used to fit the models. This ability to extrapolate and the constancy of acceleration factors at low and high fields makes these models more appropriate for determining lifetime at operating conditions from a fit of high field data alone. While the ID model has 3 parameters and presents fitting challenges, the PL model is a good practical alternative and may have its physical basis on arguments based on scaling theory. The paper will additionally discuss in detail statistical analysis including clustering model, fitting aspects of ID model and physical basis of the power-law model from scaling point of view.

**DI-6 Evaluation of Inter and Intra Level TDDB of Cu/Low-k Interconnect for High Voltage Application**

M. Lin, C. Yang, H.-Y. Chen, A. Juan, K.C. Su, United Microelectronics Corp.

The conduction current and TDDB of intra and two kinds of inter level low-k dielectric structures for high voltage application are studied. Electrical field distributions are different on the different structures and impact the TDDB results. Failure analysis shows the Cu ion diffusion and SiCN interface are the dominant impact factor of the low-k dielectric breakdown. An inter level layout design principle to improve dielectric reliability under high voltage operation is suggested.

**DI-7 Effect of H2O on TDDB for a Range of ULK ILD Materials with Varying Damage Resistance for Robust and Weak Liners**

E. Linger, R. Laibowitz*, T. Shaw, S. Cohen, A. Raja*, IBM TJ Watson Research Center, *Columbia University

In this study we look at the correlation between TDDB lifetime, in the presence of intentionally introduced H2O and top surface damage for different ILD materials using a robust liner. The activation energy for the movement of loosely bound physi-adsorbed H2O has been obtained using AC loss measurements. We also explore the role of moisture in drawing Cu out of metal lines through an intentionally fabricated thin/weak liner under prolonged stress at a relatively low voltage. AC loss, I-V, triangular voltage sweep (TVS) and TDDB measurements all provide evidence that Cu is migrating out of the lines into the ILD.

**DI-8 Reliability-Performance Trade-off For Work- Function Optimization In Advanced Node Replacement Metal Gate Technology**

R. Ranjan, T. Nigam, B. Parameshwaran, Y. Liu, S.F. Yap, Globalfoundries

In this work, we explore the complex interaction of the gate stack process and time-dependent-dielectric breakdown (TDDB) in high-K (HK) replacement metal gate (RMG) technology. TDDB is a key reliability metric governing the product lifetimes under long-term operation. Based on this study, it is observed that TDDB is greatly modulated by the proximity of Al to the MG/HK interface. The key parameter modulated by gate stack optimization is voltage acceleration exponent (VAE) for TDDB. All observations indicate higher VAEs can be achieved by keeping the Al away from the MG/HK interface.

# ESD and Latch-up

## ESD and Latch-up

### EL-1 ESD Self-Protection Design on 2.4-GHz T/R Switch for RF Application in CMOS Process

C.-Y.Lin, R.-H. Liu*, M.-D. Ker*, National Taiwan Normal University, *National Chiao Tung University

The RF transceiver front-end for 2.4-GHz applications realized by a fully integrated T/R switch with ESD self-protection capability is presented in this work. Experimental results show that the proposed design can provide enough ESD self-protection capability with good RF performances.

### EL-2 Failure Mechanism of High-Voltage Isolated Lateral Diffused NMOS under High-Current Events

C.-H. Wu, J.-H. Lee*, C.-H. Lien, National Tsing Hua University, *Globalfoundries

In this study, the mechanism of the effect of a high-voltage (HV) NWell guardring (NW-GR) on the electrostatic discharge (ESD) robustness of the HV isolated lateral diffused NMOS (HV ISO-LDNMOS) is investigated. The device fails on low-voltage ESD zapping events when the HVNW-GR is connected to the drain, whereas the device passes these events once it is floated.

### EL-3 Optimization of PESD Implant Design for ESD Robustness of 5V Drain-Back N-LDMOSFET

C. Chiang, P.C. Chang, P.-S. Tseng, P.-Y. Lai, H. Tang, K.C. Su, UMC

An N-LDMOS ESD protection device with drain back and PESD optimization design is proposed. With PESD layer enclosing the N+ drain region, a parasitic SCR is created to achieve high ESD level. When PESD is close to gate, the turn-on efficiency can be further improved (Vt1: 11.2V reduced to 7.2V) by the punch-through path from N+/PESD to PW. The proposed ESD N-LDMOS can sustain over 8KV HBM with low trigger behavior.

**EL-4 On-Chip Protection in Precision Integrated Circuits Operating at High Voltage and High Temperature**

J. Salcedo, J.-J. Hajjar, J. Zhao, Analog Devices

A new high voltage swing bipolar ESD (electrostatic discharge) protection device for enabling low leakage precision mixed-signal interface circuits (ICs) operating at high voltage (~ 40V to 60V) and high temperature (~125°C to 200°C) is presented. Under these operating conditions, parasitic structures in junction-isolated high voltage process technologies induce unexpected shift in the leakage current over time, leading to malfunction in the precision high voltage input/output interface circuit. A proposed device design addresses the low leakage targets at the mentioned operating conditions, while achieving the required ESD robustness of the high voltage interface for industrial applications.

**EL-5 Improving the Long Pulse Width Failure Current of NPN in BiCMOS Technology**

Y. Xiu, A. Appaswamy, Z. Chen*, A. Salman, M. Dissegna, G. Boselli, E. Rosenbaum*, Texas Instruments, *University of Illinois at Urbana-Champaign

The pulse width dependency of the failure current for NPN structures in a 0.18-µm BiCMOS technology is studied using measurements and TCAD simulation. The desired "Wunsch-Bell" behavior is not observed due to formation of current filaments in this device; however, the failure current for long pulse widths can be increased by layout changes.

**EL-6 Analysis of ESD Effects on Organic Thin-Film-Transistors by Means of TLP Technique**

N. Wrachien, M. Barbato, A. Cester, A. Rizzo, G. Meneghesso, R. D'Alpaos*, G. Turatti*, G. Generali*, M. Muccini**, University of Padova, *ETC srl, **CNR-ISMN

We analyzed the effects of Electrostatic Discharge events on large area high voltage Organic Thin Film Transistors, using the transmission line pulsing technique. These transistors survived ESD events exceeding 500V. A partial dielectric breakdown occurred at voltage higher tan 600V. Small mobility and threshold voltage variations are observed, prior breakdown.

**EL-7 Unique ESD Behavior and Failure Modes of AlGaN/GaN HEMTs**

B. Shankar, M. Shrivastava, Indian Institute of Science

Present experimental study reports various failure modes under ESD stress conditions and distinct ESD behavior of AlGaN/GaN HEMTs for the first time. Effect of MESA isolation and gate finger on the ESD behavior of HEMTs is analyzed. Effect of pulse width on ESD robustness and trigger voltage is observed and a unique power law like behavior is found. Cumulative nature of device degradation under ESD stress condition is discovered.

Correlation between depth of snapback and failure threshold with % device degradation is found. Finally, impact of inverse piezoelectric effect in AlGaN/GaN system, fringing electric field, role of contact resistivity, temperature and field induced contact metal migration and premature breakdown of parasitic MESA Schottky junction are studied in context to AlGaN/GaN HEMT failure ESD conditions.

**EL-8 New Insights on the ESD Behavior and Failure Mechanism of Multi Wall CNTs**

A. Mishra, M. Shrivastava, Indian Institute of Science

ESD conditions, through inner and outer shells of MWCNT is explored. ESD time scale current annealing behavior of outer and inner shells was discovered, which is unique to MWCNTs. Shells – by – shell failure was confirmed to be the universal failure mode of MWCNTs. Failure behaviors of suspended and collapsed (tubes resting on dielectric surface) tubes in single and bundled configuration are discussed.

# System Reliability

## System Reliability

**ES-1 Long-Term Reliability of a Hard-Switched Boost Power Processing Unit utilizing SiC Power MOSFETs**

S. Ikpe, J.-M. Lauenstein, G. Carr*, D. Hunter*, L. Ludwig, W. Wood, C. Iannello, L. Del Castillo*, F. Fitzpatrick, M. Mojarradi, Y. Chen, NASA, *Jet Propulsion Laboratory California Institute of Technology

With the expedient maturation of Silicon-Carbide (SiC) device technology, a great deal of interest has been generated in the development of switching power applications capable of harnessing the inherent wide-bandgap (WBG) properties of the material. SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) in particular, offer significant benefit over their Silicon counterparts. The potential for lower total switching losses, higher breakdown field tolerance and superior thermal performance make SiC devices highly attractive for both high temperature and extreme environment applications. Though successful power conversion implementations show promise [1], these noteworthy device innovations have yet to directly translate into pragmatic power conversion systems. Therefore, it is still necessary to evaluate the application-specific performance of these devices to fully understand thermal limitations as well as estimate the overall device reliability. This paper describes a design-for-reliability approach for an innovative power processing architecture intended for in-space solar electric propulsion (SEP) systems. The work herein also presents reliability data on CREE's commercially available N-channel enhancement mode SiC MOSFETs.

# Failure Analysis

## Failure Analysis

### FA-1 Dynamic Avalanche in Charge-Compensation MOSFETs Analyzed with the Novel Single Pulse EMMI-TLP Method

T. Chirila, T. Reimann*, M. Rüb, University of Applied Science Jena, *Technische Universität Ilmenau

As a main switch in a broad range of applications, the Charge-Compensation MOS Transistor must be able to withstand the avalanche multiplication regime. Using the classical rating method for avalanche robustness, two destruction limits have been identified – thermal and current limit. However, up to date there is no complete understanding of current induced failure mechanisms. In this paper we combine single transmission line pulses with emission microscopy in order to bring more insight into these kinds of destruction modes. We identify three different avalanche regimes and observe the occurrence of current filaments. We provide an interpretation for filament formation.

### FA-2 Fast 3D Electro-Optical Frequency Mapping and Probing in Frequency Domain

K. Melendez*, K. Sanchez*, P. Perdu*, K. Melendez, D. Lewis, Bordeaux University, *CNES

The main goal of this paper is to show the capability of extracting several frequencies at one electro-optical scanning
in order to reconstruct few 512 by 5 12 pixels images. With these 3D data (X and Y are pixels and Z is the frequency locked), it is possible to study several frequencies in one time and to reconstruct the original signal waveform at each pixel.

### FA-3 Direct Photo Emission Monitoring for High Power IGBT during Avalanche Operation

T. Matsudai, K. Endo, T. Ogura, T. Matsumoto*, K. Uchiyama*, K. Koshikawa*, Toshiba Corporation, *Hamamatsu Photonics K.K.

IGBTs have been developed extensively to improve trade-off relation between on state losses and switching losses. Therefore the reliability enhancement of IGBTs is very important technology. For the past failure analyses, only the final destruction point have been observed under testing. With this way, it is difficult to perform physical analysis, because the process of the destruction phenomenon is unknown. In this work, our target is investigating the avalanche phenomenon of IGBTs, directly. During avalanche operation, it is well known that the formation of current filament appears and visible light is emitted in the device. For the first time, we have succeeded observing the photo emission directly

from avalanche phenomena under UIS (Unclamped Inductive Switching) condition of IGBTs using the streak camera. We have also measured moving the emission region in edge termination area.

# Interconnect Metallization Reliability

## Interconnect Metallization Reliability

### IT-1 Optimizing Cu Barrier Thickness for Interconnects Performance, Reliability and Yield

T. Shen, B. Rajagopalan, M.C. Silvestre, E. Ramanathan, A.S Mahalingham, W. Zhang, K.B. Yeap, P. Justison, Globalfoundries

Cu barrier thickness optimization on our 90nm pitch Vx/Mx layers with porous ULK SiCOH (κ=2.55) was systematically investigated. Both via resistance and intrinsic EM performance favors thinner TaN and Ta films, however, the robustness of the plating requires thicker Ta to improve seed quality that withstand dissolution during plating. Overall, a thin TaN barrier with moderate thick Ta provides the optimum solution for performance, reliability and yield.

### IT-2 Semi-empirical Interconnect Resistance Model for Advanced Technology Nodes: A Model Apt for Materials Selection Based upon Test Line Resistance Measurements

P. Roussel, I. Ciofi, R. Degraeve, V. Vega, N. Jourdan, R. Baert, D. Linten, J. Bömmels, Z. Tőkei, G. Groeseneken*, A. Thean, IMEC, *KU Leuven

As the dimensions of interconnects shrink into the nanoscale for the NX node, their electrical conductivity becomes dependent on their size, even at room temperature. This paper presents a semi-empirical interconnect resistance model apt for fitting wire resistance data. The model combines grain boundary and sidewall scattering effects with the impact of Line Edge Roughness (LER). It allows subsequent selection of interconnect metallization material candidates through extrapolation to target widths of future technology nodes on the basis of their wire resistance, while still considering other performance metrics like yield, electromigration and TDDB. A refined model parameter calibration procedure, that accounts for interconnect height and width variability between the test structures is demonstrated for two Cu metallization schemes, employing Co and Ru as a metal liner, respectively. The model allows inclusion of more accurate, geometry dependent interconnect resistance estimators in higher abstraction level simulators, enabling a more realistic assessment of the impact of BEOL parasitics on circuit delay at advanced technology nodes.

### IT-3 Electromigration: Multiphysics Model and Experimental Calibration

G. Marti, W.H. Zisser, L. Arnaud*, Y. Wouters**, STMicroelectronics, *CEA-Leti Minatec, **SIMAP, ***Technische Universität Wien

Electromigration (EM) is one of the main reliability failure mechanism of integrated circuit interconnects. The result of EM in copper interconnects is void nucleation and growth close to the cathode. For EM tests, most commonly elementary structures are stressed under accelerated conditions (high current and temperature) until degradation occurs. The understanding of the main mechanism governing the reliability of copper interconnects is mandatory to develop lifetime predictive laws and allows architecture optimizations of future MOS technologies. Thus more accurate and less pessimistic full-chip EM assessment and mean-time-to-failure (MTTF) prediction will require a development of new methods that deal with the design of the grid structure and take redundancy into account. We describe in this work a new methodology to calibrate an existing EM numerical model. The effective charge (Z*) of this technology has been extracted experimentally. Furthermore, the proposed post-processing method allowed us to find the critical tensile stress of void nucleation. This method allows to answer design requests about void nucleation which may depend upon geometry and process conditions. Taking into account these parameters will increase the accuracy of reliability prediction at design level and help designers with high current density needs.

# Memory

## Memory

### MY-1 The Complete Time/Temperature Dependence of I-V drift in PCM Devices

M. Le Gallo, A. Sebastian, D. Krebs, M. Stanisavljevic, E. Eleftheriou, IBM Research – Zurich

Phase-change memory (PCM) devices are expected to play a key role in future computing systems as both memory and computing elements. Hence, a comprehensive understanding of the change in the current/voltage (I-V) characteristics of these devices with time and temperature is of considerable importance. Here, we present a unified drift model to predict the I-V characteristics at any instance in time and at any temperature. The model was validated on large sets of experimental data for an extensive range of time (10 orders of magnitude) and temperatures (180 – 400 K), different phase-change materials and a collection of 4k cells from a PCM chip.

### MY-2 Reliability-Performance Tradeoff between 2.5D and 3D-Stacked DRAM Processors

S.M Hassan, W. Song, S. Mukopadhyay, S. Yalamanchili, Georgia Institute of Technology

MY-3 Root cause of degradation in novel HfO2-based Ferroelectric Memories M. Pešić, F. Fengler, S. Slesazeck, U. Schröder, T. Mikolajick, L. Larcher*, A. Padovani*, NaMLab gGmbH,

*University of Modena and Reggio Emilia Summary:HfO2-based ferroelectrics reveal full scalability and CMOS integrability compared to perovskite-based ferroelectrics that are currently used in non-volatile ferroelectric random access memories (FeRAMs). Up to now, the mechanisms responsible for the decrease of the memory window have not been revealed. Thus, the main scope of this study is an identification of the root cause for the endurance degradation. Utilizing trap density spectroscopy for examining defect evolution with cycling of the device studied together with modeling of the degradation resulted in an understanding of the main mechanisms responsible for degradation of the ferroelectric behavior.

**MY- 3 Root Cause of Degradation in Novel HfO2-based Ferroelectric Memories**

Milan Pešić, Franz P. G. Fengler, Stefan Slesazeck, Uwe Schroeder, Thomas Mikolajick*
NaMLab gGmbH

HfO2-based ferroelectrics reveal full scalability and CMOS integratability compared to perovskite-based ferroelectrics that are currently used in non-volatile ferroelectric random access memories (FeRAMs). Up to now, the mechanisms responsible for the decrease of the memory window have not been revealed. Thus, the main scope of this study is an identification of the root causes for the endurance degradation. Utilizing trap density spectroscopy for examining defect evolution with cycling of the device studied together with modeling of the degradation resulted in an understanding of the main mechanisms responsible for degradation of the ferroelectric behavior.

**MY- 4 Voltage Acceleration and Pulse Dependence of Barrier Breakdown in MgO Based Magnetic Tunnel Junctions**

S. Van Beek, K. Martens, P. Roussel, G. Donadio, J. Swerts, S. Mertens, A. Thean, G. Kar, A. Furnemont*, G. Groeseneken, KU Leuven, *IMEC

Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is a promising non-volatile memory for high speed applications. The Magnetic Tunnel Junction (MTJ), the key element, contains a thin crystalline MgO dielectric
sandwiched in between two ferromagnetic layers. One of these magnetic layers retains a magnetic memory state, that can be altered by nanosecond current pulses. The nanometer thin MgO dielectric should show sufficient reliability at used switching voltages. For DRAM applications 1000FIT is required. The lifetime prediction is largely influenced by a voltage acceleration model. For MgO there is no consensus about this acceleration model however. Moreover, large dependencies on pulse width and duty cycle are reported. In this paper we study barrier breakdown time over a range of 11 orders of magnitude. With a maximum likelihood ratio method, we test the statistical significance of fits for different voltage acceleration models on 855 devices. We find that the power law best describes voltage acceleration with a p-value less than 1e-10. In addition we observe no significant influence of duty cycle (1% – 77%) and pulse widths (10ns – 1us) down to 30ns.

**MY-5 A Compact Model for RRAM Including Random Telegraph Noise**

B.Guan, J. Li*, Sun Yat-sen University, *University of Wisconsin

Read instability in resistive random access memory (RRAM) devices, mainly caused by random telegraph noise (RTN), needs to be fully addressed before its wide commercial adoption. To fulfill the increasing need for circuit level reliability study, it is desirable to develop a compact model to account for RTN effect. In prior art, several analytical compact models have been developed to simulate resistive switching behavior . However, none of them are capable of capturing current fluctuation caused by RTN. In this paper, we develop a RRAM compact model for circuit simulation, which for the first time takes into account the RTN effect. The model is validated using different sets of experimental data. Our simulation fits well with measurements both in high resistance state (HRS) and low resistance state (LRS).

**MY-6 System-Level Error Correction by Read-Disturb Error Model of 1Xnm TLC NAND Flash Memory for Read-Intensive Enterprise Solid-State Drives (SSDs)**

Y. Deguchi, T. Tokutomi, K. Takeuchi, Chuo University

Read-disturb Modeled LDPC (RDM-LDPC) ECC is proposed. Conventional Advanced Error-Prediction LDPC (AEP-LDPC) corrects data-retention errors of data-storage-purpose SSDs storing photos, movies, etc. but cannot correct read-disturb errors. For read-intensive computing-purpose enterprise SSDs, this paper analyzes the read-disturb errors, develops the error model of 1Xnm TLC NAND Flash memory and proposes ECC suitable for read-disturb errors. It is experimentally demonstrated that proposed RDM-LDPC extends the read cycle of SSDs by 5000-times.

**MY-7 On the Variability of Threshold Voltage Window in Gate-Injection Versatile Memories with Sub-60mV/dec Subthreshold Swing and 1012-Cycling Endurance**

Y. Chiu, C. Cheng*, M.-H. Lee, C. Liu*, P.-W. Chen*, P.-C. Chen*, C. Chang, S.Yen, C. Fan, H. Hsu, G. Liou*, C. Chang, C. Liu*, W.-C. Chou*, National Chiao Tung University, *National Taiwan Normal University

Incorporating a charge-trapped ZrSiO with ferroelectric HfZrO dielectrics, we demonstrated a gate-injection versatile memory with sub-60mV/dec subthreshold swing (SS) and large threshold voltage window (ΔVT) of >2V under a fast 20-ns speed. Moreover, it is revealed that the local defects at ZrSiO/HfZrO interface affect the ferroelectric negative capacitance tuning and thus increases the variability of VT and SS during 1E12 cycling endurance.

**MY-8 Random Telegraph Noise in HfOx Resistive Random Access Memory: from Physics to Compact Modeling**

F.M. Puglisi, L. Larcher, P. Pavan, University of Modena and Reggio Emilia

As RRAM technology is entering the industrial phase, compact models accounting for variability and RTN effects at circuit level are essential to evaluate the technology potential. Variability and RTN represent major concerns for HfOx RRAM applications such as non-volatile memory, neuromorphic computing, and Physical Unclonable Function (PUF). In this paper, starting from the physics of charge transport and RTN, we develop a physics-based compact model for RTN in RRAM, valid in both high-(HRS) and low-resistance state (LRS). The proposed model is validated on a wide data set and well reproduces also data from the literature. The RTN model can be easily integrated in compact RRAM device models and can describe I-time traces in both resistive states.

# Packaging and 3D Assembly

## Packaging and 3D Assembly

### PA-1 Optimum Filler Geometry for Suppression of Moisture Diffusion in Molding Compounds

W. Ahn, S, Shin, R. Asadpour, L. Nguyen*, D. Varghese*, S. Krishnan*, M. Alam, Purdue University, *Texas Instruments

Inorganic fillers, such as fused silica or organic clay, help tailor/co-optimize the mechanical toughness, thermal conductivity, and moisture diffusivity of polymer mold compounds used to package microelectronic integrated circuits. Despite long history and wide-spread current use, the optimization of filler-infused composites is generally empirical and therefore time-consuming. A physics-based predictive modeling will improve application-specific design of composites that would offer optimum performance and reliability. As an illustrative example, in this paper, we develop a general theory of polymer composites that anticipates the suppression of moisture diffusion as a function of fill-fraction, size-dispersion, shape, and topology of filler nanoparticles. Our results show that the best performance is obtained by incorporation rod-shaped fillers, randomly closed packed at maximum density (~60%). Our numerical results are succinctly captured by the analytical model based on generalized Maxwell Garnett effective medium theory. The analytical model can be used for initial optimization of mold compounds before large-scale numerical modeling is invoked and characterization experiments are designed.

### PA-2 A Finite Element Method Study of Delamination at the Interface of the TSV Interconnects

S. Papaleo, H. Ceric, TU Wien

Through Silicon Vias (TSVs) are the interconnections in three dimensional integrated circuits responsible for the vertical lines inside the dies. In particular, the open TSV has been developed in order to reduce thermo-mechanical issues. This interconnect structure has interfaces where the possibility of a device failure due to delamination needs to be

considered. The Critical Energy Release Rate Gc determines the condition for a fracture to propagate. When the Energy Release Rate G exceeds Gc, a fracture will propagate. Experimental measurements were used to calculate Gc. The experimental Gc, was calculated at the interface between silicon dioxide and tungsten; materials used for Open TSVs. We have developed a model to calculate the G and compared the experimental data with our results. The results obtained are in good agreement with experimental measurements. Therefore, the model developed provides a convenient tool for the study of delamination issues in TSVs.

**PA-3 Electromigration Induced Thermomigration in Microbumps by Thermal Cross-talk Across Neighboring Chip in 2.5D IC**

M. Li, D.W. Kim*, S. Gu*, K.-N. Tu, University of California, Los Angeles, *Qualcomm

This paper investigates the thermal cross-talk between the powered microbumps under one chip and the unpowered microbumps under the neighboring chip. Both chips were on a Si interposer for 2.5D IC. The Joule heating from the powered chip was found to be transferred laterally along the interposer to the unpowered chip and produced a temperature gradient in the microbumps in the unpowered chip. Void formation is observed in both the powered and the unpowered microbumps. The latter is due to thermomigration (TM), and the former is due to electromigration (EM). The amount of voids is bigger by TM than by EM. The void nucleation and growing is studied by examining the un-powered microbumps at different stages during electromigration tests. The nucleation of voids at the cold end in TM is observed, which indicates that Sn atoms diffuse from cold end to hot end. The current-enhanced surface electromigration of Sn along the side walls of Cu pillars to form intermetallic compound is observed in the powered microbumps that were subjected to a 5.3×104 A/cm2 current density at 150 °C for a period of time. The depletion of Sn will cause serious void formation in these powered microbumps.

# Process Integration

## Process Integration

**PI-1 Resolution of Poly Gate to Substrate Contact Short Reliability Failures on Non-Volatile Memory**

S. Chandrasekaran, P. Jowett, T. Mishra, C. Shafer, R. Cruz, K. Noronha, S. Bhosle, V. R. Sanivarapu, N. Rangaraju*, D. Kapoor*, Intel Micron Flash Technologies LLC, *Intel Corporation

Due to continual scaling of CMOS device dimensions, the dielectric spacing between poly gate (PG) and contact to substrate (Con) has been drastically reduced. This reduction in gate to substrate contact spacing has challenged the dielectric breakdown between poly

gate and substrate contact. Several studies involving the breakdown of dielectric between gate and substrate contact have been reported in the past. In this paper, we report the elimination of poly gate to substrate contact shorts on 90 nm Non-Volatile Memory technology with the help of process optimizations in pre-metal dielectric stack. This led to a significant improvement in wafer level reliability metric to the tune of ~1.7X.

**PI-2 Highly-Accelerated WLR Learning Cycles for Development of a Trench MOSFET: Method and Case Study**

G. Hall, D. Moore, P. Burke, M. Suzuki, ON Semiconductor

ON Semiconductor Trench MOSFET integration process is designed to be manufacturable with high yields and world-class reliability. Power MOSFET discrete devices are required to pass a number of packaged level reliability (PLR) tests based on IEC guidelines [1], which involve very long time horizons -e.g. High Temperature Gate Bias (HTGB), and Reverse Bias (HTRB) have 1000+ hour time-on-test. When developing a new integration or design, it is of high value to have an expedient methodology for providing fast results on design-of-experiments (DOE), which lead to process or design paths with a high likelihood of passing qualification. In this study we describe the use of WLR methodology to identify an optimized Trench MOSFET gate salicidation scheme. The DOE splits were evaluated using a highly accelerated wafer level bias temperature instability test (WLBTI), and Wafer Level Time Dependent Dielectric Breakdown (WLTDDB). The process conditions which had acceleration factors predicting optimal results at PLR and use conditions were selected for qualification using the standard PLR program. The business case for using WLR methodology to evaluate cycles of learning is clear when one considers the impact to time-to-market of innovative technologies.

# Product IC Reliability

## Product IC Reliability

**PR-1 Modelling of 1T-NOR Flash Operations for Consumption Optimization and Reliability Investigation**

J. Coignus, G. Torrente*, A. Vernhet, S. Renard*, D. Roy*, G. Reimbold, CEA, LETI, *STMicroelectronics

Based on novel experimental capabilities, Flash NOR memory consumption, scalability and reliability trade-off is addressed, by mean of programming and erase operation schemes modelling. A fine tuning of programming energy and max. current is provided, together with an extended description of Flash programming dynamics along device ageing. Optimized cycling conditions are shown to reduce power consumption without any detrimental impact on device reliability.

**PR-2 Near Neighbor Sort Yield & Wafer Sort Yield Impact on Product Burn-In and a Time-Dependent Reliability Study**

R. Heller, Jr., Advanced Micro Devices

Local Yield is the yield of near neighbor die to a central die at wafer sort (excluding the results of the central die). It has been shown in literature that the local yield of a die can estimate the future reliability of the die. Die that come
from regions of other passing die pose less reliability risks than faulty regions. This is due to defect clustering and the fact that same killer defects that cause sort fails are the same types of defects that cause latent defects only differing in size and location. Based on information we can gather at Wafer Sort, does it make sense to have a "one size fits all" approach for a downstream production burn-in screen? What techniques can we use to better identify potentially unreliable die? Can we use Local Yield and Wafer Sort Yield to better determine burn-in durations? This paper examines all of these questions and the relationship between yield and reliability using both Local Yield and Wafer Sort Yield and production burn-in using a production dataset of AMD CPU. This paper also examines the time-dependent reliability fallout during production burn-in by near neighbor sort bin.

**PR-3 Machine Learning-Based Proactive Data Retention Error Screening in 1Xnm TLC NAND Flash**

Y. Nakamura, T. Iwasaki, K. Takeuchi, Chuo University

A screening method to proactively reduce data retention error, based on screening of PD-weak cells, where PD-weak cells have high program disturb error frequency. Repeated measurement of program disturb (P.D.), indicates that 25% of P.D. errors are concentrated in 3.5% of the memory cells, called PD-weak cells. PD-weak cells have 4× worse data retention (D.R.) than non- PD-weak cells, therefore retention errors can be reduced by PD-weak cell screening. Proactive D.R. detection is a new capability, because conventional retention testing times are not practical during product test. In 1Xnm TLC NAND flash, removal of PD-weak cells with <2% overhead extends D.R. by 30%. The method to measure PD-weak cells is described, as well as machine learning to model and detect PD-weak cells. Finally, detection rate vs. false detection cost is compared for 3 learning algorithms.

# Photovoltaics Reliability

## Photovoltaics Reliability

**PV-1 Study of the Potential-Induced Degradation Kinetics**

J. Bengoechea, M. Ezquer, J. Diaz, A.R. Lagunas, National Renewable Energy Centre

A dedicated set-up which allows a real-time characterization of the PV modules, while being subjected to the Potential-Induced Degradation (PID) test, was developed and tested. This real-time characterization includes the measurement
of the dark I/V curve and the acquisition of electroluminescence (EL) images at different biasing levels. By means of this realtime characterization it is possible to early identify the PID presence and its kinetics during the total duration of the test.This set-up allowed the investigation of the influence of salt as an impurity in module packaging with regard to PID. To this aim, a mini-module contaminated with salt including on the surface of one of its solar cells and in the glass-EVA interface was laminated. This mini-module showed an increased susceptibility to PID, which developed also in the uncontaminated solar cells. Repetitions of the PID test showed that its influence diminished with the number of cycles.

**PV-2 Potential Induced Degradation in High-Efficiency Bifacial Solar Cells**

M. Barbato, M. Meneghini, A. Cester, A. Barbato, G. Tavernaro*, M. Rossetto*, G. Meneghesso, University of Padova, *MegaCell S.r.l.

This paper presents an analysis of the degradation of Bifacial Solar Cells submitted to potential induced degradation (PID) stress. We report the results obtained on cells with two different encapsulation materials: ethylene-vinyl-acetate (EVA) and polyolefin elastomer (POE). Results show that the use of different encapsulation materials may result in a better robustness towards PID in Bifacial Solar Cells.

**PV-3 Improvement of DSSC Performance by Voltage Stress Application**

A.Scuto, G. Di Marco*, G. Calogero*, I. Citro*, F. Principato**, C. Chiappara**, S. Lombardo,, CNR IMM, *CNR IPCF, ** Università degli Studi di Palermo

Dye-sensitized solar cells (DSSCs) are promising third generation photovoltaic devices given their potential low cost and high efficiency. Some factors still affect DSSCs performance, such structure of electrodes, electrolyte compositions, nature of the sensitizers, issues of power conversion efficiency and stability under prolonged electrical cycles, etc. In this work we discuss the effect of electrical stresses, which allow to improve DSSC performance. We have investigated the outcomes of forward and reverse DC bias stress as a function of time, voltage, and illumination level in the DSSCs sensitized with the N719, Ruthenium complex based dye. We demonstrate that all the major solar cell parameters, i.e., open circuit voltage (VOC), short circuit current (ISC), series resistance (ROC), fill factor (FF), and power conversion efficiency are strongly influenced by the stress conditions and a clear reversibility of the parameters on the stress type is shown. In this context we examined the possible effects that emerge from the electrolyte composition. Our study suggests that under proper biasing the DSSCs noticeably improve in terms of efficiency and long-term stability.

**PV-4 Adhesion Requirements for Photovoltaic Modules of Polymeric Encapsulation**

J. Zhu, G. Surier, D. Wu, D. Montiel-Chicharro, T. Betts, R. Gottschalg, Longborough University

This paper addresses the delamination issue and investigates the adhesion requirement and failure of packaging material at the different interfaces. Lamination condition has significant impacts on the adhesion stability and failure modes, which will be further investigated too.

# Soft Errors

## Soft Errors

### SE-1 Alpha-Particle and Neutron-Induced Single-Event Transient Measurements in Subthreshold Circuits

M. Gadlage, J. Albhin*, P. Gadfort**, S. Stansberry***, A. Roach, A. Duncan, M. Kay, NSWC Crane, *MDA, **Army Reseach Lab, ***USC-ISI

Experimental data from alpha particle testing are dis-cussed and analyzed from a sub-threshold voltage SET characterization circuit. Using a Schmitt trigger inverter target chain fabricated in a 28-nm bulk CMOS process, SET pulse widths are captured from an operating voltage down to 0.32 V. These results show that alpha particles can induce SET pulse widths that range up to hundreds of nanoseconds when operating at voltages well below the nominal voltage. Additionally, the alpha particle results show that sub-Vt circuits are significantly more susceptible, as compared to circuits operating at nominal voltages, to low-energy particles inducing SETs that have a high probability of being latched as errors in a combinatorial logic design.

### SE-2 Error Characterization and Mitigation for 16nm MLC NAND Flash Memory under Total Ionizing Dose Effect

Y. Li, D. Sheldon*, A. Ramos, J. Bruck, California Institute of Technology, *NASA Jet Propulsion Laboratory

This paper investigates the system-level reliability that 16nm MLC NAND flash can offer to SSDs under total ionizing effect for storage in space. Measurements show that blocks that carried less than 3k program/erase cycles (PECs) only survived up to 10k rad total doses under the protection of standard ECCs. We characterize errors at the levels of threshold voltage Vt, cell logical state, and binary bit, respectively, and study error mitigation schemes for reliability enhancement. We adopt a novel data representation where data are read using the relative order of cell voltages.
Experimental results show that the new representation reduced bit errors by 60% on average. We propose a new memory scrubbing (MS) scheme that refreshes cells without block erasure and operates under lower voltage. Measurements show that flash blocks

survived up to 8k PECs and 57k rad total doses using the new scrubbing scheme. Both schemes were implemented as parts of a flash controller, and significantly outperform existing methods in various aspects.

**SE-3 Investigating the Single-Event-Transient Sensitivity of 65 nm Clock Trees with Heavy Ion Irradiation and Monte-Carlo Simulation**

V. Malherbe, G. Gasiot, S. Clerc, F. Abouzeid, J.-L. Autran*, P. Roche, STMicroelectronics, *Aix-Marseille Université

We present a study of single-event transients in clock tree structures in 65 nm bulk silicon technology. Shift registers are irradiated with heavy ions over a large range of linear energy transfers representative of both terrestrial and space environments. By attributing large error clusters in the flip-flop shifters to clock tree events, we derive experimental cross sections for the clock tree cells. Monte-Carlo irradiation simulations performed on the same structures are in good agreement with these data, allowing to assess the radiation robustness of other clock-tree configurations.

**SE-4 Exploiting Low Power Circuit Topologies for Soft Error Mitigation**

N. Mahatme, S. Jagannathan, N. Gaspard,III*, B. Bhuva**, S. Wen***, R. Wong***, I. Chatterjee^, T. Assis**, NXP Semiconductor, *Altera Corporation, **Vanderbilt University, ***Cisco, ^University of Bristol

Alpha particle experimental results for arithmetic circuits implemented using transmission gate logic in 20-nm bulk technology node are shown to have 35% lower soft error rate as well as 30% lower power consumption compared to standard CMOS circuits. Analytical models confirm the experimental trends and help optimize and predict the power-SER trade-off.

**SE-5 Estimation of Single-Event Transient Pulse Characteristics for Predictive Analysis**

T. Assis, J. Kauppila, B. Bhuva, R. Schrimpf, L. Massengill, R. Wong*, S. Wen*, Vanderbilt University, *Cisco

Estimate the Single Event Transient (SET) pulse width of standard cells is challenge task requiring hundreds of spice simulations for the library characterization. In this work analytical models are used to estimate the SET pulse width for multiple standard cells considering both different hit node locations and charge sharing. By using the Ambipolar-Diffusion-Cutoff (ADC) model extension this methodology is also able to properly model the SET Pulse Quenching effect. The model requires a simple characterization step performed only once for 3 simple circuits. Comparison with electrical simulations (SPICE) for 4 technologies shows great model accuracy. Heavy ion experiments in a 65nm bulk technology Test Chip also show good accuracy. The simple model formulation and low

computational requirements make this methodology ideal to be used by Electronic Design Automation (EDA) tools.

**SE-6 Predicting the Vulnerability of Memories to Muon-Induced SEUs with Low-Energy Proton Tests Informed by Monte-Carlo Simulations**

J. Trippe, R. Reed, B. Narasimham*, B. Sierawski, R. Weller, R. Austin, L. Massengill, B. Bhuva, K. Warren, Vanderbilt University, *Broadcom Corporation

Low-energy terrestrial muons have been shown to induce single-event upsets (SEUs) in complementary metal-oxide semiconductor (CMOS) static random access memories (SRAM). Only a handful of facilities produce surface muon beams, and these facilities have limited access to muon beamtime. As a result, it is difficult to carry out experiments to evaluate and/or characterize vulnerability to muons. To address the lack of muon beam availability, this work presents a method for determining a design's vulnerability to muon-induced upsets by performing tests at a readily available, low energy proton facility. It is shown that low-energy protons have similar characteristics as muons for soft error effects. This will allow test engineers to use proton test results to determine if a device is vulnerable to muon induced upsets.

# Transistor Reliability

## Transistor Reliability

**XT-1 Alteration of Oxide-Trap Switching Activity at Operating Condition By Voltage-Accelerated Stressing**

Z.Y.Tung, D.S. Ang, Nanyang Technological University

It is found that voltage-accelerated stressing can change the switching activity of a time-zero oxide defect measured under operating condition. The defect can be rendered either less active or more active by the applied stress, implying a possible modification of its atomic structure. With the impact of oxide trapping on MOSFET channel conduction becoming increasingly important as device dimension decreases, the observed stress-induced alteration of trap-switching behavior under operating condition should be a consideration in the reliability assessment of small-area devices.

**XT-2 Nano-Scale Evidence for the Superior Reliability of SiGe High-k pMOSFETs**

M. Waltl, A. Grill, G. Rzepa, W. Goes, J. Franco*, B. Kaczer*, J. Mitard*, T. Grasser, TU Wien, *imec

It has recently been demonstrated that the susceptibility of conventional Si channel pMOSFETs to the negative bias temperature instability (NBTI) is a serious threat to further

scaling. One possible solution to this problem is the use of SiGe quantum-well devices, which not only offer high mobilities but also superior NBTI reliability. It has been speculated that the latter is due to the band offset of the SiGe channel with respect to Si, which increases the energetic separation between the defect bands in the high-k gate stack and the channel. We investigate this claim by comparing single-defects in nano-scale devices to the behavior of the large number of defects visible in large-area devices. Using detailed TCAD simulations we determine the energetic and spatial locations of the traps in the gate stack and confirm that the previously developed picture correctly explains the significant reliability benefits of SiGe channel devices.

**XT-3 Negative Bias Temperature Instability Lifetime Prediction: Considering Frequency, Voltage and Activation Energy via Novel Methodology of MSM-SFMF**

C.H. Chiang, N. Ke, S. N. Kuo, C. J. Wang, K. C. Su, United Microelectronics Corporation

The reliability of pMOSFETs is limited by NBTI. Recent NBTI studies for aggressive scaling CMOS technology found the recoverable component. According to the present observation, the recoverable component is contributed by hole trapping while the permanent component is explained by the creation of interface. It implies that NBTI results from two tightly coupled mechanisms. This paper discusses a new measuring skill that helps us to realize characteristic of traps via frequency, voltage and temperature [4]. After considering activation energy (Ea), traps can be divided into three types. It includes simple concept of Reaction-Diffusion (RD) and two-stage models, and doesn't need complicated mathematics operations. Consequently, it benefits the study of transistor NBTI behavior.

**XT-4 Device-Level Jitter as a Probe of Ultrafast Traps in High-k MOSFETs**

D. Veksler, J. Campbell, J. Zhong*, H. Zhu*, C. Zhao*, K. Cheung, National Institute of Standards and Technology, *Chinese Academy of Sciences, *IMECAS

We developed the methodology to quantify ultra-fast interface traps using jitter measurements as a probe. This methodology was applied to study the effect of PBTI stress in high-k/Si MOSFET on density of fast interface traps (500ps to 5ns timescale). It was shown that increase of jitter of 2Gbt/s signal caused by stress is solely related to the degradation of a FET threshold voltage, while density of fast interface traps is not affected by PBTI stress. The developed methodology can be used for evaluation of the interface quality and quantification of fast interface traps in MOSFET and HEMT devices, built using different technologies and material systems. It can be used to study interface degradation induced by different type of stresses, including electric, thermal, and radiation effects.

**XT-5 Spatio-Temporal Mapping of Device Temperature due to Self-Heating in Sub-22nm Transistors**

M.A. Wahab, S. Shin, M.A. Alam, Purdue University

With the increase of transistor density and adoption of novel geometries, such as, FinFET, ETSOI, and gate-all-around (GAA) transistors, self-heating has emerged as a persistent concern for modern ICs. Various reliability issues, such as, NBTI, HCI, PBTI, and TDDB depend sensitively on channel temperature, ⟦ΔT⟧_C (x,y,z;t), due to self-heating. An accurate spatio-temporal map of channel temperature is essential for Fin-resolved reliability/lifetime of sub-22 nm technology nodes. In this paper, we demonstrate that (i) none of the existing techniques, in isolation, can map the Fin-resolved channel temperature of modern transistors, and (ii) only a collection of orthogonal techniques (multiprobe approach) or novel test structures (material approach), integrated/interpreted through self-consistent electro-thermal simulation, can map the temperature in sufficient detail necessary for reliability prediction.

**XT-6 Surface-Potential-Based Compact Modeling of BTI**

I.S. Esqueda, H. Barnaby*, University of Southern California, *Arizona State University

Characterization and modeling of bias temperature instability (BTI) is conventionally based on time-dependent shifts in threshold voltage (Vth) resulting from stress and relaxation conditions. Contributions of oxide near-interfacial (i.e., border) and interface traps are not independently captured in these conventional methods. By considering the effects of charge trapping dynamics on MOSFET operation, we present new techniques for characterizing and modeling the contributions of oxide and interface traps. Characterization is based on the rapid response of interface traps to high-frequency measurements of inverse subthreshold slope (S), for which slower oxide traps do not contribute, as their occupancy does not change at high frequencies. The modeling approach uses calculations of surface potential (ψs) to describe the distinct contributions of oxide and interface traps on BTI. Combined with capture/emission time maps, this approach describes BTI induced ΔS, and ΔVth stress/recovery characteristics.

**XT-7 Width and Layout Dependence of HC and PBTI Induced Degradation in HKMG nMOS Transistors**

N. Mahapatra*, P. Duhan, V. Rao, Indian Institute of Technology Bombay, *Indian Institute of Technology Gandhinagar

In this abstract, we have studied the width dependence of HC and PBTI induced degradation in HKMG nMOS transistors. It is clearly shown that the oxygen vacancies play a major role in the long term reliability of the HKMG nMOS transistors and this could be improved by dividing the active into multiple active fingers and by increasing the active-to-active spacing.

**XT-8 Characterization and Modeling of NBTI Permanent and Recoverable Components Variability**

D. Nouguier, X. Federspiel, G. Ghibaudo*, M. Rafik, D. Roy, STMicroelectronics, *University of Grenoble Alpes

In this paper we use a statistical analysis of NBTI recoverable and recoverable component measured on Pfet device issued from ST Microelectronics 28nm FDSOI technology. From measurement of NBTI degradation and recovery measured at µs time scale, resulting from AC and DC stress, we performed statistical analysis of the permanent and recoverable components and analyzed it separately. Accordingly, we proposed a Dual Defect Centric Model (DDCM) to account for differences of these two components.

**XT-9 Temperature Sense Effect in HCI Self-heating de convolution – Application to 28nm FDSOI**

X. Federspiel, G. Torrente, W. Arfaoui, V. Huard, F. Cacho, STMicroelectronics

Hot carrier injection (HCI) remained a major reliability concern for advanced CMOS nodes due to lateral field increase with device scaling but also due to increase of power dissipation [1,2,3,4]. HCI was reported as a wear-out mechanism that induces interface traps and oxide traps which cause in turn MOS device parameter drift. Parameter drift models were published to take into account lateral field, impact ionization, carrier energy distribution as well as local channel temperature. Recently, the need to deconvolute self-heating from HCI apparent voltage acceleration was pointed out to obtain accurate reliability modeling [5,6,7]. We will show here, that calculating temperature activation as if only depicting defect generation activation is an incomplete description of temperature dependency and that parameter drift temperature sensitivity factor must also be taken into account to correctly model HCI out. In the following, sense effect will refer to sensitivity of MOS parameter drift to temperature for a constant number of defect.

**XT-10 Comparative Experimental Analysis of Time-dependent Variability using a Transistor Test Array**

M. Simic, A. Subirats*, P. Weckx*, B. Kaczer*, J. Franco*, P. Roussel*, D. Linten*, A. Thean*, G. Groeseneken, G. Gielen, KU Leuven, *IMEC

As the transistors dimension reach the deca-nanometer scales, time-zero and time-dependent variability, which includes Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI), become a great concern for IC design. Accurate statistical models describing these two variability sources are necessary in order to design reliable circuits and systems. This paper gives insights in the geometry scaling of these variabilities and studies time-dependent variability through three different measurement techniques: the 2-point Measure-Stress-Measure, the Time Dependent Defect Spectroscopy, and the precise IdVg. Advantages and downsides of each technique are discussed.

# IRPS 2016 Poster Sessions

# Compound/Opto Electronics

## Compound/Opto Electronics

### CD-1 On Conduction Mechanisms through SiN/AlGaN based Gate Dielectric and Assessment of Intrinsic Reliability

A. Banerjee, P. Vanmeerbeek, L. De Schepper, S. Vandeweghe, P. Coppens, P. Moens, ON Semiconductor

The first section of this article focuses on the investigations of the gate leakage conduction mechanisms under forward and reverse bias conditions using temperature dependent Jg-Eg characteristics on a Silicon Nitride (SiN)/AlGaN based Metal-Insulator-Semiconductor (MIS) structure. TCAD study under forward bias conduction show majority of the voltage drop on the SiN layer only. The model fitting the electrical characteristics was observed to be Poole- Frenkel (PF) emission. Under reverse bias condition, the entire voltage drop occurs on the entire SiN/AlGaN/GaN. The conduction mechanism responsible for the leakage was found to be Fowler-Nordheim (FN) tunneling along with a thermionic emission component. Second section of this article focuses on the Time Dependent Dielectric Breakdown (TDDB) measurements and lifetime extrapolation of the SiN/AlGaN based di-electric stack. TDDB measurements were done under constant field stress for different temperatures. Normalization of the data exhibited only field accelerated degradation with no influence from the temperature.

### CD-2 Correlation Between Dynamic RDSon Transients and Carbon Related Buffer Traps in AlGaN/GaN HEMTs

F. Iucolano, A. Parisi, S. Reina, A. Patti, S. Coffa, G. Meneghesso*, G. Verzellesi**, F. Fantini**, A. Chini**, STMicroelectronics, *University of Padova, **University of Modena and Reggio Emilia

The on resistance increment observed when the device is operated at high drain-source voltages is one the topics that limits the performance of the AlGaN/GaN HEMT devices. In this paper, the physical mechanisms responsible of the RDSon degradation are investigated. The dynamic RDSon transient method is used in order to get insight to characterize the traps states. By calculating the Arrhenius plot associated with the RDSon transients an activation energy of 0.86eV was extracted, that can be correlated to the traps due to the incorporation of Carbon inside the buffer. This hypothesis was further supported by the analyses performed on a simpler structure (TLM). By applying a negative substrate bias the effect of only the buffer traps was studied. A fairly close value of the

activation energy (0.9eV) to the one extracted when analyzing the RDSon transient was obtained.

**CD-3 Investigation of Trapping Effects on AlGaN/GaN HEMT under DC Accelerated Life Testing**

W. Sun, C. Lee*, P. Saunier*, S. Ringel, A. Arehart, Ohio State University, *Qorvo Inc

GaN-based high electron mobility transistors (HEMTs) were subjected to DC-based accelerated life testing to determine which defect levels form or are activated, and how they impact the static and dynamic HEMT performance. The primary static changes were a negative shift of the threshold voltage and an increase in knee walkout/onresistance. The primary dynamic effect of the stressing appeared in the form of a time-dependent increase in the onresistance, and this was found to correlate to first order with formation and/or activation of traps at EC-0.57 and EC-0.72 eV traps that contributed to the dynamic changes, and the EC-1.5 eV trap was likely responsible for the static change in onresistance. Trapping kinetics analysis revealed that the physical sources for the EC-0.57 and EC-0.72 eV states are not simple, ideal, non-interacting point defects, but instead are associated with physically extended defects, such as dislocations, and/or defect complexes.

**CD-4 Evaluations of Threshold Voltage Stability on COTS SiC DMOSFETs Using Fast Measurements**

D. Habersat, R. Green, A. Lelis, US Army Research Laboratory

Threshold voltage (VT) stability of commercial SiC DMOSFETs during bias-temperature stressing was evaluated using the fast-ID and fast ID-VGS measurement techniques at both room and elevated temperatures. Unipolar bias stress results confirmed that there is a rapid recovery of VT and that all vendors' devices showed the same basic charge-trapping behavior, although some differences were observed in negative bias response at high temperatures. In situ VT measurements during 10 kHz gate switching showed stable device operation at room temperature but accelerating VT drift and increasing switching oxide trap densities when operated at 175 °C. VT hysteresis during high temperature gate switching indicates the presence of a mobile ion or polarization effect in addition to the expected interface- and oxide-trap charging mechanisms.

**CD-5 Device Breakdown Optimization of Al2O3/GaN MISFETs**

X. Kang, S. Yamazaki, K. Takeuchi, Chuo University

In this paper we demonstrate a solution to achieve robust enhancement-mode Al2O3/GaN MISFETs with a high breakdown voltage and suggest a possible model for the device off-state breakdown. It is found that the device breakdown exhibits different gate voltage dependence for different surface treatments before the gate dielectric deposition. The device performance is greatly improved by using an in-situ surface plasma treatment. The improved device performance is explained by a reduction of traps at the Al2O3/GaN

interface, which finally leads to a reduction in the amount of trapped positive charges and associated with that a reduction of the effective electric field across the gate dielectric when the device isin off-state. Several experimental results support this hypothesis: (1) The recoverable negative threshold voltage shift after reverse gate bias depends on the interface clean before gate dielectric deposition, (2) The reverse bias gate dielectric breakdown voltage is improved by this interface plasma treatment, although the forward bias gate dielectric breakdown voltage is identical.

# Design for Circuit Reliability

## Design for Circuit Reliability

### CR-1 The Impact of Process Variation and Stochastic Aging in Nanoscale VLSI

S. Kiamerh, P. Weckx*, M. Tehoori, B. Kaczer*, H. Kukner*, P. Raghavan*, G. Groeseneken**, F. Catthoor*, Karlsruhe Institute of Technology, *IMEC, **KU Leuven

With the down-scaling of CMOS technology into deep nano-scale era, negative-bias temperature instability (NBTI) effect becomes stochastic due to its widely distributed defect parameters. As a result, the delay degradation due to intrinsic variability of NBTI becomes also stochastic and the matter is aggravated when it is combined with process variation (PV). Accurate stochastic timing analysis of the circuit becomes very important in this case since over and under margining can lead to significant performance or yield loss (timing failure), respectively. This paper proposes a scalable flow and investigates the combined effect of stochastic NBTI and process variation on the performance of the VLSI design at the circuit level in a 7 nm FinFET technology node by abstracting atomistic NBTI models (for the stochastic behavior) to the circuit timing analysis flow.

### CR-2 Mismatch Circuit Aging Modeling and Simulations for Robust Product Design and Pre-/Post-Silicon Verification

H. Shim, Y. Kim, J. Jeon, Y. Cho, J. Park, S. Pae, H. Lee, Samsung Electronics

As technology scales down, PMOS NBTI-induced mismatch, in addition to the NBTI mean-shifts and time0-Vt variation, is critical for designing circuitry having matched pair transistors, such as OP amplifier. This paper covers mismatch aging models incorporated into design simulation tool for PMIC products and used the Monte-Carlo simulation to consider process and systematic variations for robust design. Circuit simulation for PMIC OP Amp and its output characteristics were investigated and then further validated through the post-silicon HTOL stress. The pre-silicon simulation further enables to optimize HTOL stress conditions.

### CR-3 Aging of IO Overdrive Circuit in FinFET Technology and Strategy for Design Optimization

S.-E. Liu, M.-H. Yu, Y.-J. Chen, J.-Y. Jao, M.-Z. Lin, Y.-H. Fang, M.-J. Lin, MediaTek

We investigated aging property of FinFET-based I/O overdrive circuits (IP) and proposed design strategies of optimization among performance/area/reliability. Aging behavior of I/O overdrive IP with 16nm FinFET process has been extracted and compared with 20nm planar-transistor process. Both pulldown and pull-up driving degradation are worse in the FinFET than planar IP. An aging simulation framework was built from transistor-level aging databases and further calibrated by an empirical equation and IP-level measurements. Finally, a design guideline was discussed and proposed to pursue balance of performance/ area/reliability, which is thus improved 13%/8%/37% respectively in our optimized design.

**CR-4 Robustness of Timing in-situ Monitors for AVS Management**

A. Benhassain, F. Cacho, V. Huard, S. Mhira, L. Anghel*, C. Parthasarathy, A. Jain, A. Sivadasan, STMicroelectronics, *Grenoble University

This paper deals with the fundamental aspects of the introduction of aging sensor in digital circuit, describing a new In-situ Timing Monitor (ISM), insertion flow and experimental results .

# Dielectric Reliability (Front-end and Back-end)

## Dielectric Reliability (Front-end and Back-end)

**DI-1 Moisture Impact on Dielectric Reliability in Low-k Dielectric Materials**

K.-D. Lee, Q. Yuan, A. Patel, Z. Mai, L. Brown, S. English, Samsung Austin Semiconductor

With intentional moisture uptake and removal, we modulate the moisture level in porous low-k dielectric materials, and investigate the moisture impact on dielectric reliability at a wide range of stress conditions. From this study, we confirm moisture can cause a significant degradation in dielectric reliability (i.e., x1.0E-06 in TDDB lifetimes) . Interestingly, the moisture impact is not permanent (with good Cu-diffusion barrier) and can be restored effectively with a high temp annealing at ≥ 350°C. Different from previous studies, moisture does not always increase the leakage currents nor change the TDDB modeling parameters, indicating there are at least two moisture states in porous low-k dielectric materials. In this paper, we will discuss the moisture-induced reliability degradation mechanisms.

**DI-2 Impact of Trap Creation at SiO2/Poly-Si Interface on Ultra-thin SiO2 Reliability**

Y. Mitani, M. Suzuki, Y. Higashi, R. Takaishi, Toshiba Corporation

The relationship between TDDB characteristics of the devices having ultrathin SiO2 as gate dielectrics and the hydrogen-related trap creation have been re-investigated from the viewpoint of the oxidation process dependence. In order to study the influence of hydrogen on the reliability, deuterium isotope effect has been used. As a result, the Weibull distributions of time-to-breakdown (tBD) depends on the oxidation process condition even under the same oxidation temperature. Trap creation at gate oxide interface strongly correlates to the dielectric breakdown in ultra-thin gate oxides However, this oxidation process dependence could not be explained only by the amount of hydrogen release from SiO2/Si substrate interface From the experimental results of low-voltage SILC, it can be concluded that not only the released hydrogen from SiO2/Si substrate interface but also those from Poly-Si/SiO2 interface correlates to the breakdown mechanisms.

**DI-3 A Fast Reliability Screening Technique for Identification of Trap Generation**

K. Joshi, Z.-R. Xiao, S.-H. Gao, C. Huang, T.-M. Shen, P.J. Liao, Y.-H. Lee, J-R. Shih, Taiwan Semiconductor Manufacturing Company

SILC spectrum technique is used to identify trap generation location in both PMOSFETs and NMOSFETs under BTI stress. It is validated using SILC spectrum technique that BTI stress in PMOSFETs leads to trap generation in IL/HK intermix whereas in NMOSFETs leads to trap generation in HK layer. Atomistic simulations are further performed to calculate formation energy for oxygen vacancies in various gate oxide layers. It has been validated that it is easy to generate hole traps in IL/HK intermix region under NBTI stress in PMOSFETs and easy to generate electron traps in HK layer in NMOSFETs under PBTI stress. The advantage of this technique is its ease of use and higher throughput thus making it an ideal tool for a quick scanning of trap generation locations and to understand the reliability strength of each layer under different processing conditions.

**DI-4 Correlation between the Variation in the Initial Current at Stress and the Variation in the Failure Time During TDDB Testing of BEOL Structures**

R. Filippi, C. Christiansen, A. Kim*, B. Li*, P-C. Wang, Globalfoundires, *IBM

A novel approach for estimating variation in the TDDB failure time is reported. The results for various test structures reveal that variation in the initial current at stress reasonably predicts variation in the TDDB failure time. The approach is a non-destructive method that only requires a current measurement, making it an efficient monitor of the expected TDDB lifetime behavior during manufacturing of an established process.

**DI-5 Towards an Appropriate Accelerate Model for BEOL TDDB**

R. Muralidhar, E. Linger, T. Shaw**, A. Kim, G. Bonilla*, IBM TJ Watson Research Center

We have evaluated the veracity of BEOL acceleration models using the largest set of data spanning 3 pitches. The raw data indicates same acceleration trends in the 3 pitches enabling them to fall into a universal curve by re-normalization to account for different areas. While the Root-E (RE), Impact Damage and Power-Law (PL) models fit data over entire range well, it is seen that only the Impact Damage and Power Law models predict the low field data when high field data alone is used to fit the models. This ability to extrapolate and the constancy of acceleration factors at low and high fields makes these models more appropriate for determining lifetime at operating conditions from a fit of high field data alone. While the ID model has 3 parameters and presents fitting challenges, the PL model is a good practical alternative and may have its physical basis on arguments based on scaling theory. The paper will additionally discuss in detail statistical analysis including clustering model, fitting aspects of ID model and physical basis of the power-law model from scaling point of view.

**DI-6 Evaluation of Inter and Intra Level TDDB of Cu/Low-k Interconnect for High Voltage Application**

M. Lin, C. Yang, H.-Y. Chen, A. Juan, K.C. Su, United Microelectronics Corp.

The conduction current and TDDB of intra and two kinds of inter level low-k dielectric structures for high voltage application are studied. Electrical field distributions are different on the different structures and impact the TDDB results. Failure analysis shows the Cu ion diffusion and SiCN interface are the dominant impact factor of the low-k dielectric breakdown. An inter level layout design principle to improve dielectric reliability under high voltage operation is suggested.

**DI-7 Effect of H2O on TDDB for a Range of ULK ILD Materials with Varying Damage Resistance for Robust and Weak Liners**

E. Linger, R. Laibowitz*, T. Shaw, S. Cohen, A. Raja*, IBM TJ Watson Research Center, *Columbia University

In this study we look at the correlation between TDDB lifetime, in the presence of intentionally introduced H2O and top surface damage for different ILD materials using a robust liner. The activation energy for the movement of loosely bound physi-adsorbed H2O has been obtained using AC loss measurements. We also explore the role of moisture in drawing Cu out of metal lines through an intentionally fabricated thin/weak liner under prolonged stress at a relatively low voltage. AC loss, I-V, triangular voltage sweep (TVS) and TDDB measurements all provide evidence that Cu is migrating out of the lines into the ILD.

**DI-8 Reliability-Performance Trade-off For Work- Function Optimization In Advanced Node Replacement Metal Gate Technology**

R. Ranjan, T. Nigam, B. Parameshwaran, Y. Liu, S.F. Yap, Globalfoundries

In this work, we explore the complex interaction of the gate stack process and time-dependent-dielectric breakdown (TDDB) in high-K (HK) replacement metal gate (RMG) technology. TDDB is a key reliability metric governing the product lifetimes under long-term operation. Based on this study, it is observed that TDDB is greatly modulated by the proximity of Al to the MG/HK interface. The key parameter modulated by gate stack optimization is voltage acceleration exponent (VAE) for TDDB. All observations indicate higher VAEs can be achieved by keeping the Al away from the MG/HK interface.

# ESD and Latch-up

## ESD and Latch-up

### EL-1 ESD Self-Protection Design on 2.4-GHz T/R Switch for RF Application in CMOS Process

C.-Y.Lin, R.-H. Liu*, M.-D. Ker*, National Taiwan Normal University, *National Chiao Tung University

The RF transceiver front-end for 2.4-GHz applications realized by a fully integrated T/R switch with ESD self-protection capability is presented in this work. Experimental results show that the proposed design can provide enough ESD self-protection capability with good RF performances.

### EL-2 Failure Mechanism of High-Voltage Isolated Lateral Diffused NMOS under High-Current Events

C.-H. Wu, J.-H. Lee*, C.-H. Lien, National Tsing Hua University, *Globalfoundries

In this study, the mechanism of the effect of a high-voltage (HV) NWell guardring (NW-GR) on the electrostatic discharge (ESD) robustness of the HV isolated lateral diffused NMOS (HV ISO-LDNMOS) is investigated. The device fails on low-voltage ESD zapping events when the HVNW-GR is connected to the drain, whereas the device passes these events once it is floated.

### EL-3 Optimization of PESD Implant Design for ESD Robustness of 5V Drain-Back N-LDMOSFET

C. Chiang, P.C. Chang, P.-S. Tseng, P.-Y. Lai, H. Tang, K.C. Su, UMC

An N-LDMOS ESD protection device with drain back and PESD optimization design is proposed. With PESD layer enclosing the N+ drain region, a parasitic SCR is created to achieve high ESD level. When PESD is close to gate, the turn-on efficiency can be further improved (Vt1: 11.2V reduced to 7.2V) by the punch-through path from N+/PESD to PW. The proposed ESD N-LDMOS can sustain over 8KV HBM with low trigger behavior.

**EL-4 On-Chip Protection in Precision Integrated Circuits Operating at High Voltage and High Temperature**

J. Salcedo, J.-J. Hajjar, J. Zhao, Analog Devices

A new high voltage swing bipolar ESD (electrostatic discharge) protection device for enabling low leakage precision mixed-signal interface circuits (ICs) operating at high voltage (~ 40V to 60V) and high temperature (~125°C to 200°C) is presented. Under these operating conditions, parasitic structures in junction-isolated high voltage process technologies induce unexpected shift in the leakage current over time, leading to malfunction in the precision high voltage input/output interface circuit. A proposed device design addresses the low leakage targets at the mentioned operating conditions, while achieving the required ESD robustness of the high voltage interface for industrial applications.

**EL-5 Improving the Long Pulse Width Failure Current of NPN in BiCMOS Technology**

Y. Xiu, A. Appaswamy, Z. Chen*, A. Salman, M. Dissegna, G. Boselli, E. Rosenbaum*, Texas Instruments, *University of Illinois at Urbana-Champaign

The pulse width dependency of the failure current for NPN structures in a 0.18-µm BiCMOS technology is studied using measurements and TCAD simulation. The desired "Wunsch-Bell" behavior is not observed due to formation of current filaments in this device; however, the failure current for long pulse widths can be increased by layout changes.

**EL-6 Analysis of ESD Effects on Organic Thin-Film-Transistors by Means of TLP Technique**

N. Wrachien, M. Barbato, A. Cester, A. Rizzo, G. Meneghesso, R. D'Alpaos*, G. Turatti*, G. Generali*, M. Muccini**, University of Padova, *ETC srl, **CNR-ISMN

We analyzed the effects of Electrostatic Discharge events on large area high voltage Organic Thin Film Transistors, using the transmission line pulsing technique. These transistors survived ESD events exceeding 500V. A partial dielectric breakdown occurred at voltage higher tan 600V. Small mobility and threshold voltage variations are observed, prior breakdown.

**EL-7 Unique ESD Behavior and Failure Modes of AlGaN/GaN HEMTs**

B. Shankar, M. Shrivastava, Indian Institute of Science

Present experimental study reports various failure modes under ESD stress conditions and distinct ESD behavior of AlGaN/GaN HEMTs for the first time. Effect of MESA isolation and gate finger on the ESD behavior of HEMTs is analyzed. Effect of pulse width on ESD robustness and trigger voltage is observed and a unique power law like behavior is found. Cumulative nature of device degradation under ESD stress condition is discovered.

Correlation between depth of snapback and failure threshold with % device degradation is found. Finally, impact of inverse piezoelectric effect in AlGaN/GaN system, fringing electric field, role of contact resistivity, temperature and field induced contact metal migration and premature breakdown of parasitic MESA Schottky junction are studied in context to AlGaN/GaN HEMT failure ESD conditions.

**EL-8 New Insights on the ESD Behavior and Failure Mechanism of Multi Wall CNTs**

A. Mishra, M. Shrivastava, Indian Institute of Science

ESD conditions, through inner and outer shells of MWCNT is explored. ESD time scale current annealing behavior of outer and inner shells was discovered, which is unique to MWCNTs. Shells – by – shell failure was confirmed to be the universal failure mode of MWCNTs. Failure behaviors of suspended and collapsed (tubes resting on dielectric surface) tubes in single and bundled configuration are discussed.

# System Reliability

## System Reliability

**ES-1 Long-Term Reliability of a Hard-Switched Boost Power Processing Unit utilizing SiC Power MOSFETs**

S. Ikpe, J.-M. Lauenstein, G. Carr*, D. Hunter*, L. Ludwig, W. Wood, C. Iannello, L. Del Castillo*, F. Fitzpatrick, M. Mojarradi, Y. Chen, NASA, *Jet Propulsion Laboratory California Institute of Technology

With the expedient maturation of Silicon-Carbide (SiC) device technology, a great deal of interest has been generated in the development of switching power applications capable of harnessing the inherent wide-bandgap (WBG) properties of the material. SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) in particular, offer significant benefit over their Silicon counterparts. The potential for lower total switching losses, higher breakdown field tolerance and superior thermal performance make SiC devices highly attractive for both high temperature and extreme environment applications. Though successful power conversion implementations show promise [1], these noteworthy device innovations have yet to directly translate into pragmatic power conversion systems. Therefore, it is still necessary to evaluate the application-specific performance of these devices to fully understand thermal limitations as well as estimate the overall device reliability. This paper describes a design-for-reliability approach for an innovative power processing architecture intended for in-space solar electric propulsion (SEP) systems. The work herein also presents reliability data on CREE's commercially available N-channel enhancement mode SiC MOSFETs.

# Failure Analysis

## Failure Analysis

### FA-1 Dynamic Avalanche in Charge-Compensation MOSFETs Analyzed with the Novel Single Pulse EMMI-TLP Method

T. Chirila, T. Reimann*, M. Rüb, University of Applied Science Jena, *Technische Universität Ilmenau

As a main switch in a broad range of applications, the Charge-Compensation MOS Transistor must be able to withstand the avalanche multiplication regime. Using the classical rating method for avalanche robustness, two destruction limits have been identified – thermal and current limit. However, up to date there is no complete understanding of current induced failure mechanisms. In this paper we combine single transmission line pulses with emission microscopy in order to bring more insight into these kinds of destruction modes. We identify three different avalanche regimes and observe the occurrence of current filaments. We provide an interpretation for filament formation.

### FA-2 Fast 3D Electro-Optical Frequency Mapping and Probing in Frequency Domain

K. Melendez*, K. Sanchez*, P. Perdu*, K. Melendez, D. Lewis, Bordeaux University, *CNES

The main goal of this paper is to show the capability of extracting several frequencies at one electro-optical scanning
in order to reconstruct few 512 by 5 12 pixels images. With these 3D data (X and Y are pixels and Z is the frequency locked), it is possible to study several frequencies in one time and to reconstruct the original signal waveform at each pixel.

### FA-3 Direct Photo Emission Monitoring for High Power IGBT during Avalanche Operation

T. Matsudai, K. Endo, T. Ogura, T. Matsumoto*, K. Uchiyama*, K. Koshikawa*, Toshiba Corporation, *Hamamatsu Photonics K.K.

IGBTs have been developed extensively to improve trade-off relation between on state losses and switching losses. Therefore the reliability enhancement of IGBTs is very important technology. For the past failure analyses, only the final destruction point have been observed under testing. With this way, it is difficult to perform physical analysis, because the process of the destruction phenomenon is unknown. In this work, our target is investigating the avalanche phenomenon of IGBTs, directly. During avalanche operation, it is well known that the formation of current filament appears and visible light is emitted in the device. For the first time, we have succeeded observing the photo emission directly

from avalanche phenomena under UIS (Unclamped Inductive Switching) condition of IGBTs using the streak camera. We have also measured moving the emission region in edge termination area.

# Interconnect Metallization Reliability

## Interconnect Metallization Reliability

### IT-1 Optimizing Cu Barrier Thickness for Interconnects Performance, Reliability and Yield

T. Shen, B. Rajagopalan, M.C. Silvestre, E. Ramanathan, A.S Mahalingham, W. Zhang, K.B. Yeap, P. Justison, Globalfoundries

Cu barrier thickness optimization on our 90nm pitch Vx/Mx layers with porous ULK SiCOH (κ=2.55) was systematically investigated. Both via resistance and intrinsic EM performance favors thinner TaN and Ta films, however, the robustness of the plating requires thicker Ta to improve seed quality that withstand dissolution during plating. Overall, a thin TaN barrier with moderate thick Ta provides the optimum solution for performance, reliability and yield.

### IT-2 Semi-empirical Interconnect Resistance Model for Advanced Technology Nodes: A Model Apt for Materials Selection Based upon Test Line Resistance Measurements

P. Roussel, I. Ciofi, R. Degraeve, V. Vega, N. Jourdan, R. Baert, D. Linten, J. Bömmels, Z. Tőkei, G. Groeseneken*, A. Thean, IMEC, *KU Leuven

As the dimensions of interconnects shrink into the nanoscale for the NX node, their electrical conductivity becomes dependent on their size, even at room temperature. This paper presents a semi-empirical interconnect resistance model apt for fitting wire resistance data. The model combines grain boundary and sidewall scattering effects with the impact of Line Edge Roughness (LER). It allows subsequent selection of interconnect metallization material candidates through extrapolation to target widths of future technology nodes on the basis of their wire resistance, while still considering other performance metrics like yield, electromigration and TDDB. A refined model parameter calibration procedure, that accounts for interconnect height and width variability between the test structures is demonstrated for two Cu metallization schemes, employing Co and Ru as a metal liner, respectively. The model allows inclusion of more accurate, geometry dependent interconnect resistance estimators in higher abstraction level simulators, enabling a more realistic assessment of the impact of BEOL parasitics on circuit delay at advanced technology nodes.

### IT-3 Electromigration: Multiphysics Model and Experimental Calibration

G. Marti, W.H. Zisser, L. Arnaud*, Y. Wouters**, STMicroelectronics, *CEA-Leti Minatec, **SIMAP, ***Technische Universität Wien

Electromigration (EM) is one of the main reliability failure mechanism of integrated circuit interconnects. The result of EM in copper interconnects is void nucleation and growth close to the cathode. For EM tests, most commonly elementary structures are stressed under accelerated conditions (high current and temperature) until degradation occurs. The understanding of the main mechanism governing the reliability of copper interconnects is mandatory to develop lifetime predictive laws and allows architecture optimizations of future MOS technologies. Thus more accurate and less pessimistic full-chip EM assessment and mean-time-to-failure (MTTF) prediction will require a development of new methods that deal with the design of the grid structure and take redundancy into account. We describe in this work a new methodology to calibrate an existing EM numerical model. The effective charge (Z*) of this technology has been extracted experimentally. Furthermore, the proposed post-processing method allowed us to find the critical tensile stress of void nucleation. This method allows to answer design requests about void nucleation which may depend upon geometry and process conditions. Taking into account these parameters will increase the accuracy of reliability prediction at design level and help designers with high current density needs.

# Memory

## Memory

### MY-1 The Complete Time/Temperature Dependence of I-V drift in PCM Devices

M. Le Gallo, A. Sebastian, D. Krebs, M. Stanisavljevic, E. Eleftheriou, IBM Research – Zurich

Phase-change memory (PCM) devices are expected to play a key role in future computing systems as both memory and computing elements. Hence, a comprehensive understanding of the change in the current/voltage (I-V) characteristics of these devices with time and temperature is of considerable importance. Here, we present a unified drift model to predict the I-V characteristics at any instance in time and at any temperature. The model was validated on large sets of experimental data for an extensive range of time (10 orders of magnitude) and temperatures (180 – 400 K), different phase-change materials and a collection of 4k cells from a PCM chip.

### MY-2 Reliability-Performance Tradeoff between 2.5D and 3D-Stacked DRAM Processors

S.M Hassan, W. Song, S. Mukopadhyay, S. Yalamanchili, Georgia Institute of Technology

MY-3 Root cause of degradation in novel HfO2-based Ferroelectric Memories M. Pešić, F. Fengler, S. Slesazeck, U. Schröder, T. Mikolajick, L. Larcher*, A. Padovani*, NaMLab gGmbH,

*University of Modena and Reggio Emilia Summary:HfO2-based ferroelectrics reveal full scalability and CMOS integrability compared to perovskite-based ferroelectrics that are currently used in non-volatile ferroelectric random access memories (FeRAMs). Up to now, the mechanisms responsible for the decrease of the memory window have not been revealed. Thus, the main scope of this study is an identification of the root cause for the endurance degradation. Utilizing trap density spectroscopy for examining defect evolution with cycling of the device studied together with modeling of the degradation resulted in an understanding of the main mechanisms responsible for degradation of the ferroelectric behavior.

**MY- 3 Root Cause of Degradation in Novel HfO2-based Ferroelectric Memories**

Milan Pešić, Franz P. G. Fengler, Stefan Slesazeck, Uwe Schroeder, Thomas Mikolajick*
NaMLab gGmbH

HfO2-based ferroelectrics reveal full scalability and CMOS integratability compared to perovskite-based ferroelectrics that are currently used in non-volatile ferroelectric random access memories (FeRAMs). Up to now, the mechanisms responsible for the decrease of the memory window have not been revealed. Thus, the main scope of this study is an identification of the root causes for the endurance degradation. Utilizing trap density spectroscopy for examining defect evolution with cycling of the device studied together with modeling of the degradation resulted in an understanding of the main mechanisms responsible for degradation of the ferroelectric behavior.

**MY- 4 Voltage Acceleration and Pulse Dependence of Barrier Breakdown in MgO Based Magnetic Tunnel Junctions**

S. Van Beek, K. Martens, P. Roussel, G. Donadio, J. Swerts, S. Mertens, A. Thean, G. Kar, A. Furnemont*, G. Groeseneken, KU Leuven, *IMEC

Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is a promising non-volatile memory for high speed applications. The Magnetic Tunnel Junction (MTJ), the key element, contains a thin crystalline MgO dielectric
sandwiched in between two ferromagnetic layers. One of these magnetic layers retains a magnetic memory state, that can be altered by nanosecond current pulses. The nanometer thin MgO dielectric should show sufficient reliability at used switching voltages. For DRAM applications 1000FIT is required. The lifetime prediction is largely influenced by a voltage acceleration model. For MgO there is no consensus about this acceleration model however. Moreover, large dependencies on pulse width and duty cycle are reported. In this paper we study barrier breakdown time over a range of 11 orders of magnitude. With a maximum likelihood ratio method, we test the statistical significance of fits for different voltage acceleration models on 855 devices. We find that the power law best describes voltage acceleration with a p-value less than 1e-10. In addition we observe no significant influence of duty cycle (1% – 77%) and pulse widths (10ns – 1us) down to 30ns.

**MY-5 A Compact Model for RRAM Including Random Telegraph Noise**

B.Guan, J. Li*, Sun Yat-sen University, *University of Wisconsin

Read instability in resistive random access memory (RRAM) devices, mainly caused by random telegraph noise (RTN), needs to be fully addressed before its wide commercial adoption. To fulfill the increasing need for circuit level reliability study, it is desirable to develop a compact model to account for RTN effect. In prior art, several analytical compact models have been developed to simulate resistive switching behavior . However, none of them are capable of capturing current fluctuation caused by RTN. In this paper, we develop a RRAM compact model for circuit simulation, which for the first time takes into account the RTN effect. The model is validated using different sets of experimental data. Our simulation fits well with measurements both in high resistance state (HRS) and low resistance state (LRS).

**MY-6 System-Level Error Correction by Read-Disturb Error Model of 1Xnm TLC NAND Flash Memory for Read-Intensive Enterprise Solid-State Drives (SSDs)**

Y. Deguchi, T. Tokutomi, K. Takeuchi, Chuo University

Read-disturb Modeled LDPC (RDM-LDPC) ECC is proposed. Conventional Advanced Error-Prediction LDPC (AEP-LDPC) corrects data-retention errors of data-storage-purpose SSDs storing photos, movies, etc. but cannot correct read-disturb errors. For read-intensive computing-purpose enterprise SSDs, this paper analyzes the read-disturb errors, develops the error model of 1Xnm TLC NAND Flash memory and proposes ECC suitable for read-disturb errors. It is experimentally demonstrated that proposed RDM-LDPC extends the read cycle of SSDs by 5000-times.

**MY-7 On the Variability of Threshold Voltage Window in Gate-Injection Versatile Memories with Sub-60mV/dec Subthreshold Swing and 1012-Cycling Endurance**

Y. Chiu, C. Cheng*, M.-H. Lee, C. Liu*, P.-W. Chen*, P.-C. Chen*, C. Chang, S.Yen, C. Fan, H. Hsu, G. Liou*, C. Chang, C. Liu*, W.-C. Chou*, National Chiao Tung University, *National Taiwan Normal University

Incorporating a charge-trapped ZrSiO with ferroelectric HfZrO dielectrics, we demonstrated a gate-injection versatile memory with sub-60mV/dec subthreshold swing (SS) and large threshold voltage window (ΔVT) of >2V under a fast 20-ns speed. Moreover, it is revealed that the local defects at ZrSiO/HfZrO interface affect the ferroelectric negative capacitance tuning and thus increases the variability of VT and SS during 1E12 cycling endurance.

**MY-8 Random Telegraph Noise in HfOx Resistive Random Access Memory: from Physics to Compact Modeling**

F.M. Puglisi, L. Larcher, P. Pavan, University of Modena and Reggio Emilia

As RRAM technology is entering the industrial phase, compact models accounting for variability and RTN effects at circuit level are essential to evaluate the technology potential. Variability and RTN represent major concerns for HfOx RRAM applications such as non-volatile memory, neuromorphic computing, and Physical Unclonable Function (PUF). In this paper, starting from the physics of charge transport and RTN, we develop a physics-based compact model for RTN in RRAM, valid in both high-(HRS) and low-resistance state (LRS). The proposed model is validated on a wide data set and well reproduces also data from the literature. The RTN model can be easily integrated in compact RRAM device models and can describe I-time traces in both resistive states.

# Packaging and 3D Assembly

## Packaging and 3D Assembly

### PA-1 Optimum Filler Geometry for Suppression of Moisture Diffusion in Molding Compounds

W. Ahn, S, Shin, R. Asadpour, L. Nguyen*, D. Varghese*, S. Krishnan*, M. Alam, Purdue University, *Texas Instruments

Inorganic fillers, such as fused silica or organic clay, help tailor/co-optimize the mechanical toughness, thermal conductivity, and moisture diffusivity of polymer mold compounds used to package microelectronic integrated circuits. Despite long history and wide-spread current use, the optimization of filler-infused composites is generally empirical and therefore time-consuming. A physics-based predictive modeling will improve application-specific design of composites that would offer optimum performance and reliability. As an illustrative example, in this paper, we develop a general theory of polymer composites that anticipates the suppression of moisture diffusion as a function of fill-fraction, size-dispersion, shape, and topology of filler nanoparticles. Our results show that the best performance is obtained by incorporation rod-shaped fillers, randomly closed packed at maximum density (~60%). Our numerical results are succinctly captured by the analytical model based on generalized Maxwell Garnett effective medium theory. The analytical model can be used for initial optimization of mold compounds before large-scale numerical modeling is invoked and characterization experiments are designed.

### PA-2 A Finite Element Method Study of Delamination at the Interface of the TSV Interconnects

S. Papaleo, H. Ceric, TU Wien

Through Silicon Vias (TSVs) are the interconnections in three dimensional integrated circuits responsible for the vertical lines inside the dies. In particular, the open TSV has been developed in order to reduce thermo-mechanical issues. This interconnect structure has interfaces where the possibility of a device failure due to delamination needs to be

considered. The Critical Energy Release Rate Gc determines the condition for a fracture to propagate. When the Energy Release Rate G exceeds Gc, a fracture will propagate. Experimental measurements were used to calculate Gc. The experimental Gc, was calculated at the interface between silicon dioxide and tungsten; materials used for Open TSVs. We have developed a model to calculate the G and compared the experimental data with our results. The results obtained are in good agreement with experimental measurements. Therefore, the model developed provides a convenient tool for the study of delamination issues in TSVs.

**PA-3 Electromigration Induced Thermomigration in Microbumps by Thermal Cross-talk Across Neighboring Chip in 2.5D IC**

M. Li, D.W. Kim*, S. Gu*, K.-N. Tu, University of California, Los Angeles, *Qualcomm

This paper investigates the thermal cross-talk between the powered microbumps under one chip and the unpowered microbumps under the neighboring chip. Both chips were on a Si interposer for 2.5D IC. The Joule heating from the powered chip was found to be transferred laterally along the interposer to the unpowered chip and produced a temperature gradient in the microbumps in the unpowered chip. Void formation is observed in both the powered and the unpowered microbumps. The latter is due to thermomigration (TM), and the former is due to electromigration (EM). The amount of voids is bigger by TM than by EM. The void nucleation and growing is studied by examining the un-powered microbumps at different stages during electromigration tests. The nucleation of voids at the cold end in TM is observed, which indicates that Sn atoms diffuse from cold end to hot end. The current-enhanced surface electromigration of Sn along the side walls of Cu pillars to form intermetallic compound is observed in the powered microbumps that were subjected to a 5.3×104 A/cm2 current density at 150 °C for a period of time. The depletion of Sn will cause serious void formation in these powered microbumps.

# Process Integration

## Process Integration

**PI-1 Resolution of Poly Gate to Substrate Contact Short Reliability Failures on Non-Volatile Memory**

S. Chandrasekaran, P. Jowett, T. Mishra, C. Shafer, R. Cruz, K. Noronha, S. Bhosle, V. R. Sanivarapu, N. Rangaraju*, D. Kapoor*, Intel Micron Flash Technologies LLC, *Intel Corporation

Due to continual scaling of CMOS device dimensions, the dielectric spacing between poly gate (PG) and contact to substrate (Con) has been drastically reduced. This reduction in gate to substrate contact spacing has challenged the dielectric breakdown between poly

gate and substrate contact. Several studies involving the breakdown of dielectric between gate and substrate contact have been reported in the past. In this paper, we report the elimination of poly gate to substrate contact shorts on 90 nm Non-Volatile Memory technology with the help of process optimizations in pre-metal dielectric stack. This led to a significant improvement in wafer level reliability metric to the tune of ~1.7X.

**PI-2 Highly-Accelerated WLR Learning Cycles for Development of a Trench MOSFET: Method and Case Study**

G. Hall, D. Moore, P. Burke, M. Suzuki, ON Semiconductor

ON Semiconductor Trench MOSFET integration process is designed to be manufacturable with high yields and world-class reliability. Power MOSFET discrete devices are required to pass a number of packaged level reliability (PLR) tests based on IEC guidelines [1], which involve very long time horizons -e.g. High Temperature Gate Bias (HTGB), and Reverse Bias (HTRB) have 1000+ hour time-on-test. When developing a new integration or design, it is of high value to have an expedient methodology for providing fast results on design-of-experiments (DOE), which lead to process or design paths with a high likelihood of passing qualification. In this study we describe the use of WLR methodology to identify an optimized Trench MOSFET gate salicidation scheme. The DOE splits were evaluated using a highly accelerated wafer level bias temperature instability test (WLBTI), and Wafer Level Time Dependent Dielectric Breakdown (WLTDDB). The process conditions which had acceleration factors predicting optimal results at PLR and use conditions were selected for qualification using the standard PLR program. The business case for using WLR methodology to evaluate cycles of learning is clear when one considers the impact to time-to-market of innovative technologies.

# Product IC Reliability

## Product IC Reliability

**PR-1 Modelling of 1T-NOR Flash Operations for Consumption Optimization and Reliability Investigation**

J. Coignus, G. Torrente*, A. Vernhet, S. Renard*, D. Roy*, G. Reimbold, CEA, LETI, *STMicroelectronics

Based on novel experimental capabilities, Flash NOR memory consumption, scalability and reliability trade-off is addressed, by mean of programming and erase operation schemes modelling. A fine tuning of programming energy and max. current is provided, together with an extended description of Flash programming dynamics along device ageing. Optimized cycling conditions are shown to reduce power consumption without any detrimental impact on device reliability.

**PR-2 Near Neighbor Sort Yield & Wafer Sort Yield Impact on Product Burn-In and a Time-Dependent Reliability Study**

R. Heller, Jr., Advanced Micro Devices

Local Yield is the yield of near neighbor die to a central die at wafer sort (excluding the results of the central die). It has been shown in literature that the local yield of a die can estimate the future reliability of the die. Die that come
from regions of other passing die pose less reliability risks than faulty regions. This is due to defect clustering and the fact that same killer defects that cause sort fails are the same types of defects that cause latent defects only differing in size and location. Based on information we can gather at Wafer Sort, does it make sense to have a "one size fits all" approach for a downstream production burn-in screen? What techniques can we use to better identify potentially unreliable die? Can we use Local Yield and Wafer Sort Yield to better determine burn-in durations? This paper examines all of these questions and the relationship between yield and reliability using both Local Yield and Wafer Sort Yield and production burn-in using a production dataset of AMD CPU. This paper also examines the time-dependent reliability fallout during production burn-in by near neighbor sort bin.

**PR-3 Machine Learning-Based Proactive Data Retention Error Screening in 1Xnm TLC NAND Flash**

Y. Nakamura, T. Iwasaki, K. Takeuchi, Chuo University

A screening method to proactively reduce data retention error, based on screening of PD-weak cells, where PD-weak cells have high program disturb error frequency. Repeated measurement of program disturb (P.D.), indicates that 25% of P.D. errors are concentrated in 3.5% of the memory cells, called PD-weak cells. PD-weak cells have 4× worse data retention (D.R.) than non- PD-weak cells, therefore retention errors can be reduced by PD-weak cell screening. Proactive D.R. detection is a new capability, because conventional retention testing times are not practical during product test. In 1Xnm TLC NAND flash, removal of PD-weak cells with <2% overhead extends D.R. by 30%. The method to measure PD-weak cells is described, as well as machine learning to model and detect PD-weak cells. Finally, detection rate vs. false detection cost is compared for 3 learning algorithms.

# Photovoltaics Reliability

## Photovoltaics Reliability

**PV-1 Study of the Potential-Induced Degradation Kinetics**

J. Bengoechea, M. Ezquer, J. Diaz, A.R. Lagunas, National Renewable Energy Centre

A dedicated set-up which allows a real-time characterization of the PV modules, while being subjected to the Potential-Induced Degradation (PID) test, was developed and tested. This real-time characterization includes the measurement
of the dark I/V curve and the acquisition of electroluminescence (EL) images at different biasing levels. By means of this realtime characterization it is possible to early identify the PID presence and its kinetics during the total duration of the test.This set-up allowed the investigation of the influence of salt as an impurity in module packaging with regard to PID. To this aim, a mini-module contaminated with salt including on the surface of one of its solar cells and in the glass-EVA interface was laminated. This mini-module showed an increased susceptibility to PID, which developed also in the uncontaminated solar cells. Repetitions of the PID test showed that its influence diminished with the number of cycles.

**PV-2 Potential Induced Degradation in High-Efficiency Bifacial Solar Cells**

M. Barbato, M. Meneghini, A. Cester, A. Barbato, G. Tavernaro*, M. Rossetto*, G. Meneghesso, University of Padova, *MegaCell S.r.l.

This paper presents an analysis of the degradation of Bifacial Solar Cells submitted to potential induced degradation (PID) stress. We report the results obtained on cells with two different encapsulation materials: ethylene-vinyl-acetate (EVA) and polyolefin elastomer (POE). Results show that the use of different encapsulation materials may result in a better robustness towards PID in Bifacial Solar Cells.

**PV-3 Improvement of DSSC Performance by Voltage Stress Application**

A.Scuto, G. Di Marco*, G. Calogero*, I. Citro*, F. Principato**, C. Chiappara**, S. Lombardo,, CNR IMM, *CNR IPCF, ** Università degli Studi di Palermo

Dye-sensitized solar cells (DSSCs) are promising third generation photovoltaic devices given their potential low cost and high efficiency. Some factors still affect DSSCs performance, such structure of electrodes, electrolyte compositions, nature of the sensitizers, issues of power conversion efficiency and stability under prolonged electrical cycles, etc. In this work we discuss the effect of electrical stresses, which allow to improve DSSC performance. We have investigated the outcomes of forward and reverse DC bias stress as a function of time, voltage, and illumination level in the DSSCs sensitized with the N719, Ruthenium complex based dye. We demonstrate that all the major solar cell parameters, i.e., open circuit voltage (VOC), short circuit current (ISC), series resistance (ROC), fill factor (FF), and power conversion efficiency are strongly influenced by the stress conditions and a clear reversibility of the parameters on the stress type is shown. In this context we examined the possible effects that emerge from the electrolyte composition. Our study suggests that under proper biasing the DSSCs noticeably improve in terms of efficiency and long-term stability.

**PV-4 Adhesion Requirements for Photovoltaic Modules of Polymeric Encapsulation**

J. Zhu, G. Surier, D. Wu, D. Montiel-Chicharro, T. Betts, R. Gottschalg, Longborough University

This paper addresses the delamination issue and investigates the adhesion requirement and failure of packaging material at the different interfaces. Lamination condition has significant impacts on the adhesion stability and failure modes, which will be further investigated too.

# Soft Errors

## Soft Errors

### SE-1 Alpha-Particle and Neutron-Induced Single-Event Transient Measurements in Subthreshold Circuits

M. Gadlage, J. Albhin*, P. Gadfort**, S. Stansberry***, A. Roach, A. Duncan, M. Kay, NSWC Crane, *MDA, **Army Reseach Lab, ***USC-ISI

Experimental data from alpha particle testing are dis-cussed and analyzed from a sub-threshold voltage SET characterization circuit. Using a Schmitt trigger inverter target chain fabricated in a 28-nm bulk CMOS process, SET pulse widths are captured from an operating voltage down to 0.32 V. These results show that alpha particles can induce SET pulse widths that range up to hundreds of nanoseconds when operating at voltages well below the nominal voltage. Additionally, the alpha particle results show that sub-Vt circuits are significantly more susceptible, as compared to circuits operating at nominal voltages, to low-energy particles inducing SETs that have a high probability of being latched as errors in a combinatorial logic design.

### SE-2 Error Characterization and Mitigation for 16nm MLC NAND Flash Memory under Total Ionizing Dose Effect

Y. Li, D. Sheldon*, A. Ramos, J. Bruck, California Institute of Technology, *NASA Jet Propulsion Laboratory

This paper investigates the system-level reliability that 16nm MLC NAND flash can offer to SSDs under total ionizing effect for storage in space. Measurements show that blocks that carried less than 3k program/erase cycles (PECs) only survived up to 10k rad total doses under the protection of standard ECCs. We characterize errors at the levels of threshold voltage Vt, cell logical state, and binary bit, respectively, and study error mitigation schemes for reliability enhancement. We adopt a novel data representation where data are read using the relative order of cell voltages.
Experimental results show that the new representation reduced bit errors by 60% on average. We propose a new memory scrubbing (MS) scheme that refreshes cells without block erasure and operates under lower voltage. Measurements show that flash blocks

survived up to 8k PECs and 57k rad total doses using the new scrubbing scheme. Both schemes were implemented as parts of a flash controller, and significantly outperform existing methods in various aspects.

**SE-3 Investigating the Single-Event-Transient Sensitivity of 65 nm Clock Trees with Heavy Ion Irradiation and Monte-Carlo Simulation**

V. Malherbe, G. Gasiot, S. Clerc, F. Abouzeid, J.-L. Autran*, P. Roche, STMicroelectronics, *Aix-Marseille Université

We present a study of single-event transients in clock tree structures in 65 nm bulk silicon technology. Shift registers are irradiated with heavy ions over a large range of linear energy transfers representative of both terrestrial and space environments. By attributing large error clusters in the flip-flop shifters to clock tree events, we derive experimental cross sections for the clock tree cells. Monte-Carlo irradiation simulations performed on the same structures are in good agreement with these data, allowing to assess the radiation robustness of other clock-tree configurations.

**SE-4 Exploiting Low Power Circuit Topologies for Soft Error Mitigation**

N. Mahatme, S. Jagannathan, N. Gaspard,III*, B. Bhuva**, S. Wen***, R. Wong***, I. Chatterjee^, T. Assis**, NXP Semiconductor, *Altera Corporation, **Vanderbilt University, ***Cisco, ^University of Bristol

Alpha particle experimental results for arithmetic circuits implemented using transmission gate logic in 20-nm bulk technology node are shown to have 35% lower soft error rate as well as 30% lower power consumption compared to standard CMOS circuits. Analytical models confirm the experimental trends and help optimize and predict the power-SER trade-off.

**SE-5 Estimation of Single-Event Transient Pulse Characteristics for Predictive Analysis**

T. Assis, J. Kauppila, B. Bhuva, R. Schrimpf, L. Massengill, R. Wong*, S. Wen*, Vanderbilt University, *Cisco

Estimate the Single Event Transient (SET) pulse width of standard cells is challenge task requiring hundreds of spice simulations for the library characterization. In this work analytical models are used to estimate the SET pulse width for multiple standard cells considering both different hit node locations and charge sharing. By using the Ambipolar-Diffusion-Cutoff (ADC) model extension this methodology is also able to properly model the SET Pulse Quenching effect. The model requires a simple characterization step performed only once for 3 simple circuits. Comparison with electrical simulations (SPICE) for 4 technologies shows great model accuracy. Heavy ion experiments in a 65nm bulk technology Test Chip also show good accuracy. The simple model formulation and low

computational requirements make this methodology ideal to be used by Electronic Design Automation (EDA) tools.

**SE-6 Predicting the Vulnerability of Memories to Muon-Induced SEUs with Low-Energy Proton Tests Informed by Monte-Carlo Simulations**

J. Trippe, R. Reed, B. Narasimham*, B. Sierawski, R. Weller, R. Austin, L. Massengill, B. Bhuva, K. Warren, Vanderbilt University, *Broadcom Corporation

Low-energy terrestrial muons have been shown to induce single-event upsets (SEUs) in complementary metal-oxide semiconductor (CMOS) static random access memories (SRAM). Only a handful of facilities produce surface muon beams, and these facilities have limited access to muon beamtime. As a result, it is difficult to carry out experiments to evaluate and/or characterize vulnerability to muons. To address the lack of muon beam availability, this work presents a method for determining a design's vulnerability to muon-induced upsets by performing tests at a readily available, low energy proton facility. It is shown that low-energy protons have similar characteristics as muons for soft error effects. This will allow test engineers to use proton test results to determine if a device is vulnerable to muon induced upsets.

# Transistor Reliability

## Transistor Reliability

**XT-1 Alteration of Oxide-Trap Switching Activity at Operating Condition By Voltage-Accelerated Stressing**

Z.Y.Tung, D.S. Ang, Nanyang Technological University

It is found that voltage-accelerated stressing can change the switching activity of a time-zero oxide defect measured under operating condition. The defect can be rendered either less active or more active by the applied stress, implying a possible modification of its atomic structure. With the impact of oxide trapping on MOSFET channel conduction becoming increasingly important as device dimension decreases, the observed stress-induced alteration of trap-switching behavior under operating condition should be a consideration in the reliability assessment of small-area devices.

**XT-2 Nano-Scale Evidence for the Superior Reliability of SiGe High-k pMOSFETs**

M. Waltl, A. Grill, G. Rzepa, W. Goes, J. Franco*, B. Kaczer*, J. Mitard*, T. Grasser, TU Wien, *imec

It has recently been demonstrated that the susceptibility of conventional Si channel pMOSFETs to the negative bias temperature instability (NBTI) is a serious threat to further

scaling. One possible solution to this problem is the use of SiGe quantum-well devices, which not only offer high mobilities but also superior NBTI reliability. It has been speculated that the latter is due to the band offset of the SiGe channel with respect to Si, which increases the energetic separation between the defect bands in the high-k gate stack and the channel. We investigate this claim by comparing single-defects in nano-scale devices to the behavior of the large number of defects visible in large-area devices. Using detailed TCAD simulations we determine the energetic and spatial locations of the traps in the gate stack and confirm that the previously developed picture correctly explains the significant reliability benefits of SiGe channel devices.

**XT-3 Negative Bias Temperature Instability Lifetime Prediction: Considering Frequency, Voltage and Activation Energy via Novel Methodology of MSM-SFMF**

C.H. Chiang, N. Ke, S. N. Kuo, C. J. Wang, K. C. Su, United Microelectronics Corporation

The reliability of pMOSFETs is limited by NBTI. Recent NBTI studies for aggressive scaling CMOS technology found the recoverable component. According to the present observation, the recoverable component is contributed by hole trapping while the permanent component is explained by the creation of interface. It implies that NBTI results from two tightly coupled mechanisms. This paper discusses a new measuring skill that helps us to realize characteristic of traps via frequency, voltage and temperature [4]. After considering activation energy (Ea), traps can be divided into three types. It includes simple concept of Reaction-Diffusion (RD) and two-stage models, and doesn't need complicated mathematics operations. Consequently, it benefits the study of transistor NBTI behavior.

**XT-4 Device-Level Jitter as a Probe of Ultrafast Traps in High-k MOSFETs**

D. Veksler, J. Campbell, J. Zhong*, H. Zhu*, C. Zhao*, K. Cheung, National Institute of Standards and Technology, *Chinese Academy of Sciences, *IMECAS

We developed the methodology to quantify ultra-fast interface traps using jitter measurements as a probe. This methodology was applied to study the effect of PBTI stress in high-k/Si MOSFET on density of fast interface traps (500ps to 5ns timescale). It was shown that increase of jitter of 2Gbt/s signal caused by stress is solely related to the degradation of a FET threshold voltage, while density of fast interface traps is not affected by PBTI stress. The developed methodology can be used for evaluation of the interface quality and quantification of fast interface traps in MOSFET and HEMT devices, built using different technologies and material systems. It can be used to study interface degradation induced by different type of stresses, including electric, thermal, and radiation effects.

**XT-5 Spatio-Temporal Mapping of Device Temperature due to Self-Heating in Sub-22nm Transistors**

M.A. Wahab, S. Shin, M.A. Alam, Purdue University

With the increase of transistor density and adoption of novel geometries, such as, FinFET, ETSOI, and gate-all-around (GAA) transistors, self-heating has emerged as a persistent concern for modern ICs. Various reliability issues, such as, NBTI, HCI, PBTI, and TDDB depend sensitively on channel temperature, ⟦ΔT⟧_C (x,y,z;t), due to self-heating. An accurate spatio-temporal map of channel temperature is essential for Fin-resolved reliability/lifetime of sub-22 nm technology nodes. In this paper, we demonstrate that (i) none of the existing techniques, in isolation, can map the Fin-resolved channel temperature of modern transistors, and (ii) only a collection of orthogonal techniques (multiprobe approach) or novel test structures (material approach), integrated/interpreted through self-consistent electro-thermal simulation, can map the temperature in sufficient detail necessary for reliability prediction.

**XT-6 Surface-Potential-Based Compact Modeling of BTI**

I.S. Esqueda, H. Barnaby*, University of Southern California, *Arizona State University

Characterization and modeling of bias temperature instability (BTI) is conventionally based on time-dependent shifts in threshold voltage (Vth) resulting from stress and relaxation conditions. Contributions of oxide near-interfacial (i.e., border) and interface traps are not independently captured in these conventional methods. By considering the effects of charge trapping dynamics on MOSFET operation, we present new techniques for characterizing and modeling the contributions of oxide and interface traps. Characterization is based on the rapid response of interface traps to high-frequency measurements of inverse subthreshold slope (S), for which slower oxide traps do not contribute, as their occupancy does not change at high frequencies. The modeling approach uses calculations of surface potential (ψs) to describe the distinct contributions of oxide and interface traps on BTI. Combined with capture/emission time maps, this approach describes BTI induced ΔS, and ΔVth stress/recovery characteristics.

**XT-7 Width and Layout Dependence of HC and PBTI Induced Degradation in HKMG nMOS Transistors**

N. Mahapatra*, P. Duhan, V. Rao, Indian Institute of Technology Bombay, *Indian Institute of Technology Gandhinagar

In this abstract, we have studied the width dependence of HC and PBTI induced degradation in HKMG nMOS transistors. It is clearly shown that the oxygen vacancies play a major role in the long term reliability of the HKMG nMOS transistors and this could be improved by dividing the active into multiple active fingers and by increasing the active-to-active spacing.

**XT-8 Characterization and Modeling of NBTI Permanent and Recoverable Components Variability**

D. Nouguier, X. Federspiel, G. Ghibaudo*, M. Rafik, D. Roy, STMicroelectronics, *University of Grenoble Alpes

In this paper we use a statistical analysis of NBTI recoverable and recoverable component measured on Pfet device issued from ST Microelectronics 28nm FDSOI technology. From measurement of NBTI degradation and recovery measured at µs time scale, resulting from AC and DC stress, we performed statistical analysis of the permanent and recoverable components and analyzed it separately. Accordingly, we proposed a Dual Defect Centric Model (DDCM) to account for differences of these two components.

**XT-9 Temperature Sense Effect in HCI Self-heating de convolution – Application to 28nm FDSOI**

X. Federspiel, G. Torrente, W. Arfaoui, V. Huard, F. Cacho, STMicroelectronics

Hot carrier injection (HCI) remained a major reliability concern for advanced CMOS nodes due to lateral field increase with device scaling but also due to increase of power dissipation [1,2,3,4]. HCI was reported as a wear-out mechanism that induces interface traps and oxide traps which cause in turn MOS device parameter drift. Parameter drift models were published to take into account lateral field, impact ionization, carrier energy distribution as well as local channel temperature. Recently, the need to deconvolute self-heating from HCI apparent voltage acceleration was pointed out to obtain accurate reliability modeling [5,6,7]. We will show here, that calculating temperature activation as if only depicting defect generation activation is an incomplete description of temperature dependency and that parameter drift temperature sensitivity factor must also be taken into account to correctly model HCI out. In the following, sense effect will refer to sensitivity of MOS parameter drift to temperature for a constant number of defect.

**XT-10 Comparative Experimental Analysis of Time-dependent Variability using a Transistor Test Array**

M. Simic, A. Subirats*, P. Weckx*, B. Kaczer*, J. Franco*, P. Roussel*, D. Linten*, A. Thean*, G. Groeseneken, G. Gielen, KU Leuven, *IMEC

As the transistors dimension reach the deca-nanometer scales, time-zero and time-dependent variability, which includes Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI), become a great concern for IC design. Accurate statistical models describing these two variability sources are necessary in order to design reliable circuits and systems. This paper gives insights in the geometry scaling of these variabilities and studies time-dependent variability through three different measurement techniques: the 2-point Measure-Stress-Measure, the Time Dependent Defect Spectroscopy, and the precise IdVg. Advantages and downsides of each technique are discussed.