



# 2017 IRPS Conference Proceedings



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# Intro

For years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world.



IRPS is Co-Sponsored by IEEE EDS and Reliability Society

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## Topics of Interest SPECIAL FOCUS TOPICS

IRPS17 is soliciting increased participation in the following areas: System reliability; Middle of Line; Extrinsic defect impact on yield and reliability; and COTS components in high-reliability applications – screening, derating, case studies, design considerations, etc.

### Circuits and Products and Systems

**Circuit Reliability** – Includes digital, mixed-signal, and RF applications; design for reliability

**Circuit Aging Simulation** – Includes compact modeling; statistical methods

**Product IC Reliability** – Includes burn-in; defect detection; on-chip sensors; modeling

**Consumer Electronics Reliability** – Includes smart phones; wearable devices; tablets; health devices Reliability Testing – Includes reliability equipment, tools, and test methods

**Electronic System Reliability** – Includes automotive, space, communications, medical, energy, and photovoltaic applications; screening techniques; system monitoring; failure root cause determination; modeling methodologies

**Soft Errors** – Includes neutron and alpha particle SER; multi-bit SER/SEU; mitigation techniques; simulation

**ESD and Latchup** – Includes component and system-level ESD design; modeling and simulation

**3D Assembly** – Includes multichip modules; 3D integration with TSV; thermomechanical stress; wafer thinning effects

**Packaging** – Includes chip-package interaction; fatigue; power dissipation issues

### Device, Process, and Materials

**Transistors** – Includes hot carrier phenomena; bias-temperature instability; random telegraph noise; advanced transistor scaling challenges; Ge and III-V channels

**Gate Dielectrics** – Includes TDDB modeling; reliability of novel gate dielectrics; modeling of progressive breakdown; gate dielectric reliability for III-V FETs

**Beyond CMOS Devices** – Includes reliability of tunnel FETs, transistors with 2D semiconductor (graphene, MoS<sub>2</sub>), and spintronics

**Wide Band-Gap** – Includes reliability of wide bandgap (GaN, SiC) power devices

**Back-End Reliability** – Includes Electromigration; Joule heating; stress migration; low-k dielectric breakdown; middle of the line processes

**Process Integration** – Includes new process related reliability issues; foundry reliability challenges

**Failure Analysis** – Includes evidence of new failure mechanisms; advances in failure analysis techniques

**Memory** – Includes DRAM and NVM; failure mechanisms in novel memory devices including 3D Flash and ReRAM

**Photovoltaic Devices** – Includes reliability of solar cell devices in silicon, CdTe, CIGS, etc.

**MEMS** – Reliability of New Structures. Sensors. Actuators. Reliability Testing. Analysis & Modeling

## Program

*NOTE – For full Program, including Abstracts and Speaker information, view Appendix*

*VIDEOS – <https://www.youtube.com/user/IEEEIRPS/videos>*

## Keynote Speakers

### First Keynote: Reflections on the risk of human space exploration – lessons learned from past failures

Dr. Nancy Currie-Gregg

NASA Astronaut; Principal Engineer, NASA Engineering and Safety Center

### Second Keynote: System Level Reliability Challenges with Technology Scaling

Mr. Ronald Newhart

IBM Distinguished Engineer, IBM Systems & Technology Group

## Tutorials

- Fundamental FEOL Reliability: Defect Generation in Gate Dielectrics to Induce Dielectric Breakdown and Device Degradation - Kenji Okada, TowerJazz Panasonic Semiconductor
- Compound Semiconductor Reliability 101 - Bill Roesch, Qorvo
- Interconnect Reliability Fundamentals - Zsolt Tokei, IMEC
- VLSI Design Methodology and Design Verification for Reliability - Michael Zaslavsky and Tim Turner, The Reliability Simulation Group
- Electromigration 101 - Cathy Christiansen, Global Foundries
- NAND Flash Memory Reliability - Hanmant Belgal and Ivan Kalastirsky, Intel
- Chip Package Interaction (CPI) and its Impacts on Reliability - CS Premachandran, Global Foundries
- Challenges for Failure Analysis - Automotive and More-Than-Moore - Ulrike Ganesh, Bosch
- 1. Recent Advances in NBTI in HKMG p-MOSFETs and 2. The Emerging Challenge of Self-Heating In Modern FINFET, ETSOI, and Gate-All-Around III-V Transistors: A Transistor to Tablet Perspective - Souvik Mahapatra (IIT, Bombay) and Muhammad Ashraf Alam (Purdue)
- The automotive transformation – cost, time-to-market, reliability and security driven design optimization from application down to semiconductor technology - Andreas Aal, Volkswagen AG
- AlGaN /GaN Power Device Reliability - Peter Moens, ON Semiconductor
- System Telemetry for Reliability Engineering - Rob Kwasnick, Intel
- Advanced MOL and BEOL Reliability - Shou Chung Lee, TSMC
- Introduction to Automotive Functional Safety – History, Trends, and Relation to Reliability - Karl Greb, NVIDIA
- Phase Change Memory: From Basic Technology to System Aspects and New Applications - Haris Pozidis, IBM
- System Reliability - Geny Gao, PhD
- Advanced Packaging and 3D Reliability - C. Raman Kothandaraman, IBM
- Juggling Knowledge Based and Standards Based Qualification - Bob Knoell, Automotive Electronics Council & NXP
- Spin Torque MRAM - Daniel C. Worledge, IBM
- Considerations for In-Field Fault Tolerance, Self-Healing, Detection & Recovery Techniques - Arijit Biswas, Intel

## Workshops

See Appendix – Full Program for Workshops

# Year In Review

See Appendix – Full Program for Workshops

## Panel Discussion

### Topics: Application Benchmarking, Systems and Architecture, Emerging Research Devices

Panel Moderator: Dr. William R. Tonti, Sr. Director, IEEE Future Directions

Biography: Dr. Tonti holds a BSEE from Northeastern University, an MSEE and a Ph.D. from the University of Vermont, and an MBA from St. Michael's College. He worked for over 30 years at IBM in the area of semiconductor technology research. Dr. Tonti holds in excess of 290 patents, and has been recognized as an IBM master inventor, and as one of the world's top patent family holders. His 250th patent has been transcribed into the U.S. Congressional Record. Dr. Tonti is a Fellow of the IEEE a past IEEE Reliability Society President, a recipient of the IEEE Reliability Engineer of the Year award, and the IEEE 3'rd Millennium medal. Dr. Tonti currently is a senior IEEE staff director leading its future technology directions. Dr. Tonti is a past IRPS and IRW General Chair.

Panelist: Dr. Geoffrey Burr, Principal Research Staff Member, IBM

#### Topic/Focus Group: Application Benchmarking

Abstract: One of the driving forces behind the evolution of ITRS (International Technology Roadmap for Semiconductors) into IRDS (International Roadmap for Devices and Systems) is the need to track both devices and systems. In the computer industry, "benchmarking" refers to the use of test programs that serve as proxies for user applications to estimate the performance of a computer system — past, present or future — on a given application domain. Within IRDS, the Applications Benchmarking (AB) International Focus Team seeks to identify key application drivers, to match these to the market drivers identified by the Systems and Architectures IFT, and then to track and roadmap system performance through relevant benchmarks. I will discuss how this connects to underlying device performance including reliability.

Biography: Geoffrey W. Burr received his Ph.D. in Electrical Engineering from the California Institute of Technology in 1996. Since that time, Dr. Burr has worked at IBM Research–Almaden in San Jose, California, where he is currently a Principal Research Staff Member. He has worked in a number of diverse areas, including holographic data storage, photon echoes, computational electromagnetics, nanophotonics, computational lithography, phase-change memory, storage class memory, and novel access devices based on Mixed-Ionic-Electronic-Conduction (MIEC) materials. Dr. Burr's current research interests include non-volatile memory and cognitive computing. An IEEE Senior Member, Geoff is also a member of MRS, SPIE, OSA, Tau Beta Pi, Eta Kappa Nu, and the Institute of Physics (IOP).

Panelist: Dr. Erik DeBenedictus, Sandia National Labs

#### Topic/Focus Group: Systems and Architecture

Abstract: Future architectures in IRDS. The ITRS->IRDS had narrowed the scope of Moore's 1965 paper to the microprocessor and DRAM memory. It is pretty clear that "Moore's law has ended" for code written for single core microprocessors. However, new architectures are in development/production that continue historical rates of progress provided that software can be rewritten. I'll describe the way new architectures can and will keep up the growth rate of Moore's law.

Biography: Ph. D. from Caltech 1983. Worked on parallel computers at Bell labs, finite element software at Ansoft corporation, parallel computers at nCUBE. Currently working on "Beyond Moore's law" research issues now at Sandia.

Panelist: Dr. Matthew Marinella, Principal Member of the Technical Staff, Sandia National Labs

#### Topic/Focus Group: Emerging Research Devices

Abstract: Low voltage logic switches and novel memory devices are the key building blocks for the next generation of computers. Using properties of these devices, such as low voltage digital and parallel analog operations will pave the way to several orders of magnitude improvement in key applications benchmarks like performance and features per watt. Research progress on the most promising emerging devices and how they will enable advanced computing have been tracked and assessed over many generations in the ITRS Emerging Research Devices Chapter, and this work continues as a core function of the IEEE International Roadmap for Devices and Systems Beyond CMOS Chapter.

Biography: Matthew Marinella is a Principal Member of the Technical Staff with Sandia National Labs. He leads several efforts focused on novel memory and neuromorphic computing, and is the Lead Scientist for Sandia's Beyond Moore Computing

Research Challenge. Dr. Marinella chairs the Emerging Memory Devices Section for the IRDS Roadmap Beyond CMOS Chapter and serves on the technical program committee for IEEE International Conference on Rebooting Computing. He received a PhD in electrical engineering from Arizona State University under Dieter Schroder in 2008.

## Poster Session

See Appendix – IRPS 2017 Full Program

## Technical Program

See Appendix – IRPS 2017 Full Program

## Exhibits & Exhibit Events

Exhibits are an integral part of the International Reliability Physics Symposium. Don't miss this opportunity to showcase your company's products and services.

**IRPS gratefully acknowledges the generous support  
of our 2021 exhibitors:**





## **Appendix – Abstracts, Bios & Technical Program**

## PREFACE

On behalf of the Management Committee of the IEEE International Reliability Physics Symposium (IRPS) and the IRPS Board of Directors, it is my pleasure to welcome you to the IRPS 2017. In its 55 years, IRPS has established itself as the world's premier conference in microelectronics reliability, and continues to attract engineers and scientists to present pioneering work in this field.

The 2017 technical program consists of 82 platform presentations, 79 poster presentations, and 17 invited talks from experts in key areas of microelectronics reliability. In addition, the symposium includes 20 tutorials, 3 Reliability Year-in-Review talks, 6 workshops, an equipment exhibit and a panel discussion with the panelists from the International Roadmap for Devices and Systems. There will be a lively poster reception on Wednesday and we are looking forward to seeing you along with your companions or family at this event. This year, the symposium has brought forward two new focus areas: reliability testing methods, and the use of Commercial Off the Shelf (COTS) components in high-reliability applications.

The symposium is the result of the dedication and tireless efforts of many individuals. I would like to thank all the authors, speakers, presenters, reviewers, panel contributors, workshop moderators, and exhibitors for making the symposium strong and successful. I also wish to thank my management committee, our consultants and the Board of Directors for their support.

Every year, we strive to organize a symposium that is technically strong while offering a great attendee experience. We look forward to your feedback so that we can continue to keep this symposium a great experience in future years.

Welcome to the symposium and I hope it will be a memorable experience for you!

Yuan Chen  
2017 IEEE IRPS General Chair

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*Widerkehr and Associates*

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## **Mark Your Calendar to Attend IRPS 2018!**

The 2018 IRPS will be held March 11-15 in South San Francisco, California, USA. A lively symposium is being planned, including keynote talks, poster session, tutorials, and a strong technical program.

Please consider submitting an abstract. Abstracts are solicited in all areas of microelectronics reliability, from the physics of device and materials wear-out to circuit and system design-for-reliability. Of special interest are works in the areas of WBG power devices, circuit aging, consumer electronics, 2D NAND Flash replacement technologies, and 2.5/3D packaging. Abstracts must be submitted by October 9, 2017.

Visit [irps.org](http://irps.org) for information regarding the abstract submission process or to register for the conference.

Feedback regarding the 2017 IRPS will allow us to plan a 2018 symposium that best meets its attendees' needs. Please complete the attendee surveys.

Elyse Rosenbaum  
2018 IEEE IRPS General Chair

Gaudenzio Meneghesso  
2018 IEEE IRPS Technical Program Chair

**Tuesday, April 4**

General Session  
Regency Main  
8:00 a.m.

**Keynote Talks**

8:30 a.m.

Keynote 1

**Reflections on the Risk of Human Space Exploration – Lessons Learned from Past Failures**, Nancy Currie-Gregg, NASA Astronaut; Principal Engineer, *NASA Engineering and Safety Center Safety*

9:15 a.m.,

Keynote 2

**System Level Reliability Challenges with Technology Scaling**, Ronald Newhart, IBM Distinguished Engineer, *IBM Systems & Technology Group*

**Panel Discussion**  
**1:10 p.m. - 2:00 p.m.**

**International Roadmap for Devices and Systems: [www.irds.ieee.org](http://www.irds.ieee.org)**

**Topics:** Application Benchmarking, Systems and Architecture, Emerging Research Devices

Panel Moderator: William R. Tonti, Sr. Director, IEEE Future Directions

*Panelists:*

Geoffrey Burr, Principal Research Staff Member, *IBM* - **Topic/Focus Group:** Application Benchmarking

Erik DeBenedictus, *Sandia National Labs*

**Topic/Focus Group:** Systems and Architecture

Matthew Marinella, Principal Member of the Technical Staff, *Sandia National Labs*

**Topic/Focus Group:** Emerging Research Devices

**Wednesday, April 5**  
**Poster Session and Reception**  
**6:30 pm – 9:30 pm - Monterey Ballroom**

## Sunday Tutorials

### Regency Main

#### **TS1.1 - Fundamental FEOL Reliability: Defect Generation in Gate Dielectrics to induce Dielectric Breakdown and Device Degradation** - *Kenji Okada, TowerJazz Panasonic Semiconductor (TPSCO)*

Reliability has been recognized as the showstopper of various kinds of *state-of-the-art* devices. To achieve further advance in various devices, both reliability and device performance must be well balanced at the extremely high levels. For this purpose, deeper understandings on the fundamental physics of various reliability items such as TDDDB, SILC, NBTI, PBTI, and HC are crucial as well as those on the device performances. In addition, appropriate methodologies for evaluation and for model parameter extraction must be employed in the predictions of lifetime and device degradation. For example, appropriate judgement of breakdown occurrence is quite difficult in ultrathin gate dielectrics due to the coexistence of large initial leakage current, large current noise, and so on. Thus, in case of TDDDB, both appropriate models and appropriate breakdown judgement are indispensable for accurate lifetime predictions. Therefore, in this tutorial, fundamental FEOL reliability items will be discussed with focusing on the defect generation in gate dielectrics under various use conditions along with appropriate models and methodologies.

#### **TS1.2 -Interconnect reliability fundamentals** - *Zsolt Tókei, imec*

Fundamentals of back-end-of-line (BEOL) dielectric and metal reliability will be presented. Different test methods, test structures, models and vehicles will be used for showcasing recent progress both for metals and dielectrics. Trends and methodology will be shown along with current and future reliability needs and concerns. In particular, we will review the usage of Internal Photoemission and Electron Spin Resonance techniques for BEOL dielectric defect characterization. Then diffusion mechanisms into low-k materials will be presented along with planar capacitor test vehicles on technology relevant dielectric layers. Damascene TDDDB and leakage mechanism studies will be used for illustrating technology relevant reliability testing. Next, mechanical stability, adhesion mechanisms, Chip Package Interaction (CPI) and Bump Assisted BEOL Stability Indentation (BABS) along with failure analysis will be presented. For metal reliability testing, besides the classical electromigration tests, specific attention will be paid to local sense structures that allow for analyzing interconnect reliability mechanisms in greater details. Other methodologies, such as drift velocity or high frequency measurements will also be mentioned to study the degradation and recovery mechanisms.

#### **TS1.3 - Electromigration 101** - *Cathy Christiansen, Global Foundries*

Electromigration (EM) is the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms. EM is one of the biggest reliability challenges for technology scaling, as the gap is widening between the required current density for design needs and the maximum current density that the metal interconnects can reliably carry. This tutorial will begin with the basics of EM and how to model it, including the physical mechanism of electromigration and copper diffusion, typical test structures and accelerated stress conditions, Black's model for extrapolation from stress to use conditions, and the short length effect. Failure time distribution statistics including lognormal, bimodal and three parameter fitting will also be discussed. An introduction will be given to characterization methods for low percentile failures and statistical EM budgeting. The second half of the tutorial will focus on the increasing challenges to electromigration with technology scaling and engineering improvements to combat them. The challenges include intrinsic trends of reduction in the critical void volume needed for failure and grain size reduction, as well as extrinsic variability and limitations in key processes such as reactive ion etch, liner/barrier/seed deposition, Cu plating and chemical mechanical polishing. Engineering improvements include better liner/barrier coverage, metal capping and alloy seed.

#### **TS1.4 - Chip Package Interaction (CPI) and its impacts on Reliability** - *CS Premachandran (Prem), Global Foundries*

Higher density, higher speed, lower power and more functions are always in high demand in the microelectronic industry. As the technology advances, the BEOL interconnect structure continues to evolve with decreasing dimensions and an increasing number of metal layers and this complexity will be a major reliability

concern for chips with low-k/ULK dielectric materials when they are integrated into high-density flip-chip packages. Moreover, mechanical properties of the dielectric materials deteriorate with increase in the porosity; raising serious concerns about the integration and reliability of Cu/low-k interconnect structural integrity. This tutorial discusses on Chip-Package Interaction (CPI), a growing concern in lower technology node reliability when using ultra-low-k porous dielectric materials. Also, discuss

on the thermal, mechanical interaction of interconnects such as C4 bumps, Cu pillar with the chip and different type of substrates, under fill, mold compound etc. that affect the stresses at the backend of line (BEOL) stacks and bump interconnects. FEA (Finite Element Analysis) simulations used to understand the CPI related failures will also be explained in this tutorial as well.

## **Regency I**

### **TS2.1 - Compound Semiconductor Reliability 101 - Bill Roesch, Qorvo**

This tutorial will examine the technology trends and reliability challenges for III-V devices. A bit of history is supplied, starting with references to Moore's Law and the Johnson Figure of Merit, which were both introduced in 1965. We will fast forward to the 80s and pick up on similarities and differences between silicon and the compounds with emphasis on the trends in materials and in reliability over the last 30 years.

Then the focus will shift to the emerging reliability challenges for Compound Semiconductors. We will look at learning what is most important by root cause failure analyses from artificially caused and naturally caused degradation. The unique GaAs mechanisms and their acceleration factors will round out the trend discussion.

In order to address emerging challenges, we will shift from wearout to defects and break down bygone separations between quality and reliability. Several types of defects and defect detection methods will be presented to show how the compounds have learned to shift focus to what's most important to customers regarding reliability.

### **TS2.2- VLSI design methodology and design verification for reliability - Michael Zaslavsky and Tim Turner, The Reliability Simulation Group**

The tutorial covers the main steps for reliability validation and assurance during the design of an IC. Methods and models will be presented for various failure mechanisms. We discuss how the software (EDA - Electronic Design Automation) tools are used, the basic modeling and analysis algorithms and provide examples.

The general IC design process is the sequence of steps, including circuit design, its simulation, and layout design and layout verification. Checking for different reliability phenomena requires analysis at different stages of the design. For example, transistor degradation can be estimated before and after the layout stage, while Electromigration analysis can be done only with a completed layout. The tutorial explains what data are required to

perform each reliability check, where and how one receives the data, and how the tools use it. We cover NBTI, Hot Carrier, ESD, Electromigration, TDDB and SER effects. The material should help the audience understand what results can be expected from design verification, what are the current challenges and how the methodologies can be optimized. We will also discuss limitations of current tools and techniques and the requirements for the future.

### **TS-2.3 - NAND Flash Memory Reliability - Hanmant Belgal and Ivan Kalastirsky, Intel**

This tutorial reviews the basic operations of NAND Flash memories and main reliability degradation mechanisms. These will be introduced using Floating-Gate 2D-NAND array. Primarily array reliability mechanisms such as endurance, disturbs and data retention will be described. A brief survey of current state-of-the-art NAND technologies, such as 3D-NAND, is also included. Implications to Solid-State Drive reliability are covered. Qualification methods and standards are also discussed.

### **TS2.4 - Challenges for Failure Analysis - Automotive and More-Than-Moore - Ulrike Ganesh, Bosch**

In this tutorial, the current (e.g. debug of analog circuits) and upcoming challenges of failure analysis labs in the automotive industry - particularly with its movement towards fully-automated driving - will be analyzed. In the second part of this tutorial, the challenges that failure analysis labs already face



while performing debug on small technology nodes (e.g. 16 nm) will be discussed. After that, a deep dive into future technology nodes (beyond 16 nm, More-Than-Moore) and the necessary development of tools and techniques in order to enable products for the market will show how important research and development for failure analysis is.

## Monday Tutorials

### Regency Main

#### **TM1.1a - Recent Advances in Negative Bias Temperature Instability (NBTI) in HKMG p-MOSFETs - Souvik Mahapatra, Indian Institute of Technology Bombay**

This presentation aims to accomplish two primary objectives. In the first part, we are going to discuss about the physical mechanism of NBTI. This has remained a topic of intense debate, and we will briefly review and compare different proposed mechanisms and models, and test their predictive capabilities

against experimental data. It is now well known that NBTI is due to interface trap generation and hole trapping in pre-existing traps. However, we will discuss whether these processes are mutually correlated or uncorrelated, review different methods to decompose measured data into these underlying components, and identify the dominant component that determines device lifetime. We will also evaluate different models for hole trapping, e.g., two well thermionic, two-well non-radiative multi-phonon, and extended non-radiative multi-phonon, as well as different models for interface trap generation, e.g., transient trap occupancy enabled reaction-diffusion, three energy well, and gate-sided hydrogen release (or dispersive reaction). The goal of this section is to identify the correct NBTI physical mechanism and model, which can explain measured data for wide range of experimental conditions.

In the second part, we will discuss the development and predictive capabilities of different NBTI simulators, which are based on the correct physical mechanism identified above. The first one is the 1-D BTI Analysis Tool (BAT), which can predict the time evolution of measured degradation during and after DC stress at different bias and temperature, during AC stress at different bias, temperature, frequency and duty cycle, and during multiple and arbitrary mixed DC-AC stress sequences under dynamic voltage, frequency and activity scaling. The simulator can predict measured data across device dimensions, explain the impact of HKMG process changes, and is compatible with both Si and SiGe channels. Next, implementation of the correct physical model in a commercial TCAD tool will be discussed. This enables accurate 3-D simulation of degradation in different device architectures and geometries, such as deeply scaled FinFETs and GAA NWFETs, where quantum confinement plays an important role. The impact of architecture, dimension and channel material on device lifetime will be accessed. Finally, we will discuss the development of a kinetic Monte Carlo process based stochastic simulator, which is based on the identified physical mechanism. We will demonstrate the consistency of the identified physical mechanism between large area deterministic and small area stochastic processes, and establish the equivalence of both these modeling frameworks.

#### **TM1.1b - The Emerging Challenge of Self-heating In Modern FINFET, ETSOI, and Gate-All-Around III-V Transistors: A Transistor to System Perspective - Muhammad A. Alam, Purdue University**

By early 2000s, many researchers would begin their talks with an iconic cartoon that superimposed the images of rocket nozzles and the sun, increasing power dissipation of an IC to the images of rocket nozzles and picture of the Sun. The message was difficult to ignore: the voltage-scaling kept power-dissipation at bay. Fast forward to 2015 – the tyranny of short channel effects at the sub 32 nm nodes has led to the development of FIGFET and ETSOI technologies, with gate-all-around III-V transistors in the horizon. The short channel effects are controlled, but at the expense of additional self-heating of the system. Stacks of materials (many poor thermal conductors) now surround the very hot channel to make the bad situation worse. In this tutorial, I will discuss the mapping the self-heating in 3D in surround gate transistors and how self-heating redefines and conflates the traditional notions of performance and reliability of ultrathin transistors and frontend and backend issues of modern ICs. The goal would be to connect the system to device perspectives to provide an end-to-end holistic view of the performance of self-heated integrated circuits.

### **TM1.2 - Advanced MOL and BEOL Reliability - Shou-Chung Lee, TSMC**

The reliability of BEOL dielectrics has become a critical issue for advanced technology development due to decreased dielectric failure times at sub-30 nm thickness of the Cu interconnect line-to-line- and via-to-line -spacing. Similar to the BEOL dielectrics, the MOL poly-to-contact spacer dielectric reliability is also becoming an important issue at the sub 20nm poly-to-contact spacing required in advanced nodes. Furthermore, accurate lifetime projection of BEOL and MOL dielectrics at circuit use conditions is becoming ever more difficult, as the BEOL via-to-line- and MOL poly-to-contact -spacing variations highly distort the intrinsic TDDB failure distributions under accelerated test conditions. In this tutorial, we will discuss all the technology scaling challenges for BEOL and MOL dielectric reliability and summarize recently proposed reliability methodologies in the industry, in order to accurately estimate dielectric reliability from acceleration testing data to circuit operation lifetime.

### **TM1.3 - Advanced Packaging and 3D Reliability - C. 'Raman' Kothandaraman, IBM Research**

Advanced packaging technologies, including 3D integration (3Di) are the key drivers for improved performance in the era of diminishing returns with traditional transistor scaling. Besides improving the power-performance characteristics of the system they also enable heterogeneous integration necessary for cost-sensitive consumer applications as well as performance intensive, novel applications such as MEMS and quantum computing. This tutorial will go in-depth into the principles of 3D integration with an emphasis on perturbations introduced into the platform technology and the methodologies necessary to quantify them.

## **Regency I**

### **TM2.1 - The automotive transformation – cost, time-to-market, reliability and security driven design optimization from application down to semiconductor technology - Andreas Aal, Volkswagen**

The car becomes the ultimate mobile device, a robot being guided by an IoT environment and by integrating step-by-step different levels of artificial intelligence. As being stated as a long-term vision/expectation one can infer that the corresponding and challenging implementation will come from a global electronic vendor rather from a vehicle manufacturer of the old days – a transformation is required. This tutorial will guide the participant through the changing automotive industry with both – the eyes of a semiconductor vendor as well its end customer. Starting with the automotive total quality management process, a detailed explanation of past and new approaches will be given not only from a formal, but rather from a technical level. Topics discussed will include the various definitions and differences between automotive and non-automotive semiconductor components w.r.t. pure environmental as well as functional perspectives. Corresponding dependencies to ECU design, vehicle design and services are discussed with context to ADAS, connected car, autonomous driving, IoT, semiconductor market dynamics and supply chain configurations. Requirements and solution proposals for new automotive semiconductor classes will be given and explained. A technology node dependent parallel application of a zero defect strategy with failure tolerant design, resilient design and replacement electronics (compatibility design) approaches will also be discussed. Semiconductor reliability in form of a DfX approach is the key enabler for electronic innovations of the automotive industry. However, beside defect caused fails, new technology inherent mechanisms under automotive loads pop up to limit automotive applicability.

### **TM2.3 - Introduction to Automotive Functional Safety – History, Trends, and Relation to Reliability - Karl Greb, NVIDIA**

Functional safety is an integral design aspect for automotive semiconductor developers, yet remains an area which few understand well. This tutorial will give the attendee an introduction to functional safety, starting with the historical concerns that created this field. We will review the pioneering work done in industrial applications which led to the development of the IEC 1508 basic safety standard as well as the challenges in IEC 61508 implementation which led the automotive industry to create ISO 26262. A deeper dive will be conducted into the requirements of the ISO 26262 standard, with special emphasis on the intersection of functional safety and reliability requirements including examples of base failure rate estimation and calculation of functional safety metrics. Finally, we'll look

towards the future and identify some of the key open topics that are shaping ISO 26262 2<sup>nd</sup> edition and beyond, including cybersecurity and Safety of the Intended Functionality (SOTIF).

## **Big Sur**

### **TM3.1 - AlGaN/GaN Power Device Reliability - Peter Moens, ON Semiconductor**

AlGaN/GaN power device technology has made tremendous progress over the past few years, and first commercial products are entering the market. The quality of the GaN MOCVD has reached a level that allows the fabrication of large area transistors with high yield and good reproducibility. Although GaN power devices achieve substantial higher system efficiency compared to their standard Si counterparts, the widespread adoption of GaN power devices in the market is still hampered by cost and reliability.

The tutorial will cover following aspects:

- Introduction to the AlGaN/GaN material system.
- A methodology on how to extract important information on the conduction mechanisms in the GaN buffer structure out of relatively simple measurements on TLM structures (back-gating or substrate ramp) and transistors (current DLTS).
- Impact of the buffer structure on dynamic Ron, to obtain dynamic Ron free transistors.
- Overview of the main intrinsic reliability mechanisms for GaN power devices: gate dielectric reliability (both MISHEMT and pGaN gate), NBTI/PBTI of MISHEMTs, Ohmic contact reliability, backend reliability, accelerated drain stress and hot carrier stress (semi-on-state stress). Focus on recoverable versus permanent degradation. n-specific failure modes such as the inverse piezo-electric effect.
- Acceleration models and statistical distribution models (Weibull, lognormal).
- Extrinsic reliability (HTRB, HTGB, thermal cycling etc.).
- Sense and non-sense of standard JEDEC testing for GaN power devices, and summary/overview of a new upcoming JEDEC standard for AlGaN/GaN power devices.

### **TM3.2 - Phase Change Memory: From basic technology to system aspects and new applications - Haris Pozidis, IBM Research**

Storage Class Memories (SCMs) promise to revolutionize future computing systems of all kinds with their universal properties, spanning the broad space between storage and memory. Among them, phase change memory (PCM) has seen well over a decade of research and development and is thus considered to be close to mass market deployment. However, PCM comes with a number of reliability challenges that are mostly associated with the nature of phase change materials. In this tutorial, we will discuss the most prominent reliability issues of PCM and present various circuit- and system-level solutions. As cost per bit is the most important attribute for memories, we will give particular emphasis on ways to decrease the cost of PCM, focusing on storage of multiple bits per cell. We will then discuss various system aspects, including possible uses of PCM in future computing systems and workloads. PCM technologies are also finding applications beyond the realm of memory. It is becoming increasingly clear that for application areas such as cognitive computing, computing architectures in which memory and logic coexist in some form may prevail. Brain-inspired neuromorphic computing and the fascinating new area of memcomputing are two key non-von Neumann approaches being researched. A critical requirement in these novel computing paradigms is a very-high-density, low-power, variable-state, programmable and non-volatile nanoscale memory device, and PCM devices are well suited to address this need. We will present a few examples to highlight this fascinating new research area.

### **TM3.3 - Title: Spin Torque MRAM - Daniel C. Worledge IBM Research Division, Almaden Research Center**

This tutorial will cover the basics of Spin Torque MRAM. Fundamental building blocks of magnetism, including dipole fields, magnetic anisotropy, oscillatory exchange coupling, and magnetoresistance will be introduced. A broad overview of Spin Torque MRAM will then be given, including applications, basics

of how Spin Torque MRAM works, device physics, and materials considerations. Particular emphasis will be placed on the physics of the spin-transfer torque mechanism and the dependence of the switching current on materials parameters. A short introduction

to Landau-Lifshitz-Gilbert dynamics will be given. Finally, unique aspects of the reliability of Spin Torque MRAM will be described, including retention, write-error-rate, and breakdown.

#### **Regency IV**

##### **TM4.1 - System Telemetry for Reliability Engineering - *Robert Kwasnick, Intel***

Understanding customer usage of ICs-based products and systems is an important part of establishing accurate use conditions inputs for product reliability modeling. Telemetry can be a useful tool for gaining product use knowledge. The objective of this tutorial is to provide a sufficient overview so that a motivated reliability engineer can start down the path of using telemetry for reliability. First, we discuss the range of telemetry signals that can be relevant to the reliability engineer and the role of IC and system architecture. Then, we review key aspects of needed software, acquiring user, and managing telemetry data towards reliability modeling. The last step is to use the field data towards reliability modeling inputs and since the reliability engineer is the key player in this, we'll discuss this in some detail, including examples. Finally, we will touch on the use of telemetry for prognostics.

##### **TM4.2 - System Level Reliability - *Geny Gao, PhD***

We expect every product is reliable. Corporate relies on product with reliable and good quality to satisfy customers, builds up reputations, make and gain revenues and profits. Reliability is always a concern during the product life cycle. This tutorial introduces reliability in system level. It describes the procedures and tasks from product realization to end user, i.e., design review, assessment, simulation, measurement, operation, and continuously improvement. A "body" is formed with standards so the whole processes are in the control. All reliability and other areas relevant to the business are monitored and methods are in places. The typical reliability concepts such as testing, DFR, MTBF, FIT, bath tub, and software based DRE are illustrated. As an effective tool to support reliability, failure analysis thoughts and skills are stated as well.

##### **TM4.3 - Considerations for In-Field Fault Tolerance, Self-Healing, Detection & Recovery Techniques - *Arijit Biswas, Intel***

As modern systems on chip become more complex - due to denser process geometries, logic & function integration and increasing needs for performance, efficiency and reliability - detection, diagnosis & recovery of faults must be enabled in the field during normal operation. These needs are primarily driven by market segments and use cases where the consequence of faults and failures in the field are extremely costly. We present a common framework to enable a coherent discussion of the various attributes and interactions for in-field fault tolerance, including in-field diagnostics, real-time fault detection, signaling and recovery techniques. We discuss various implementation options and their suitability for various software use cases. We look at fault tolerance techniques for variant hardware configurations for system on chip including accelerators and sensors. All these factors are described at a conceptual level while bringing the concepts into focus for various implementations specific to a few high-reliability-demanding use cases: exascale computing for HPC and Advanced Driver Automation Systems (ADAS) for Functional Safety.

## Reliability Year In Review

### **FinFET Reliability Year-in-Review and What's in Store for the Post-FinFET Era** – *Aaron Thean, National University of Singapore*

Over the last decade, CMOS logic technologies have incorporated several material disruptions. Advanced CMOS made the transition from Poly-SiON to High-k metal gate (HKMG) process about 10 years ago, for 45nm and 32nm/28nm planar CMOS transistors developed from 2007 to 2009, respectively. The efforts to bring these technologies to high-volume manufacturing accelerated our learning on gate-stack reliability, especially the role of thermal budget management on the replacement metal-gate process. There are major influences of gate PBTI and NBTI due to the device integration scheme like dopant activation and silicidation. For example, “high-k-first” and “high-k-last” gate stacks showed different reliability potentials. However, with process and integration schemes, we found solutions to engineer both stacks to meet requirements.

The next disruption came quickly as we transitioned from planar to FinFET technologies in 2011, with Intel's 22nm CMOS. This coincided with the capabilities of Atomic Layer Deposition (ALD) technologies for the HKMG process. The lessons learnt on managing BTI impact did carried forward, but we now contend with new influences due to a different dielectric-crystalline interface of the fin sidewalls and the process challenges of a largely vertically oriented gate structure. We saw that ALD material improvements helped us overcome some of the issues. However, with increased current densities and aggressive dimensional scaling, hot-carrier and device self-heating rose to top of the issue list. Following the current success of 14nm/16nm FinFET technologies, we will soon be seeing the 3<sup>rd</sup> generation FinFET technologies with upcoming 10nm and 7nm CMOS, in the coming two years. However, there are still really few knobs to overcome these top issues at the material or process levels. Except, at the circuit design or system levels through engineering the use conditions.

The next disruptions may come at or after 5nm CMOS targeted for 2020. With the need for more performance, new materials like SiGe fins are being considered for integration, or stacked Nanowires. We see exciting new reliability understanding and opportunities brought forth with these new materials and structures. Beyond FinFETs and beyond Si, we will need to prepare for low-thermal budget processes (E.g. for III-V, Ge). Encouragingly in recent years, we have gained significant new insights towards reliable low-thermal budget gate stacks. This will pave the way needed to realize the integration of these new materials for the Fin or Nanowire devices. In this presentation, we will review this evolution of understanding in reliability physics driven by this relentless revolution of device and material architectures to continue Moore's law.

### **GaN Device Reliability Year-in-Review** – *Matteo Meneghini, University of Padova*

The past few years have been exciting and extremely productive for the GaN community, and the research in the field of GaN-power devices has shown impressive advancements. In lateral GaN HEMTs, a two-dimensional electron gas (2DEG) is formed at the interface between GaN and AlGaIn; the high mobility of the 2DEG (in excess of 2000 cm<sup>2</sup>/Vs) results in current densities around 1 A/mm, and in a very low on resistance (25 mΩ for a 650 V/60 A device). This implies a significant reduction in the resistive and switching losses, compared to silicon devices, and this has a positive impact on the efficiency of GaN-based power converters (kW-range power converters with efficiency higher than 99% have already been demonstrated, based on GaN HEMTs).

A relevant aspect that is currently under study is the reliability of GaN-based transistors. In fact, during operation in high-voltage power converters, the HEMTs may be subject to extreme field and current levels that may favor device degradation. In real-life applications, several potentially harmful conditions may be reached, favoring the exposure to off-state bias, semi-on stress conditions, hard switching, and high gate bias.

This presentation reviews the most recent results published in the field of GaN-based power transistors. After a brief introduction, we discuss the latest technology developments that have an impact on device reliability. Then, we summarize the most important papers on degradation and reliability published over the past year, with focus on the most relevant stress regimes (off-state, hard switching, positive gate bias, high temperature, etc.).

### **Memory Technology Reliability Year-in-Review – Bob Gleixner, Micron**

As they continue to pursue higher performance and densities at lower cost, semiconductor memory technologies have introduced novel materials and integration schemes from the cell to the

packaging level. Understanding the reliability failure modes associated with these materials and processes is critical to providing a robust memory component. This presentation will review the major technology directions taking place in the areas of DRAM, NAND, and emerging memories. It will then review recent publications that identify the reliability concerns posed by these directions, with an emphasis on those that attempt to discern the underlying physics.

### **Workshops**

#### **COTS/System: Handshaking between systems users and COTS vendors**

**Moderators:** *ShiJie Wen, Cisco, Kenneth A. LaBel, NASA, Ken Wu, TSMC, Bharat Bhuvra, Vanderbilt University*

This workshop will discuss the different views of reliability challenges of components from the silicon technology, to design, to application requirement, and the importance of early and close hand-shaking or collaboration from end to end in the chain to address the challenges.

#### **Memory/Product: Solid State Drive (SSD) Reliability from Flash Cells to Systems**

**Moderators:** *Chandra Mouli, Micron Technology Inc, Xiaoyu Yang, SanDisk, Shosuke Fujii, Toshiba Corporation*

Solid State Drive (SSD) is basically a storage device composed of NAND flash memory. However, its reliability is determined not only by memory cell reliability but also by controller technology such as ECC, wear leveling technique. In addition, users' requirements for SSD reliability can be dependent on their use cases. Discussions including system and device engineers as well as users are thus indispensable for understanding and optimizing SSD reliability.

#### **MOL: MOL Dielectric TDDB Models**

**Moderators:** *Adrian Chasin, imec, Tian Shen, GLOBALFOUNDRIES, Shou-Chung Lee, TSMC*

FEOL and BEOL reliabilities are well recognized fields of research and are proven to be crucial for device/circuit qualification. More recently, due to increased gate-to-contact proximity for advanced nodes only the spacer sidewall material provides isolation. Moreover, a trend exists towards thinner spacers (<10nm) to maximize contact area. In this regard, MOL

reliability became also a crucial reliability aspect that has to be secured to avoid device malfunctioning. The main objective of this workshop is to discuss the possible models to extrapolate the accelerated experimental data set to device working conditions, because of its unique feature that differs from both FEOL and BEOL cases. However, the discussion will be by no means limited to this topic and other subjects will also be covered such as device layout, characterization techniques, impact of variability and materials choice.

#### **Wide Band Gap: GaN power devices reliability standardization**

**Moderators:** *Matteo Meneghini, University of Padova, Tim McDonald, Infineon Technologies*

Over the last few years, GaN has emerged as an excellent material for the fabrication of high voltage/current transistors, that will rapidly find application in the next-generation power conversion systems. 650 V/60 A transistors are already commercially available, and 1200 V devices are under development. Several papers investigated the failure modes and mechanisms of GaN-based power HEMTs, providing pathways for the improvement of this technology. However, there is no standard for the qualification of the reliability, and several questions are still open: Is dynamic Ron still a problem? How to standardize the pulsed measurements? Which testing procedures must be used for reliability estimation/assessment? Are there specific degradation processes that are not present in silicon? This workshop will address these questions, by stimulating the discussion on the standardization of reliability procedures for the development of GaN-based power HEMTs.

**Transistor: Self-heating effects on HCI and BTI: How worried should we be and what should we do about it?**  
**Moderators:** *Ashraf Alam, Purdue University, Andreas Kerber, GLOBALFOUNDRIES, Chetan Prasad, Intel Corporation*

The issue of localized self-heating is relatively new to scaled CMOS devices, such as FinFETs, fabricated on bulk-Si substrates, but it has been known to affect the performance/reliability of partially and fully depleted SOI devices for many generations. Thus, self-heating corrections were frequently employed in the HCI assessment for SOI devices. Comprehending self-heating on HCI and BTI in scaled discrete devices and CMOS circuits relies on accurate thermal modeling for circuits operating at high frequencies. Such thermal modeling

must not only account for the power dissipated and the thermal resistances, but also comprehend the open boundary conditions

associated with mobile devices, such as tablets and cell phones. The intent of this workshop is to discuss the characterization and

modeling approaches for localized self-heating in advanced technology nodes, and to highlight areas which need further attention.

**Extrinsic: Juggling Knowledge Based and Standards Based Qualifications**

**Moderators:** *Bob Knoell, NXP  
Jeffrey Hicks, Intel*

This compromise can also be between application-specific and stress-test based qualification methods or between physics-of-failure and right-censored testing. In one case, an application that fits, say, the 90th percentile of customer usage that utilizes one set of tests, conditions and durations versus one where the application determines a variable set of tests, conditions and durations. In the other case, a set of tests, conditions and durations that are based on the acceleration of known specific physical failure mechanisms versus a set of tests, conditions and durations based on a set of known stimuli such as temperature, humidity and mechanical stress experienced in the field. This workshop will discuss the advantages and limitations of each method to give the participants an idea of when to utilize each for their qualification program.

## IRPS Program

Tuesday, April 4, 2017

General Session  
Regency Main  
8:00 a.m.

Welcome Remarks  
Yuan Chen, NASA

8:10 a.m.  
Introduction to Technical Program

8:30 a.m.  
Keynote 1

**Reflections on the risk of human space exploration – lessons learned from past failures, Dr. Nancy Currie-Gregg**  
*NASA Astronaut; Principal Engineer, NASA Engineering and Safety Center*



Human spaceflight is an inherently risky endeavor. From the first missions to explore space to recent problems on the International Space Station, NASA has faced many challenges and has relied on creative and innovative ways to overcome issues, complete the mission, and ensure the safe return of crew members. However, over the past 50 years, NASA has also experienced three fatal accidents resulting in the loss of seventeen astronauts – the Apollo 1 fire on the launch pad, the Space Shuttle Challenger explosion during ascent, and the destruction of the Space Shuttle Columbia during entry. Studying the lessons learned from the Challenger and Columbia accidents, as well as similarities in those two tragedies, provides a prospective of cultural, organizational, and management failures that can occur in any engineering organization managing extremely complex systems operated in high risk environments.



**System Level Reliability Challenges with Technology Scaling, Mr. Ronald Newhart**  
*IBM Distinguished Engineer, IBM Systems & Technology Group*



Mr. Ronald Newhart is currently a Distinguished Engineer with IBM working in the Systems & Technology Group, focusing on product engineering and reliability. His first nineteen years with IBM entailed assignments in semiconductor parametric and functional characterization, memory design, yield modeling, and reliability engineering. For the past sixteen years, he has been the lead technology interface to the IBM POWER and Z Series circuit design teams. Ron's contributions have supported the development and manufacturing of more than nine generations of POWER and Z System microprocessors. Ron frequently consults on complex problems that span design, process, and technology for both IBM internal products and other IBM System supplier components. He has co-authored fourteen US Patents and has received several corporate awards.

Mr. Newhart has a Bachelor of Science degree in Electrical Engineering from Pennsylvania State University and a Master of Science degree in System Management from the University of Southern California.

***Session 2A - Wide Band Gap***

Session Chairs: *Denis Marcon, IMEC, Sandeep Bahl, Texas Instruments*

Tuesday, April 4

Regency Main

10:35 a.m. - Session Introduction

10:40 a.m.

**2A.1 Understanding and Reduction of Degradation Phenomena in SiC Power Devices (Invited)**

*T. Kimoto, A Iijima, T. Tsuchida\*, T. Miyazawa\*, T. Tawara\*\*, A. Otsuki\*\*, T. Kato\*\*\*, Y. Yonezawa\*\*\*, Kyoto University, \*Central Research Institute of Electric Power Industry, \*\*Fuji Electric Co., Ltd., \*\*\*Nat'l Institute of Advanced Industrial Science and Technology*

Impacts of extended defects on performance and reliability of SiC power devices are reviewed. Threading dislocations in the state-of-the-art SiC wafers do not work as the major leakage paths and macroscopic defects generated during epitaxial process are more harmful. A basal plane dislocation is a killing defect in SiC bipolar devices because a Shockley-type stacking fault (SSF) is expanded from the dislocation when the electron-hole recombination energy is given. After classification of SSF-expansion patterns, the major types of SSFs (triangular-shaped and bar-shaped SSFs) and their origins are identified. Based on these understandings, two approaches to eliminate the "bipolar degradation" in SiC devices are presented. In particular, it is demonstrated that a "recombination-enhancing layer" is effective for substantial reduction of bipolar degradation in SiC devices.

11:05 a.m.

### **2A.2 SiC MOSFET Design Considerations for Reliable High Voltage Operation (Invited)**

*P. Losee, A. Bolotnikov, L. C. Yu, G. Dunne, D. Esler, J. Erlbaum, B. Rowden, A. Gowda, A. Halverson, R. Ghandi, P. Sandvik and L. Stevanovic, R. Hristov\*, General Electric, \*Powerex Power Semiconductor Solutions*

SiC MOSFETs have demonstrated continued performance improvement and maturation in the areas of gate-oxide stability and reliability over the past few years. While gate oxide reliability is necessary, it is not sufficient to achieving reliable high voltage operation. In this paper, the constraints of achieving such reliability and their impact on SiC MOSFET device design and performance at useful operating conditions are discussed. Experimental results are demonstrated with industry benchmark, reliable operation of up to  $T_j=200^\circ\text{C}$  with 1.2kV/25mOhm SiC MOSFETs and  $T_j=175^\circ\text{C}$ , 1.7kV/450A All-SiC Dual-Switch Modules. Avalanche ruggedness of the high-performance devices is also demonstrated with single-pulse Energy densities of 10-15J/cm<sup>2</sup> recorded with drain currents as high as  $I_D=90\text{A}$  for 0.2cm<sup>2</sup> die.

11:30 a.m.

### **2A.3 Transient Out-of-SOA Robustness of SiC Power MOSFETs (Invited)**

*A. Castellazzi, A. Fayyaz, G. Romano\*, M. Riccio\*, A. Irace\*, J. Urresti-Ibanez\*\*, N. Wright, \*\*, Nottingham University, \*University of Naples "Federico II", \*\*Newcastle University*

Beyond their main function of high-frequency switches in modulated power converters, solid-state power devices are required in many applications to also ensure robustness against a number of overload operational conditions. This paper considers the specific case of 1200 V SiC power MOSFETs and analyses their performance under three main transient regimes at the edge of and out of their Safe Operating Area: unclamped inductive switching led avalanche breakdown; short-circuit; operation as current limiting and regulating devices. The results presented highlight both inherent major strengths of SiC over Si and areas for improvement by tailored device design. The paper aims to contribute useful indications for technology development in future device generations to better match widespread and varied application requirements.

11:55 a.m.

### **2A.4 SiC MOSFET Reliability and Implications for Qualification Testing (Invited)**

*A. Lelis, U.S. Army Research Laboratory*

There are a number of potential reliability issues associated with SiC power MOSFETs, including threshold-voltage stability, gate-oxide reliability, body-diode robustness, short-circuit current robustness, and radiation effects. This talk is primarily focused on threshold-voltage stability and the need for an improved test method to unambiguously separate out good devices from bad ones. Threshold-voltage stability is affected primarily by active charge traps in the near-interfacial region of the insulating gate oxide. Their close proximity to the semiconductor interface leads to a strong time dependence in the direct-tunneling mechanism in response to changes in gate bias. This time dependence is not properly accounted for in the existing test methods for assessing high-temperature gate-bias (HTGB) effects, which allow temporary removal of bias during cool down and significant un-biased delay (up to 96 hours) before the post-stress measurements are performed. However, this delay, introduced to accommodate the practical constraints of industrial testing, renders this test practically meaningless due to the significant recovery that occurs in the charge states of the near-interfacial oxide traps. This difficulty can be overcome by reapplying the gate bias for a brief period of time before measuring. Details of the nature of the near-interfacial oxide traps will be discussed, including their activation energy. All this work will be presented within the context of standards development within JEDEC, and a new SiC power-devices qualification working group.

## Session 2B - Failure Analysis/Process Integration

Session Chairs: *Bryan Tracy, EAG Laboratories, Kevin Johnson, Intel*

Tuesday, April 4

Regency I

10:35 a.m. - Session Introduction

10:40 a.m.

### **2B.1 Study of Junction Degradation and Lifetime Assessment in FinFETs**

*P.J. Liao, T.Y. Hox, K. Joshi, J.R. Shih and Y.-H Lee, Taiwan Semiconductor Manufacturing Company*

Time dependent junction degradation (TDJD) is studied in detail for advanced FinFET technology and is to be caused by band to band tunneling current increase. This current leakage can be controlled by process optimization and junction engineering. It is shown that non-optimized process has poor junction reliability due to trap assisted band to band tunneling. A degradation rate based prediction model is also proposed which can be helpful in assessing junction reliability lifetime at use-condition

11:05 a.m.

### **2B.2 Effect of La and Al Addition used for Threshold Voltage Shift on the BTI Reliability of HfON-based FDSOI MOSFETs**

*P. Kumar, C. Leroux, F. Domengie\*, C. S. Segovia\*, B. Mohamad, A. Toffoli, G. Romano, X. Garros, G. Ghibaudo\*\* and G. Reimbold, CEA-LETI, \*STMicroelectronics, \*\*IMEP-LAHC*

Incorporation of La into the FDSOI gate dielectrics causes significant degradation of NBTI (Negative Bias Temperature Instability) effect attributed to La creating IL defects. La reduces the PBTI (Positive Bias Temperature Instability) effect due to La passivating oxygen vacancies in HfON. Al has small impact on NBTI but a large impact on PBTI degradation, it can be attributed to no or little reaction of Al with the IL and defect creation in HfON respectively.

11:30 a.m.

### **2B.3 Gate Stack Thermal Stability and PBTI Reliability Challenges for 3D Sequential Integration: Demonstration of a Suitable Gate Stack for Top and Bottom Tier nMOS**

*J. Franco, L. Witters, A. Vandooren, H. Arimura, S. Sioncke, V. Putcha, A. Vais, Q. Xie\*, M. Givens\*\*, F. Tang\*\*, X. Jiang\*\*, A. Subirats, A. Chasin, L.-Å. Ragnarsson, N. Horiguchi, B. Kaczer, D. Linten and N. Collaert, imec, \*ASM Belgium, \*\*ASM America*

3D Sequential Integration has been envisioned to stack transistors in the same front-end process. A crucial challenge is the management of the thermal budget. We focus on Si nMOS gate stack challenges, specifically: for a top tier device, we demonstrate sufficient PBTI reliability without resorting to unsuitable high temperature anneals by inserting a thin LaSiO<sub>x</sub> interlayer between SiO<sub>2</sub> and HfO<sub>2</sub>. This gate stack also offers good thermal stability for a pMOS over nMOS scenario.

11:55 a.m.

**2B.4 The Copy Exactly! Evolution Story: High Reliability, Fungible Output Based Solely Upon Matching**, *A. Lucero, C. Connor, T. Utlaut and I. Hsu, Intel Corporation*

Early Copy Exactly! methods which focused on matching of equipment, inputs and output matching have evolved to include all aspects of real-time automated controls, inline monitors and human interfaces. Present-day copy exactly! (CE!2.0) for high-yielding factory start-up is now augmented with online real-time process quality and reliability monitors for timely decisions and responses ensuring high reliability and equivalent performance. The manuscript will show CE! and demonstrate matching of key process real-time data, reliability and yield.

***Session 2D - Transistors/Beyond CMOS***

Session Chairs: *Souvik Mahapatra, India Institute of Technology, Steve Ramey, Intel*  
Regency Main  
Tuesday, April 4

2:10 p.m. - Session Introduction

2:15 p.m.

**2D.1 Circuit Relevant HCS Lifetime Assessments at Single Transistors with Emulated Variable Loads**

*C. Schlünder, F. Proebster, J. Berthold, K. Puschkarsky, G. Georgakos, W. Gustin and H. Reisinger, Infineon Technologies AG*

The mechanism of HCI-Assisted-TDDB (HA-TDDB) was investigated. Weak temperature dependence is associated with two competing mechanism, i.e., mitigation of impact-ionization and enhanced traps generation under high temperature. HA-TDDB lifetime was improved >10x by AC-stress due to significant recovery. Large Weibull slope and negligible area scaling factor at high Vd bias are ascribed to oblique percolation path and self-heating effect. The trade-off between performance and reliability was resolved through process and design rule optimization.

2:40 p.m.

**2D.2 Circuit Relevant HCS Lifetime Assessments at Single Transistors with Emulated Variable Loads**

*C. Schlünder, F. Proebster, J. Berthold, K. Puschkarsky, G. Georgakos, W. Gustin and H. Reisinger, Infineon Technologies AG*

HCS measurements at single devices reveal critical parameter degradation, but there are several publications stating that HCS plays only minor role. An accurate circuit relevant assessment method is required to evaluate the correct HCS impact on lifetime. We introduce a new methodology to investigate product relevant HCS lifetime at single test devices. We compare the results in detail with the standard worst case approach. We elaborate this at two different technologies (130nm and 40nm).

3:05 p.m.

### **2D.3 Device Reliability Metric for End-of-Life Performance Optimization Based on Circuit Level Assessment (Invited)**

*A. Kerber, P. Srinivasan, S. Climino, P. Paliwoda, S. Chandrashekar, Z. Chbili, S. Uppal, R. Ranjan, M.-I. Mahmud, D. Singh, P.P. Manik, J. Johnson, F. Guarin, T. Nigam, B. Parameshwaran, GLOBALFOUNDRIES Inc.*

Device performance enhancement is critical for offering competitive CMOS solutions for advanced technology nodes. To benchmark the impact of performance enhancement elements the device reliability metric needs to comprehend the impact of the degradation on the CMOS circuits like SRAM and ring-oscillators. We confirm that time-zero and BTI induced stochastic variation are most critical for SRAM circuits while for logic circuits like ring-oscillators the focus is on the mean degradation. In addition, we explore the impact of self-heating on the correlation of device to circuit degradation for the FinFET device architecture.

3:30 – Break

3:50 p.m.

### **2D.4 Comparison of DC and AC NBTI Kinetics in RMG Si and SiGe p-FinFETs**

*N. Parihar, R. G. Southwick\*, M. Wang\*, J. Stathis\*\* and S. Mahapatra, Indian Institute of Technology Bombay, \*IBM Research Division, Albany, \*\* IBM Research Division, TJ Watson Research Center*

Negative Bias Temperature Instability continues to be a reliability concern for HKMG FinFETs. It is expected that future p-MOSFETs will incorporate SiGe channels. In this paper, we report new data from UF (10us delay) characterization of DC and AC NBTI in Si and SiGe FinFETs. We examine similarities and differences between Si and SiGe FinFET NBTI temporal kinetics during stress and recovery, and dependencies on the stress bias, temperature, AC duty cycle and frequency.

4:15 p.m

### **2D.5 Statistical Assessment of the Full $V_G/V_D$ Degradation Space using Dedicated Device Arrays**

*E. Bury, B. Kaczer, K. Chuang, J. Franco, P. Weckx, A. Chasin, M. Simicic, D. Linten and G. Groeseneken, imec*

In this work, we i) design and measure a fabricated test-array capable of capturing degradation statistics, ii) obtain the mean and the variance of multiple device degradation metrics ( $\Delta V_{TH}$ ,  $\Delta g_m$ , ..) for any arbitrary  $\{V_G, V_D\}$  combination, and iii) show that time-dependent variability induced by channel Hot Carrier Degradation (HCD) in deeply scaled devices is much more severe than (P)BTI-induced variability.

4:40 p.m.

### **2D.6 Benchmarking Time-Dependent Variability of Junctionless Nanowire FETs**

*B. Kaczer, G. Rzepa\*, J. Franco, P. Weckx, A. Chasin, V. Putchu, E. Bury, M. Simicic, P. Roussel, G. Hellings, A. Veloso, P. Matagne, T. Grasser\* and D. Linten, imec, \*TU Wien*

We study the time-dependent variability of JL GAA NW pFETs and observe it to be comparable to IM pFinFETs. However, provided that other sources of variability are suppressed, JL FETs time-0 and time-dependent variability may remain high due to the high body doping.

## ***Session 2E - Soft Error***

Session Chairs: *Balaji Narasimham, Broadcom, Marta Bagatin, University of Padova*

Tuesday, April 4

Regency I

2:10 p.m. - Session Introduction

2:15 p.m.

### **2E.1 Paving the Way Towards Autonomous Driving – Tackling Soft Errors to Security Challenges (Invited)**

*M. Duncan, STMicroelectronics*

The complexity of the requirements for automotive applications is increasing at an astonishing pace. Concepts from other domains are being introduced in order to address these demands. For example we now need to cover fault tolerant and failsafe systems. The functional safety of systems, products and processes increases with every day and with every new development and we must maintain a grasp of the risks during every phase: from the first concept through development and from operation through shutdown. With the increasing complexity of automotive devices mainly microcontrollers with increased performance, features and memory size the importance of soft errors is becoming critical and must be considered as potential main risk for safety critical functions. Increased connectivity and complexity creates serious security challenges for the design of automotive hardware/software architectures due to attacks. Virtualization is now being made available in automotive embedded environments providing developers with the ultimate open platform: the ability to run any flavor of operating system in any combination, creating an unprecedented flexibility for deployment and usage. With the immense processing power that is being unlocked with multi-processor systems we are now able to address complex issues such as a complete inspection of the vehicle's environment. In this paper, we will discuss the challenges of implementing a safe, secure, complex driver assistance system that paves the way towards autonomous driving.

2:40 p.m.

### **2E.2 A Critical Re-examination of the Impact of Body-bias on Soft Error Rate and Single-event Latch-up in Automotive STRAMs**

*N. Mahatme, K. Loiko and B. Min, NXP Semiconductors*

Body-biasing is used for power/performance regulation for modern ICs. Body-biasing does have SER/SEL implications which have complex dependence on well bias based on trade-offs between drive current and physics of parasitic bipolar action. For specific applications, it may be possible to reduce power, SER and SEL, all three, with body-biasing. Practical design limits are proposed on the extent of well bias to achieve lower power and high reliability especially for high temperature automotive SRAMs.

3:05 p.m.

### **2E.3 Investigation of Logic Soft Error and Scaling Effect in 10 nm FinFET Technology**

*T. Uemura, S. Lee, G. Kim and S. Pae, Samsung Electronics*

This paper presents characterization of soft error in logic circuits manufactured with Samsung's 10 nm FinFET technology. The 10 nm FinFET technology provides significant improvement in logic SER, more than 10X smaller than in 14 nm FinFET technology. The scaling impact in logic circuit is larger than SRAM. As a result, FF-SER becomes lower than SRAM-SER in 10 nm FinFET. The SER impacts on the technology scaling and design changes are analyzed with physics-based simulation.

3:30 – Break

3:50 p.m.

**2E.4 On the influence of BTI and HCI on parameter variability – ESREF Paper**

*C. Schlünder, J. Berthold, F. Proebster, A. Martin, W. Gustin, H. Reisinger, Infineon Technologies AG*

***Session 2F - Photovoltaics***

Session Chairs: *Andrea Cester, University of Padova, Michael Daenen, Hasselt University*

Tuesday, April 4

Regency IV

2:10 p.m. - Session Introduction

2:15 p.m.

**2F.1 Interface Engineering for High Performance and Stable MIS Photosynthesis Cells (Invited)**

*P. McIntyre, Stanford University*

Photoelectrolysis is of interest for direct solar-driven production of chemicals and fuels. A persistent challenge in this field is the difficulty of simultaneously achieving high photovoltaic efficiency and chemical stability of semiconductor photoelectrodes during water oxidation. In 2011, Chen et al. demonstrated that atomic layer deposition (ALD) of a thin TiO<sub>2</sub> layer can avoid oxidation of the surface of a Si photoanode during long-duration oxygen evolution. Using an ALD-TiO<sub>2</sub> corrosion protection layer, it was possible to decouple efficient light absorption by the Si anode from the oxygen evolution reaction (OER) occurring on the surface of a catalyst layer overlying the TiO<sub>2</sub>. Metal oxide protection layers that block oxidative corrosion of highly efficient solar absorbers while permitting facile hole transport from the semiconductor to the OER catalyst layer have since become the standard approach for photoelectrochemical hydrogen synthesis. Reports of increasing photocurrent, photovoltage, and corrosion stability appear in the literature regularly.

For silicon photoanodes, the most favorable combination of photovoltage and photocurrent during water splitting has been achieved using thin ALD-TiO<sub>2</sub> protection layers on a buried p+n junction. However, a buried homojunction electrode has several drawbacks compared to a simpler metal-insulator-semiconductor (MIS) Schottky junction. Formation of the buried junction involves extra processing steps and complexity. Furthermore, some interesting absorbers for tandem cells cannot form such junctions. Based in part on lessons learned from MIS gate stack engineering<sup>5</sup> and from ultrathin oxide passivation of Schottky junction solar cells,<sup>6</sup> we have investigated methods to boost the performance of MIS Schottky silicon photoanodes. This presentation will describe several approaches for engineering the interface region between the silicon surface and an overlying OER catalyst to build in high photovoltage and photocurrent, while inhibiting oxidative corrosion of the semiconductor. Relevance of these methods to other systems will be summarized briefly.

This work is supported in part by the Stanford Global Climate and Energy Project and by National Science Foundation program CBET-1336844. The contributions of A. Scheuermann, P. Satterthwaite, K. Kemp, A. Meng, K. Tang, J. Lawrence, O. Hendricks, P.K. Hurley and C.E.D. Chidsey are gratefully acknowledged.

2:40 p.m.

**2F.2 Open Circuit Voltage Decay as a Tool to Assess the Reliability of Organic Solar Cells: P3HT:PCBM vs. HBG1:PCBM**

*L. Torto, A. Cester, L. Passarini, A. Rizzo, N. Wrachien, M. Seri\* and M. Muccini\*, University of Padova, \* CNR-ISOF, CNR-ISMN*

We performed electrical stresses on organic solar cells based on two polymers (P3HT:PCBM, HBG1:PCBM) applying different characterizations, such as impedance spectroscopy and open circuit voltage decay. We modeled the carrier lifetime decay, showing the better reliability of HBG1 with respect to P3HT.

3:05 p.m.

**2F.3 Effect of Field and Pump Light Wavelength During DC Stress on the Efficiency Improvement of Amorphous Silicon Single Junction and Tandem Solar Cells**

*A. Scuto, C. Gerardi\*, A. Battaglia\*\*, A. Canino\*\* and S. Lombardo, CNR-IMM, \*ENEL Green Power, \*\*3SUN S.r.l.*

In this work it is compared the instability behavior of single a-Si:H p-i-n devices with that of tandem a-Si:H / microcrystalline Si solar cells. In details, it is here reported about the radical differences between the forward and reverse bias stress and on the spectroscopic signature of the defects responsible for the recovery / improvement effect.

3:30 – Break

3:50 p.m.

**2F.4 Analysis of Electrical and Thermal Stress Effects on PCBM:P3HT Solar Cells by Photocurrent and Impedance Spectroscopy Modeling**

*L. Torto, A. Rizzo, A. Cester, N. Wrachien, L. Passarini, F. C. Krebs\*, M. Corazza, and S. A. Gevorgyan\*, University of Padova, \*Technical University of Denmark*

We investigated the effects of electrical stress and thermal storage by means of photocurrent and Impedance Spectroscopy models. The electrical stress damages only the active layer, by reducing the generation rate and the polaron separation probability. The thermal stress also degrades the anode interface changing the photocurrent shape.

4:15 p.m.

**2F.5 Irreversible Damage at High Levels of Potential-induced Degradation on Photovoltaic Modules; a Test Campaign**

*J. Carolus, W. De Ceuninck and M. Daenen, Hasselt University*

A stress test for potential-induced degradation (PID) on photovoltaic (PV) modules according to IEC 62804 and a recovery test in the same conditions were conducted on a set of 49 modules. From this report, it can be stated that a significant number of modules installed in Flanders are PID sensitive. Furthermore, it is important to detect and recover the PID affected modules in an early stage in order to be able to recover them.



**Wednesday, April 5, 2017**

***Session 3A - Product/Memory***

Session Chairs: *Alessandro Spinelli, Politecnico di Milano, Brian Pedersen, Intel*

Wednesday, April 5

Regency Main

8:00 a.m. - Session Introduction

8:05 a.m.

**3A.1 Knowledge Based Qualification Using Temperature/Vltage Time-Ordered Events Pairing (Invited)**

*I. Sauciuc, Intel*

The explosion in usage across many different market segments requires very clear understanding of the CPU products usage. We will describe a method to standardize the reliability qualifications base on defining use cases which will help establish a baseline for minimum reliability qualifications. Once the use case are defined the importance of multitasking is discussed for both turbo residencies and thermal mechanical requirements. The new methodology validation is discussed using client field consumer data.

8:30 a.m.

**3A.2 Robust Automotive Products in Advanced CMOS Nodes, V. Huard, S. Mhira, M. De Tomasi, E. Trabace, R. E. Vaion and P. Zabberoni, STMicroelectronics**

We demonstrate that many elements are needed on top of conventional foundry reliability knowledge to enable robust automotive products in compliance with all restrictive norms. For intrinsic reliability, the main element is the reliability models, their usage for design margins definition and their validation at IP level. For extrinsics failure, two different screening procedures are documented and in use for volume production. Altogether, the global approach presented enable robust automotive products based on validated procedures.

8:55 a.m.

**3A.3 Product-Level Reliability Estimator with Budget-Based Reliability Management in 16nm Technology, J.-G. Ahn, M.F. Lu, N. Navale, D. Graves, G. Refai-Ahmed, P.-C. Yeh, J. Chang, Xilinx, Inc.**

We have developed Product-Level Reliability Estimator with budget-based reliability management in 16nm technology with considering thermal impact on product lifetime more accurately. Reliability risk of each block and mechanism is obtained quantitatively and is saved as a database for each product by using EDA tools extensively. Budget checking approach helps design and application to make realistic estimation on product lifetime with temperature increase issues which is unavoidable in scaled technology.

9:20 a.m.

### **3A.4 Dynamic Adaptive Voltage Scaling in Automotive Environment,**

*S. Mhira, V. Huard, F. Cacho, S. A. Benhassain, A. Jain, C. Parthasarathy, S. Naudet and A. Bravaix\*, STmicroelectronic, \*ISEN-REER, IM2NP*

Novel control loop for Dynamic Adaptive Voltage Scaling for safety-critical applications has been proved using a System-On-Chip demonstrator with integrated Programmable Dynamic Controller and fully-featured BCH decoders and commercial microcontrollers with IS2M monitors. The control loop robustness was studied by using Time-Dependent Markov Chains theoretical description and confronted to experimental results. Even considering Static AVS approach, our solution offers an additional 25% power savings while enabling very low failure rate.

9:45 a.m.

### **3A.5 Type-C Interface Reliability Concern of Electrical Overstress and Design for Mitigation**

*S.-E. Liu, H.-S. Huang\*, Y.-H. Lin\*, C.-H. Kuo\*, C.-Y. Hsiao\*, T.-C. Kao\*, G.-Y. Chen\*\*, M.-Z. Lin, Y.-H. Fang and M.-J. Lin, Quality Assurance, \*MediaTek, \*\*Taiwan Semiconductor Manufacturing Company*

We disclose USB Type-C interface reliability concern of electrical overstress, discuss design considerations for mitigation, and then verify our design by a proposed testing methodology. Type-C connectors feature bi-directional plugging and high power delivery, but their smaller pin spacing can induce overstress events to impact IC reliability. The possible USB system weakness is examined and design considerations are discussed and implemented. Finally, a testing methodology is proposed to validate the robustness of our design.

## ***Session 3B - Wide Band-Gap***

Session Chairs: *Denis Marcon, imec, Sandeep Bahl, Texas Instruments*

Wednesday, April 5

Regency I

8:00 a.m. - Session Introduction

8:05 a.m.

### **3B.1 Reverse Bias Lifetime Reliability Assessments of HV GaN Power Device**

*D. Veerreddy, S. G. Khalil, H. Kannan, A. Dip, H. Kim, Z. Wang, M. Crandell, M. Imam, T. McDonald and A. Charles, Infineon Technologies Americas Corporation*

There is no existing industry standard for Gallium Nitride (GaN) power device high temperature reverse bias (HTRB) qualification test. In this work, we conducted reverse bias lifetime assessments of 600 V rated prototype GaN devices processed with different gate module processes to deduce the related acceleration models. These results were then used to present the methodology of use-level lifetime estimations and HTRB qualification stress time derivation, translated from hypothetical application profiles.

8:30 a.m.

### **3B.2 Reliability and Failure Analysis in Power GaN-HEMTs (Invited)**

*M. Meneghini, I. Rossetto, C. De Santi, F. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni and G. Meneghesso University of Padova*

Power GaN transistors have recently demonstrated to be excellent devices for application in power electronics. The high breakdown field and the superior mobility of the 2-dimensional electron gas allow to fabricate transistors with low resistive and switching losses, that permit to increase the efficiency of switching mode power converters beyond 99 %. GaN-based transistors are currently supposed to be adopted in KW-range power converters; 650 V transistors are already available on the market, and 1200 V devices are currently under development.

During operation, GaN power transistors can reach critical conditions, especially in the off-state (with a high VDS, in excess of 650 V), during hard-switching (where high current and voltage can be simultaneously present), and for high positive gate voltages (in the case of normally-off devices). This paper reports our most recent results on the gradual and catastrophic degradation of GaN-based power HEMTs. We present the results of three different case studies, on: (i) the time-dependent breakdown of power HEMTs submitted to high off-state stress; (ii) the degradation of HEMTs with p-GaN gate submitted to high gate stress; (iii) the hot electron effects in GaN-MISHEMTs submitted to high-temperature source current stress.

8:55 a.m.

### **3B.3 Trapping effects considerations on Linearity requirements for Basestation (Invited)**

*J. Jimenez, Qorvo*

The increase of the number of channels of today's communication systems has augmented the linearity requirements of the components used in the signal transmitters, particularly in the power amplifier stage. Increasing linearity is required to a) decode the symbols in an everyday tighter constellation as well as to keep the information in a channel and not to spill into adjacent channels. Increasing the raw linearity of the semiconductor used in the amplifier stage (LDMOS, GaN or GaAs) has, in most of the cases, not been enough given the inherent non linearities of a FET or HBT type device, particularly when efficiency is also a requirement. Dynamic Pre-Distortion (DPD) architectures have come to the rescue and today most high performance linear system use such techniques. DPD systems attempt to pre-distort the input signal to compensate for the raw non-linearities of the devices. The signal response of an amplifier at a given time does not only depend on the particular input signal at a given time but also on its history (short and long term). It is this fact what has blur the boundaries between linearity and transistor memory topics, the latter a topic covered in many reliability conferences. The linearity field is not anymore just about getting more constant gm's or less bias dependent capacitances, but also about engineering the memory effects of the transistor. In this presentation, we will use GaN device technology variations to study trapping effects and more important the DPD improvements it produce at the product level. In this paper, we will also study circuit design knobs, such as drain voltage, quiescent current, or temperature, all of which change memory effects on the transistors to study DPD improvements. Finally, in this presentation, we will use different system test benchmark (ACPR and Dynamic AM-AM corrected and uncorrected, AM-PM and pulse recovery and EVM) to study the limiting factors to a given correction.

9:20 a.m.

### **3B.4 Gate Current Degradation in W-band InAlN/AlN/GaN HEMTs under Gate Stress**

*Y. Wu and J. del Alamo, Massachusetts Institute of Technology*

InAlN/GaN HEMTs is very promising for millimeter-wave applications due to their excellent gate length scaling potential. This stems from the high spontaneous polarization of InAlN that yields a large 2DEG density at the InAlN/GaN interface. However, the use of a very thin barrier layer also brings leakage current and reliability concerns to the fore. To address the issues, this work focuses on gate voltage stress through which two degradation mechanisms have been identified.

9:45 a.m.

### **3B.5 Characterization and Modeling of Single Defects in GaN/AlGaIn Fin-MIS-HEMTs**

*A. Grill, B. Stampfer, M. Watzl, K.-S. Im\*, J.-H. Lee\*, C. Ostermaier\*\*, H. Ceric and T. Grasser, TU Wien, \*Kyungpook National University, \*\*Infineon Technologies AG*

Charge trapping in GaN-MIS-HEMTs is a serious reliability challenge but is still poorly understood. In this work, we extract the properties of four preexisting single-charge defects, which are identified by their correlated random telegraph noise (RTN) signals and step heights. We show that they are in close proximity to each other and also share a similar trap-level despite their different capture and emission times.

## ***Session 3C - Dielectrics-Gate, MOL, BEOL***

Session Chairs: *Yung-Huei Lee, TSMC, Nagarajan Raghavan, Singapore University of Technology*

Wednesday, April 5

Regency IV

8:00 a.m. - Session Introduction

8:05 a.m.

### **3C.1 Statistical Basis and Physical Evidence for Clustering Model in FinFET Degradation**

*Se. Mei, N. Raghavan, M. Bosman\* and K. L. Pey, Singapore University of Technology and Design, \*A\*STAR*

In this study, we present physical and statistical evidence to highlight the similarities and differences in the kinetics of the dielectric breakdown mechanism in FinFET devices, in comparison to their planar analogues. We have provided a phenomenological derivation of the failure distribution that demonstrates the need for a clustering model to represent dielectric breakdown in FinFET devices, accompanied by statistical data analysis and physical analysis evidence of DBIE failures (involving clustered Si defect growth).

8:30 a.m.

### **3C.2 SILC Degradation Model to Predict Area Scaling for Gate Dielectric Breakdown in Advanced Technologies**

*S. Chang, K. Joshi, P.J. Liao, J.R. Shih and Y.-H. Lee, Taiwan Semiconductor Manufacturing Company*

High-K metal gate stack with bi-modal distribution provides the TDDB benefit in product usage condition. A degradation rate based Monte-Carlo simulator is developed for the first time to predict TDDB degradation based on two degradation regimes, namely SILC and thermal runaway regime. It is validated against experimental data. Finally it is shown for an optimized process, the model can provide 50X higher lifetime compared to conventional area scaling model, providing needed headroom in advanced technologies.

8:55 a.m.

### **3C.3 New Insights into the Amplitude of Random Telegraph Noise in Nanoscale MOS Devices**

*Z. Zhang, S. Guo, X. Jiang, R. Wang, Z. Zhang, P. Hao, Y. Wang and R. Huang, Peking University*

The distributions of RTN amplitude are comprehensively understood based on the extracted RTN data with and without coupling, which are characterized based on the proposed HMM method. With the coupling effect increasing, the apparent amplitude distribution is changing from exponential-like to lognormal-like, while the exact format is the two-stage lognormal distribution. The new insights into the RTN amplitude distribution with the impacts of trap coupling are important for reliability modeling and circuit design against RTN.

9:20 a.m.

### **3C.4 The Physical Explanation of TDDB Power Law Lifetime Model Through Oxygen Vacancy Trap Investigations in HKMG NMOS FinFET Devices**

*C.-H. Yang, S.-C. Chen, Y.-S. Tsai, R. Lu and Y.-H. Lee, Taiwan Semiconductor Manufacturing Company*

The physical explanation of TDDB power law lifetime model is successfully interpreted through the analysis of oxide trap generation with HK/IL gate stack in NMOS-FinFET technology using SILC spectrum methodology. It is found that TDDB power law model has a strong correlation to deep trap generation. While shallow trap plays a role in the increase of SILC behavior and the promotion of further deep trap formation during the gate oxide degradation.

9:45 a.m.

### **3C.5 Nanoscale Investigations of Soft Breakdown Events in Few Layered Fluorinated Graphene**

*A. Ranjan, N. Raghavan, B. Liu\*\*, S.J. O' Shea\*, K. Shubhakar, C.S. Lai\*\* and K. L. Pey, Singapore University of Technology and Design, \*A\*STAR, \*\*Chang Gung University*

We perform scanning-tunneling-spectroscopy on bi/tri-layered fluorinated-graphene dielectrics, enabling investigation of degradation-and-breakdown at nanoscale. Our characterization results show that energy-gap can be tailored by surface-functionalization of graphene. Experimental evidence of electrical stress induced degradation and breakdown trends at localized spots across bi/tri-layered FG films is presented. Statistical analysis on bi-layered FG film breakdown data reveals trimodal Weibull distribution trend possibly due to variations in effective FG thickness due to imperfect fluorine incorporation during fluorine diffusion process.

## ***Session 3D - Soft Error***

Session Chairs: *Balaji Narasimham, Broadcom, Marta Bagatin, University of Padova*

Wednesday, April 5

Regency Main

10:40 a.m. - Session Introduction

10:45 a.m.

### **3D.1 CubeSat: Real-time Soft Error Measurements at Low Earth Orbits (Invited)**

*B.Sierawski, R. Reed, K. Warren, A. Sternberg, R. Austin, J. Trippe, R. Weller, M. Alles, R. Schrimpf, L. Massengill, D. Fleetwood, G. Buxton\*, J. Brandenburg\*, W. Burns Fisher\* and R. Davis\*, Vanderbilt University, \*AMSAT*

Vanderbilt has developed a low-cost on-orbit system to assess the radiation reliability and survivability of advanced semiconductor components in space. This system was integrated into the AO-85 CubeSat to enable comparisons between observations and proton error rate predictions. The Vulcan payload includes

the Low-Energy Proton (LEP) Experiment reporting on the integrity of data stored in a commercial SRAM thus providing data on the single event upset rate. Three additional missions are underway to investigate the upset rate of various technology nodes.

11:10 a.m.

### **3D.2 Abnormal Increase in Soft-error Sensitivity of Back-biased Thin-BOX SOI SRAMs**

*D. Kobayashi, K. Hirose, T. Ito\*, Y. Kakehashi\*, O. Kawasaki\*, T. Makino\*\*, T. Ohshima\*\*, D. Matsuura\*\*\*, T. Narita\*\*\*, M. Kato\*\*\* and K. Masukawa\*\*\*, The University of Tokyo, \*JAXA, \*\*National Institutes for Quantum and Radiological Science and Technology, \*\*\*Mitsubishi Heavy Industries, Ltd.*

SOI SRAMs supported by a thin BOX film have been exposed to wide-range high-energy heavy ions for simulating terrestrial and galactic radiation impacts. Experimental results have demonstrated that a back-bias approach leads to a 100-times increase in their soft-error sensitivity compared to the counterpart zero-bias situation. This is attributed to that back biasing enhances radiation-induced potential fluctuation under BOX, which spreads and causes multi-cell errors in the top SOI circuits via the capacitance coupling principle.

11:35 a.m.

### **3D.3 Thermal Neutron-Induced Soft-Error Rates for Flip-flop Designs in 16-nm Bulk FinFET Technology,**

*H. Zhang, H. Jiang, J. Brockman\*, T. Assis\*\*, X. Fan, B. Bhuva, B. Narasimham\*\*\*, S.-J. Wen^ and R. Wong^, Vanderbilt University, \*University of Missouri Research Reactor Center, \*\*Robust Chip, Inc., \*\*\*Broadcom Corporation, ^Cisco Systems, Inc.*

12:00 p.m.

### **3D.4 Influence of Polonium Diffusion at Elevated Temperature on the Alpha Emission Rate and Memory SER Performance**

*B. Narasimham, E. Ogawa, J. K. Wang, S. Gupta, D. Reed, B. Mitra, H. Luk, X. Zhang, J. Yeung, H.-Y. Ho and J. Dull, Broadcom Limited*

## ***Session 3E - Reliability Testing***

Session Chairs: *Hosain Farr, Qualitua, Kevin Manning, Analog Devices*

Wednesday, April 5

Regency I

10:40 a.m. - Session Introduction

10:45 a.m.

### **3E.1 TAISAM: A Transistor Array-Based Test Method to Characterise Ion-Induced Sensitive Area**

*R. Song, S. Chen, Y. Chi and Z. Wu, National University of Defense Technology*

This paper presents a transistor array-based test method called TAISAM. It is used to characterise the ion-induced sensitive area. The measured ion-induced sensitive area is 1.75  $\mu\text{m}^2$  and 1.00  $\mu\text{m}^2$  when the LET is 37.6 and 15.3 MeV-cm<sup>2</sup>/mg. The source of the transistor and the well contact can affect the ion-induced sensitive area.

11:10 a.m.

### **3E.2 Test Method for Moisture-Driven Failure: Effect of VLSI Device Self-heating and Local Temperature Rise**

*N. Lajo, E. Armagan, F. Chai and S. Padiyar, Intel Corporation*

Peck's model for humidity test correlation is well studied and applied in semiconductor industry. Effect of environment temperature and humidity to failure rates at stress or at use condition are recognized in the model. This paper discusses the effect of device Self Heating on accelerated reliability stress with supporting data and results.

11:35 a.m.

### **3E.3 Ultrafast Pulse Characterization of Hot Carrier Injection Effects on Ballistic Carrier Transport for Sub-100 nm MOSFETs**

*R. Cheng, X. Yu, B. Chen, L. Shen\*, L. Yin\*, Y. Zhang, Z. Zheng, X. Liu\* and Y. Zhao, Zhejiang University, \*Peking University*

We investigate the effect of hot carrier injection on the ballistic transport characteristics of SOI MOSFETs for the first time. During HCI stress, the traps and defects generated in the transistor channel would increase the carrier scattering and degrades the ballistic efficiency. The effect of this degradation changes with gate length. In addition, ultrafast pulsed measurement were employed to exempt the SHE, yielding more realistic results for the reliability estimation.

12:00 p.m.

### **3E.4 Comparison of RTN and TDDS Methods for Trap Extraction in Trigate Nanowires**

*A. Tsiara, X. Garros, A. Vernhet, S. Barraud, O. Faynot, G. Ghibaudo\* and G. Reimbold, CEA, LETI, MINATEC, \*IMEP-LAHC*

TDDS and RTN measurements are used to investigate the impact of the defects in the reliability of nanoscaled PMOS devices and, mostly, to make a comparison between the two trap detection methods. This procedure was followed for three different geometries, in the first part of our setup, while in the second we make a comparison of the results, before and after stress.

## ***Session 3F - ESD/Latch-Up***

Session Chairs: *Farzan Farbiz, Texas Instruments, Michael Khazhinsky, SI Labs*

Wednesday, April 5

Regency IV

10:40 a.m. - Session Introduction

10:45 a.m.

### **3F.1 ESD Behavior of Large Area CVD Graphene RF Transistors: Physical Insights and Technology Implications**

*N. K. Kranthi, A. Mishra, A. Meersha and M. Shrivastava, Indian Institute of Science*

We report ESD investigations on top-gated mono-layer graphene FETs. Impact of mode of carrier transport and gate configuration on failure mechanism is investigated. A unique contact limited failure in graphene transistors is reported. Physical insights on current saturation in graphene FET and unique step-by-step failure in dielectric-capped transistors is presented. Degradation under ESD time scales and its implications

on current saturation are revealed. Influence of various top-gate designs on the ESD performance is reported.

11:10 a.m.

### **3F.2 New Voltage Controlled Diode For Power Rail And Regulator ESD Protection**

*J.-H. Lee, N. M. Iyer, R. Jain, G. Zhang and M. Prabhu, GLOBALFOUNDRIES Inc.*

For the first time, a novel diode structure is successfully designed to protect the ESD stress condition in the high voltage CMOS technology nodes. Controlled by the voltage difference between VDD and signal, the depletion regions of two HV-NW's can shut off or turn on the current path to the ground (GND) of the diode depending on whether it is under normal operation mode or ESD event.

11:35 a.m.

### **3F.3 ESD Ballasting of Ge FinFET ggNMOS Devices**

*R. Boschke, S.-H. Chen\*, M. Scholz\*, G. Hellings\*, D. Linten\*, L. Witters\*, N. Collaert\* and G. Groeseneken, KU Leuven, \*imec*

Five SD stacks - Ge, SiGe, SiGe + thin or thick Si, Si - on Ge ggNMOS FF devices are studied wrt ESD failure level and Ron. Small series resistance due to low contact and SD resistance results in very low Ron, but can harm the ESD robustness shown for resistivity for all Si contacted options. It was demonstrated that a longer contact length and gate length can improve the ESD robustness for these options.

## ***Session 4A - 3D/2.5D/Packaging***

Session Chairs: *Alan Lucero, Intel, Sudarshan Rangaraj, Amazon Lab126*

Wednesday, April 5

Regency Main

2:15 p.m. - Session Introduction

2:20 p.m.

### **4A.1 CPI Advancement in Integrated Fan-Out (InFO) Technology (Invited)**

*D. Yu, J. Yeh, T.-S. Lin and KC Yee, Taiwan Semiconductor Manufacturing Company*

2:45 p.m.

### **4A.2 Impact of TSV Process on 14nm FEOL and BEOL Reliability**

*S. Kannan, C.S. Premachandran, D. Smith, R. Ranjan, S. Cimino, K. B. Yeap, G. Wu, L. Cao, M. Prabhu, R. Agarwal, W. Yao, L. England and P. Justison, GLOBALFOUNDRIES*

Evaluating the impact of TSV process on the front-end of line (FEOL) devices and back-end of line (BEOL) structures is essential for advanced packaging applications including 3D integration. This paper presents the impact of TSV process on wafer level reliability with respect to FEOL and BEOL reliability aspects. A TSV proximity study was performed by placing the TSV at various KOZ distances of 2 $\mu$ m to 7 $\mu$ m; and different orientations of horizontal, vertical, and 45 degrees.

3:10 p.m.

### **4A.3 Observations of Copper (Cu) Transport in Through-Silicon Via (TSV) Structure by Electrical Characterization for its Reliability Evaluation**



*J. M. Chan, C. S. Tan, K. C. Lee\*\*, X. Cheng\*, W. Kanert\* and Nanyang Technological University, \*Infineon Technologies AG, \*\*Infineon Technologies Pte Ltd.*

Observations and control of Cu transport in TSV structure were demonstrated. This allows analysis to be carried out in stages, monitoring Cu transport from the Cu TSV, through the barrier, dielectric and into the silicon substrate. These observations provide insights to critical parameters allowing Cu transport through the layers. Observation of Cu ions in the silicon substrate which alters neighbouring device performances, and the dielectric reliability in the presence of Cu ions, will be discussed.

3:35 p.m. – Break

4:05 p.m.

#### **4A.4 Reliability Tests for Modelling of Relative Humidity Sensor Drifts**

*S. Jose, F. Voogt, C. van der Schaar, S. Nath, N. Nenadovic\*, F. Vanhelmont\*, E. J. Lous\* H. Suy\*, M. in't Zandt\*, A. Sakic\*, A. Abdelrazek\* and G. Calaerts\*, NXP Semiconductors Nijmegen, \*AMS Netherlands BV Eindhoven*

There are several RH sensors available in the market, however a methodology to evaluate sensor's capability to reliably measure Relative Humidity(RH) is not available. In this paper we discuss two types of sensor drifts and methods to measure them. We also introduce a novel test methodology Relative Humidity Cycling (RHCL) test to estimate real time sensor drift over long-term use. We propose RHCL as a methodology to evaluate, qualify and benchmark RH sensors.

4:30 p.m.

#### **4A.5 A Study of Self- and Mutual-Heating in Wafer Level Packaging Systems**

*C. Hau-Riege, H. Farr\*, G. Xu, QJ Zhang, and Y.W. Yau, Qualcomm Technologies, Inc., \*Qualitau, Inc.*

A detailed investigation of the Joule heating for today's printed circuit board has been characterized according to metal layer, trace width, and ambient conditions. When compared to a long-standing industry specification, significant margin in current-carrying capability was observed, which can alleviate design constraints for printed circuit board layout. Additionally, mutual heating between the chip and board was assessed for product-like conditions. Finally, metrics are proposed for both two- and three-dimensional PCB trace heat flow.

4:55 p.m.

#### **4A.6 A Unique Failure Mechanism Induced by Chip to Board Interaction on Fan-Out Wafer Level Package**

*C.K. Yu, W.S. Chiang, N.W. Liu, M.Z. Lin, Y.H. Fang, M.J. Lin, B. Lin and M. Huang, MediaTek Inc.*

A unique failure mechanism was first observed by an innovative test methodology in interconnects of FOWLP induced by CBI under thermal stress gradient. Circular cracks were detected on passivation and RDL owing to mismatched thermal expansion among modules. CBI were studied and improved by appropriate passivation properties, fine-tuned process window, optimized RDL patterns and suitable solder ball material. A novel simulation model was established and an in-house design guideline was generated for reliability robustness.

## **Session 4B - Wide Band-Gap**

Session Chairs: *Denis Marcon, imec, Sandeep Bahl, Texas Instruments*

Wednesday, April 5

Regency I

2:15 p.m. - Session Introduction

2:20 p.m.

### **4B.1 GaN-Based MIS-HEMTs: Impact of Cascode-Mode Stress on NBTI Shift**

*S. Dalcanale, M. Meneghini, A. Tajalli, I. Rossetto, M. Ruzzarin, P. Moens\*, A. Banerjee\*, S. Vandeweghe\*, E. Zanoni and G. Meneghesso, Univeristy of Padova, \*Onsemiconductor*

The aim of this paper is to investigate the reliability of cascoded HEMTs in off-state operation. We demonstrate that in subthreshold bias, the flow of a constant source current in the channel (with high VDS) may be beneficial, strongly reducing the overall NBTI  $V_{th}$  shift with respect to the case of standard HTRB stress. To demonstrate this result we adopt a specific stress protocol that emulates the real-life operation of cascoded HEMTs.

2:45 p.m.

### **4B.2 Reliability of Hybrid-Drain-embedded Gate Injection Transistor**

*K. Tanaka, T. Morita, M. Ishida, T. Hatsuda and T. Ueda, K. Yokoyama\*, A. Ikoshi\*, M. Hikita\*, M. Toki\*, M. Yanagihara\*, Y. Uemoto\*, Panasonic Corporation, \*Panasonic Semiconductor Solutions Co., Ltd.*

We performed High Temperature Reverse Bias (HTRB) test on the Hybrid-Drain-embedded Gate Injection Transistors (HD-GITs), and found that the lifetime depends on the leakage current before the HTRB test. We extracted the acceleration factors for the temperature and reverse bias voltage. Based on the obtained conclusions, we designed reliable devices whose lifetimes are sufficiently long for conventional power converter applications.

3:10 p.m.

### **4B.3 OFF-state TDDB in High-Voltage GaN MIS-HEMTs**

*S. Warnock and J. del Alamo, Massachusetts Institute of Technology*

We have investigated time-dependent dielectric breakdown (TDDB) in high-voltage AlGaIn/GaN MIS-HEMTs in the OFF state. We have developed a novel methodology using ultraviolet light that allows us to separate permanent effects of dielectric degradation from transient behavior due to trapping after high voltage stress. This new approach reveals unmistakable evidence of TDDB in the OFF state.

3:35 p.m. – Break

4:05 p.m.

### **4B.4 Failure Modes for p-GaN Gates under Forward Gate Stress with Varying Mg Concentration**

*S. Stoffels, A. N. Tallarico\*, C. Fiegna\*, B. Bakeroot\*\*, T.-L. Wu, D. Marcon, N. E. Posthuma and S. Decoutere, imec, \*University of Bologna, \*\*Ghent University*

In this work we will study the degradation of p-GaN gates subjected to forward gate stress. The degradation will be studied for either a high ( $2.6 \times 10^{19}/\text{cm}^3$ ) or low active Mg concentration ( $3 \times 10^{18}/\text{cm}^3$ ) in the p-type doped region of the gate. The degradation kinetics will be studied for these devices and a TCAD model will be presented which can give qualitative insight in the physics of a device after failure.

4:30 p.m.

#### **4B.5 Degradation of GaN-HEMTs with p-GaN Gate: Dependence on Temperature and on Geometry**

*M. Meneghini, I. Rossetto, M. Borga, G. Meneghesso, E. Canato, E. Zanoni, C. De Santi, F. Rampazzo, S. Stoffels\*, M. Van Hove\*, N. Posthuma\* and S. Decoutere\*, University Padova, \*imec*

This paper investigates the dependence of the degradation kinetics of GaN-HEMTs with p-GaN gate on temperature and device geometry. The analysis is based on combined experimental analysis and 2D simulations. We demonstrate that the TTF has an exponential dependence on stress voltage. We suggest that the time-dependent degradation is caused by a defect generation process taking place in the p-GaN layer.

### ***Session 4C - Circuit Reliability/Aging***

Session Chairs: *Vijay Reddy, Texas Instruments, Chris Kim, University of Minnesota*

Wednesday, April 5

Regency IV

2:15 p.m. - Session Introduction

2:20 p.m.

#### **4C.1 Physically Unclonable Function using CMOS Breakdown Position**

*K.-H. Chuang, E. Bury, R. Degraeve\*, B. Kaczer\*, G. Groeseneken, I. Verbauwhede and D. Linten\*, KU Leuven, \*IMEC*

This paper discussed a novel physically unclonable function (PUF) utilizing the intrinsic randomness of the oxide breakdown positions for hardware security applications. The breakdown PUF (BD-PUF) arrays were designed and fabricated in a commercial 40nm CMOS process. We demonstrate the feasibility of this implementation. With the experimental results and an analysis on oxide physics, we also show that BD-PUF has all the important properties of PUF including randomness, uniqueness and thermal stability.

2:45 p.m.

#### **4C.2 Investigation of HCI Effects in FinFET Based Ring Oscillator Circuits and IP Blocks**

*Y. Kim, H. Shim, M. Jin, J. Bae, C. Liu and S. Pae, Samsung Electronics*

HCI effect with circuits running at very high frequency through overdrive can manifest under very long stress time and lower temperature where NBTI is suppressed. On FinFET technology with presence of self-heating effects, it is important to decouple the effects to obtain accurate HCI modeling along with right duty cycle. We'd devised a unique RO test structure to characterize HCI duty cycle and compare with HCI duty extracted from the RO and IP aging results.

3:10 p.m.

#### **4C.3 A Novel On-Die GHz AC Stress Test Methodology for High Speed IO Application**

*P.-Z. Kang, T.-Y. Yew, K.-W. Shih, M.-H. Hsieh, W.-S. Chou, C.-M. Fu, Y.-C. Huang, W. Wang, Y.-C. Peng and Y.-H. Lee, Taiwan Semiconductor Manufacturing Company*

In this paper, an on-die wave front generator was established in circuit level. Experiments in this study cover from subjects of off state, BTI and HCI. Based on the extensive results, strong dependence of reliability to layout effect can be concluded. And the reliability guidelines and recommendations for high speed IO circuit design can be made.

3:35 p.m. – Break

4:05 p.m.

#### **4C.4 Reliability Compact Modeling Approach for Layout Dependent Effects in Advanced CMOS Nodes**

*C. Ndiaye, R. Berthelon, V. Huard, A. Bravaix\*, C. Diouf, F. Andrieu\*\*, S. Ortholland, M. Rafik, R. Lajmi, X. Federspiel and F. Cacho, STMicroelectronics, \*ISEN REER-IM2NP, CEMES-CNRS, \*\*CEA-LETI*

We analyse and model the layout dependent effects (LDE) found in pMOSFET transistors on 14nm UTBB FDSOI CMOS technology. Experiments show that changing the layout has an impact on  $V_{th}$ , on NBTI reliability and on Ring Oscillator (RO) Frequency Drift. Compacts model taking account the impact of LDE on  $V_{th}$ , NBTI reliability, and RO frequency is proposed. Measurement data are fitted with compact model and the obtained results are in very good agreements with modelling.

4:30 p.m.

#### **4C.5 Reliability of 2T-core CMOS OTP Non-Volatile Memory Bitcells**

*R. Ranjan, T. Nigam, Y. Liu, A. Gondal, A. Kerber, M. I. Natarajan and B. Parameshwaran, J. Versaggi and E. Ehrichs GLOBALFOUNDRIES, US, Inc.*

Reliability assessment of 2T CMOS antifuse bitcell, consisting of two core NMOSFETs having a program transistor (WP) coupled in series with a select transistor (WR), is presented. Key contributors to minimum programming voltage ( $V_{pmin}$ ) and maximum programming voltage ( $V_{pmax}$ ) under programming/inhibit stage stress were identified. It is suggested that stronger WR and lowering the junction leakage between middle node of Wp/WR and substrate will be helpful in providing a more robust memory technology.

4:55 p.m.

#### **4C.6 Thermally-aware Sensor Placement for Real-time Monitoring and Mitigation of FEOL Aging in System-on-Chip (SoC) Applications**

*H. Kufluoglu, M. Chen, S. Lu, A. Rabindranath, R. Kakoe and S.-H. Hu, Qualcomm Inc.*

A novel aging sensor design, thermally-aware allocation, selection and degradation compensation capability are presented. High resolution, multiple use-case thermal characterization and identification of the temperature sensitive sections of the chip are described. The verification of the sensor based technique is shown with data from current technology nodes. These techniques enable controlling the FEOL aging without exceeding the power requirements of SoC applications.

### **Wednesday Evening - Posters April 5, 2017**

#### ***3D/2.5D/Packaging***

##### **PA.1 Evidence of Mechanical Degradation in Microelectromechanical Switches Subjected to Long-Term Stresses**

*M. Barbato, A. Barbato, A. Cester, V. Mulloni\*, M. Silvestrini, and G. Meneghesso, University of Padova, \*Centre for Materials and Microsystems*

This paper presents an analysis of the degradation of Radio Frequency (RF) Microelectromechanical Switches (MEMS) subjected to long term stresses. We report the results obtained on two different types of devices respectively with (a) straight and (b) meander anchors. Results show that the use of straight anchors results in a better robustness towards viscoelastic mechanical degradation and in a higher reliability to stiction phenomenon during long term stresses.

### **PA.2 Electromigration Behavior in Aluminum Wires for Power Base-station Applications**

*P. van der Wel, R. Otte, H. Roberts, F. de Bruijn\*, A. van Zuijlen\* and B. Merkus\*, NXP Semiconductors, \*Ampleon*

A qualitative study of electromigration in 50um Aluminum (with 1% Si) wires as used in base station products is presented. During the electromigration stressing, three phases are observed: 1) Bamboo formation (grains>50um) while resistance increases 2) Bamboo displacements while resistance decreases 3) wire deformation and resistance increase towards total destruction. Experiments have been performed to obtain the Black's parameters. With these, an extrapolation to user conditions has been made.

### **PA.3 Model to Establish Relation between Residual Thermal Stress and Loss of Luminosity of High Power LEDs**

*B. R. Ankit, B. S. Dhakad, A. Chatterjee and U. S. Dixit, Indian Institute of Technology Guwahati*

Packaging issue due to the residual stress transfer from Solders to the LED generate highly stressed middle section, which leads to different intensity light output from the highly-stressed region. Parametric study of solder height and stress profile is done at various temperatures. This study is used to show the relation between level of defects in the wafer due to stress in different region and relation with loss in light output.

## ***Circuit Reliability/Aging***

### **CR.1 A CDM-like Damage Mechanism for Multiple Power Domains Fabricated with Deep N-well Processes**

*Y.-L. Chu, H.Y. Chuo, J.W. Young, Y.S. Tsai, C.Y. Ko, M-Y. Wang, C.L. Chang, B. Kiang and K. Wu, TSMC Ltd.*

a new mechanism of CDM (Charged-Device Model)-like damage is observed across separated power domain interfaces. This new mechanism is modeled and validated by test patterns in a 40 am logic process and by SPICE simulation. The damage mechanism is found to be unlike the traditional CDM and can be observed in wafer form, which means that such damage should be generated during the chip fabrication process. Prevention of damage is proposed and verified.

### **CR.2 Adaptive Accelerated Aging with 28nm HKMG Technology**

*D. Patra, A. Reza\*, K. Hassan\*, M. Katozzi\*\*, E. Cannon\*\*, K. Roy\* and Y. Cao, Arizona State University, \*Purdue University, \*\*The Boeing Company*

Adaptive Accelerated Aging method is targeted at controlled stress of the DUTs to the end of their lifetime within one hour, which is usually defined by gate dielectric breakdown. In addition, this accelerated process is adaptive to the device response, i.e., a weaker device with higher level of defects will fail faster while a better device will degrade less or even not get damaged during the stress test.

### **CR.3 Impact of BTI on Dynamic and Static Power: From the Physical to Circuit Level**

*H. Amrouch, S. Mishra\*, V. van Santen, S. Mahapatra\* and J. Henkel, Karlsruhe Institute of Technology (KIT), \*Indian Institute of Technology (IIT) Bombay*

We investigate from the physical to circuit level the impact of BTI on the dynamic and static power of circuits based on our proposed aging-aware cell library. We demonstrate how considering solely threshold voltage leads to a significant overestimation of the aging-induced power reduction due to the compensation

of other degradations in MOSFET parameters. Our library is compatible with existing commercial synthesis tools allowing designers to seamlessly analyze the impact of BTI on circuits' power.

#### **CR.4 SRAM Enablement Beyond N7: A BTI Study**

*M. Gupta, P. Weckx\*, S. Cosemans\*, P. Schuddinck\*, R. Baert\*, D. Jang\*, Y. Sherazi\*, P. Raghavan\*, B. Kaczer\*, A. Spessot\*, A. Mocuta\* and W. Dehaene, KU Leuven, \*imec*

High density (HD) SRAM Vmin improvement with scaling is halted due to variability and aging effect which become a bottleneck for energy optimized operation. Device level and cell level advancements help the SRAM in lowering Vmin. Moreover assist techniques become beneficial in Vmin lowering but due to BTI their Vmin degrades. BTI sensitivity analysis for these solutions gives the insight of BTI resilient HD SRAM design for advance technology node.

#### **CR.5 Efficient Prediction of 28nm Path Delay Degradation under Activity Uncertainty**

*D. Patra, A. Bansal, R. Rao\*, W. Li\*, E. Shimelis\*, A. Ramamurthy\* and Y. Cao, Arizona State University, \*Microsemi Corp.*

Even at 28nm HKMG, a typical reliability analysis uses SPICE, which is inefficient for large-scale digital design. Moreover, PDK doesn't describe well the physics of recovery in BTI, causing a significant overestimation of path delay degradation. In this work, we evolve System Reliability Analyzer (SyRA)-X for gate-level aging prediction with robust analysis under activity uncertainty. The aging analysis of path delay with fixed activity at each gate gives a safe and tight prediction.

#### **CR.6 Towards On-line Estimation of BTI/HCI-induced Frequency Degradation**

*M. Altieri, S. Lesecq, E. Beigne and O. Heron\*, CEA-LETI, \*CEA-LIST*

This work proposes a new bottom-up approach for on-line estimation of circuit degradation. Built on the top of device-level models, it takes into account all factors that impact global circuit aging, i.e.: process, topology, workload, voltage and temperature variations. The proposed model allows an accurate evaluation of the degradation of the circuit critical paths during its operation. The model is fed by voltage and temperature monitors that on-line track dynamic variations.

#### **CR.7 Defect-based Compact Modeling for RTN and BTI Variability**

*P. Weckx, M. Simicic, K. Nomoto\*, M. Ono\*, B. Parvais, B. Kaczer, P. Raghavan, D. Linten, K. Sawada\*, H. Ammo\*, S. Yamakawa\*, A. Spessot, D. Verkest and A. Mocuta, imec, \*Sony Semiconductor Solutions*

A defect-centric approach of modeling workload dependent BTI and RTN degradation capturing both the mean and stochastic behavior in a combined way is introduced. Using a novel Verilog-A based wrapper a wide range of SPICE analyses and BTI workload degradation abstraction levels are covered. All BTI related electrostatics and kinetics are incorporated in standard EDA-tools as a 'black box' without any custom simulation flow.

#### **CR.8 Architecture- And Workload-Dependent Digital Failure Rate**

*A. Sivadasan, S. Mhira, A. Notin, A. Benhassain, V. Huard, E. Maurin, F. Cacho, L. Anghel\* and A. Bravaix\*\*, STMicroelectronics, \*TIMA, \*\*ISEN-REER, IM2NP*

In this work, we demonstrate various novel methodologies to take into account more accurately the duty cycle dependence of NBTI degradation in digital products. The main outcome of this paper is a consistent, silicon-proven methodology to evaluate failure rates at early design stages as a function of digital architecture and workloads. This work opens the way to new developments towards optimal

performance/reliability trade-off at architectural level as well as product hardening for safety-critical applications.

### ***Dielectrics-Gate, MOL, BEOL***

#### **DG.1 Time Dependent Dielectric Breakdown of SiN, SiBCN and SiOCN Spacer Dielectrics**

*R. Southwick III, E. Wu, S. Mehta and J. Stathis, IBM*

Close proximity of the contact to gate requires lower dielectric constant materials to reduce the parasitic capacitance and meet AC performance targets. Here we investigate the TDDB reliability of two possible low-k spacer dielectrics: SiBCN and SiOCN and compare that to the traditional SiN and SiO<sub>2</sub> dielectrics. Using the Self-Consistent-Poisson-Statistics approach we indicate the acceleration model which best describes the failure statistics and point out many of the similarities of spacer dielectric breakdown to SiO<sub>2</sub>.

#### **DG.2 Field Acceleration Factor Extraction in MOL and BEOL TDDB**

*T. Shen, K. B. Yeap, C. Christiansen and P. Justison, GLOBALFOUNDRIES*

Recently a BEOL and MOL TDDB reliability test and fail rate projection methodology based on large data analysis was proposed and studied. However the extraction of one of the key model parameter, the field acceleration factor  $\gamma E$  was flawed, which leads to a pessimistic projection. In this work, the fundamental issues with current method are systematically studied. A more realistic and robust method is then proposed, for a more accurate reliability projection.

#### **DG.3 Impacts of Censoring on Lifetime Analysis by Two-step Probability Plot in Defect Clustered TDDB**

*S. Yokogawa, The University of Electro-Communications*

Lifetime distribution characteristics of MOL/BEOL TDDB with defect clustering were investigated by using 2-step probability plot. This method was proposed to estimate parameters of the time-dependent clustering model. In first step, clustering parameter is estimated by a linearization procedure on a proposed chart. In second step, shape and scale parameters are estimated by slope and intercept of the plot. Impacts of censoring are investigated statistically by using Monte-Carlo simulation and mean squared error of estimators.

#### **DG.4 A Stochastic Model for Impact of LER ON BEOL TDDB**

*R. Muralidhar, E. Wu, T. Shaw, A. Kim, B Li, P. McLaughlin, J. Stathis and G. Bonilla, IBM Thomas J. Watson Center*

This paper presents a new Monte-Carlo based model to assess the impact of line edge roughness (LER) on BEOL TDDB. It shows that LER generally impacts key quantities,  $t_{63}$ , Weibull beta as well as apparent acceleration parameter of field acceleration model all of which impact projection of TDDB lifetime at operating conditions. The paper also shows that the field dependence is dependent on underlying field acceleration model (root E or power law).

#### **DG.5 TDDB in HfSiON/SiO<sub>2</sub> Dielectric Stack: Büttiker Probe Based NEGF Modeling, Prediction and Experiment**

*A. K. Reza, M. K. Hassan, K. Roy, D. Patra\*, A. Bansal\*, Y. Cao\* Purdue University, \*Arizona State University*

Here we have demonstrated and experimentally verified a Büttiker probe based leakage current model in HfO<sub>2</sub> based high- $\kappa$  metal gate transistor for determining the gate leakage current due to the pre-existing

and post-stress defects as well as breakdowns in the dielectric layers. Also this method is integrated with percolation model to predict the time to failure of the device and required stress condition to observe breakdown in the device within a certain period of time.

#### **DG.6 Hole Trap Effect on Time-dependent-Dielectric Breakdown (TDDB) of High-Voltage Peripheral nMOSFETs in flash Memory Application**

*G. Jiao, S. Baek, K.-j. Nam, S.-I. Chang, S. Cho, T. Kauerauf, C. Lee, S.-U. Han, J.-S. Kim, E.-A. Chung, Y.-C. Shin, J. Lim, Y.-G. Shin and K. Hwang, Samsung Electronics*

In this work, the TDDB mechanism in high-voltage nMOSFETs with high-density of pre-existing defects in the gate oxide is investigated. In contrast to the traditional nMOSFETs with very few defects in the gate oxide, the additional hole trapping through the stress-induced generated defects close to the gate side not only induce longer fail time, but also induce smaller voltage acceleration factor and lower 10-year  $V_{max}$

#### **DG.7 Impact of SiO<sub>2</sub>/Si Interface Micro-roughness on SILC Distribution and Dielectric Breakdown: A Comparative Study with Atomically Flattened Devices**

*H. Park, T. Goto, R. Kuroda, A. Teramoto, T. Suwa, D. Kimoto and S. Sugawa, Tohoku University*

By measuring QBD and SILC characteristics of the conventional and the atomically flattened SiO<sub>2</sub>/Si interface, the impact of the micro-roughness on QBD and SILC has been investigated. It was found that both the numbers of the defects inducing QBD and SILC are reduced by applying the atomically flat SiO<sub>2</sub>/Si interface. It is clarified that the SiO<sub>2</sub>/Si interface micro-roughness is one of the origins that induce the anomalous SILC, due to localized electric field concentration effect.

#### **DG.8 Gate Stack Engineering to Enhance High-k/metal Gate Reliability for DRAM I/O Applications**

*B. O'Sullivan, R. Ritzenthaler, E. Simoen, E. D. Litta, T. Schram, A. Chasin, Y. Ji\*, D. Linten, V. Machkaoustan\*\*, P. Fazan\*\* and N. Horiguchi, imec, \*SK Hynix, \*\*Micron Technology Belgium*

Integration of high-k metal-gate stacks into high-voltage DRAM I/O devices can enable continued scaling, together with introducing significant reliability challenges. We present and rationalise the dramatic improvement in NBTI robustness resulting from fluorine incorporation in the high-k layer or application of TaN electrode.

#### **DG.9 Conductivity and Reliability of 28nm FDSOI Middle of the Line Dielectrics**

*X. Federspiel, D. Nouguier, T. Ya and D. Ney, STMicroelectronics*

With shrinking of gate to contact distance as well as poly routing to active distance, middle-of-the line dielectrics reliability become challenging to design compacity. We performed reliability tests on poly to contact and poly to active configuration and found a consistent breakdown field, conduction mechanisms and time to breakdown. Besides, we found that TDDB variability is dominated by die to die variation as shown by previous studies.

#### **DG.10 Impact of AC Voltage Stress on Core NMOSFETs TDDB in FinFET and Planar Technologies**

*R. Ranjan, Y. Liu, T. Nigam, A. Kerber and B. Parameshwaran, GLOBALFOUNDRIES, US, Inc.*

In this work, we explore the impact of AC stress voltage, frequency and duty cycle, on HK/metal gate core NMOSFET TDDB in FinFETs and planar technologies. Power on AC/DC ratio of  $\geq 63\%$  increases with frequency and duty cycle for both FinFET and planar devices. In addition, Weibull  $\beta$  shows a reduction at



high frequencies while voltage acceleration increases. 100mV gain in the product  $V_{max}$  is estimated under high frequency AC stress compared to DC stress.

## ***ESD/Latch-Up***

### **EL.1 Latchup in Bulk FinFET Technology**

*C.-T. Dai, S.-H. Chen, D. Linten, M. Scholz, G. Hellings, R. Boschke, J. Karp\*\*, M. Hart\*\*, G. Groeseneken, M.-D. Ker\*, A. Mocuta and N. Horiguchi, imec, \*National Chiao-Tung University and \*\*Xilinx*

Latchup (LU) had been considered to be less important in advanced CMOS technologies. However, I/O interface and analog applications can still operate at high voltage (e.g., 1.8V or 3.3V) in sub-20nm bulk FinFET technologies. LU threats are never eliminated and the sensitivity towards LU is increased in bulk FinFET technology.

### **EL.2 New Triggering-Speed-Characterization Method for Diode-Triggered SCR Using TLP**

*M. Mahane, D. Tremouilles\*, M. Bafleur\*, B. Thon, M. Diatta and L. Jaouen, STMicroelectronics Tours SAS, \*LAAS-CNRS, Université de Toulouse, CNRS, UPS*

One of the key disadvantages of the Diode Triggered SCR (DTSCR) as a RF ESD protection, is the turn-on time during very fast ESD transients. At this time, there is no normalized method to evaluate the ESD device turn on speed. Such a method would be required to effectively compare devices performances. In this work a new method, based on stored-charge, is investigated to characterize the triggering speed using Transmission Line Pulsing (TLP) measurements.

### **EL.3 Abnormal IO Failure Caused by the HBM Induced MM-Like ESD Event**

*J.-H. Lee and N. M. Iyer, GLOBALFOUNDRIES Inc*

In this paper, IO failure caused by a new mechanism during the HBM event of the NC pin is reported. Although the IO can pass HBM 2kV, it is damaged after a 0.5kV HBM event at a NC pin. Moreover, the failure IO is not necessary at the adjacent pin of the NC pin.

### **EL.4 Embedded Shunt Diode Pair to Suppress Overshoot Voltage**

*L. He, J. A. Salcedo\*, S. Parthasarathy\*, P. Zhou\*, J.-J. Hajjar\*, A. Dong and J. J. Liou\*\*, University of Central Florida, \*Analog Devices, \*\*Zhengzhou University*

An EMC (electromagnetic compatibility) bidirectional blocking voltage protection clamp for narrow design window interface applications is introduced. To suppress the overshoot voltage of this device, embedded avalanche diodes accelerate the transition of the clamp to the on-state. By embedding the avalanche-driven triggering mechanism, this device provides a fast turn-on speed without compromising its high current handling capability. The device physics insight and design optimization is demonstrated via numerical simulations.

## ***Failure Analysis/Process Integration***

### **FA.1 $V_{ce}$ as Early Indicator of IGBT Module Failure Mode**

*K. Pedersen, P. Kristensen, K. Pedersen, C. Uhrenfeldt, S. Munk-Nielsen, Aalborg University*

A monitoring methodology able to separate failure modes in IGBT modules is applied during active thermal cycling and used for early estimation of component lifetime. The concept renders it possible to run low load testing, normally requiring a long test period, and still provide viable lifetime models. In the present work

especially the separation of solder and bond wire fatigue is addressed. All results are supported with detailed micro-scale failure analysis.

### **FA.2 ATE and Lock-in Thermography Coupling Techniques for a 3D Defect Localization in a 4 Stacked Die Memory**

*N. Courjault, K. Sanchez\*, F. Messenger\*\* and F. Infante, Intraspec Technologies, \*French Space Agency, \*\*Thales Communications & Security*

In this paper we propose a new methodology consisting in coupling an Automatic Test Equipment (ATE) system to a failure localization system, and more specifically Lock-in Thermography. This allows the localization of the defective die inside a stack of 2 or more chips by alternatively activating different areas of the device.

### **FA.3 Effect of Contact Field Plate on Hot-Carrier-Induced On-Resistance Degradation in n-Drain Extended MOS Transistors**

*W. Lin, C. Cheng, R. Jain, P.R. Verma and U. Singh, GLOBALFOUNDRIES Semiconductor Corp*

In this paper, one new concept of Contact Field Plate is carried out, Contact Field Plate on drift region results in less bulk current and improved Ron degradation. Contact field plate on drift region is a promising concept on medium voltage EDNMOS application in terms of better HCI reliability capability.

### **FA.4 Investigation on the Local Variation in BCAT Process for DRAM Technology**

*S. Jeon, J. Choi, H.-C. Jung, S. Kim and T. Lee, Samsung Electronics Co.*

The local variation of fin height plays a vital role in determining a performance of DRAM and this variation is caused by a subtle difference during the process. We discovered that the active dimension and profile is the key factor to improve this local variation and suggest that a measurement of a threshold voltage in an array of cell transistor could be the effective method to figure out a degree of local variation.

### **FA.5 Demonstration of Sufficient BTI Reliability for a 14-nm finFET 1.8V I/O Technology Featuring a Thick ALD SiO<sub>2</sub> IL and Ge p-channel**

*G. Hellings, A. Subirats, J. Franco, T. Schram, L.-A. Ragnarsson, L. Witters, R. Boschke\*, P. Roussel, D. Linten and N. Horiguchi, imec, \*KU Leuven*

1.8V I/O transistors were fabricated in a 14-nm bulk finFET technology, using 2-3nm Atomic Layer Deposition (ALD) SiO<sub>2</sub> in a high-k/metal gate stack. PBTI characterization showed negligible degradation at the operating VDD, with nFET VOV<sub>max</sub> exceeding 2.2V. To boost the NBTI reliability, we propose a Ge channel for the I/O pfinFET to reduce the interaction of channel holes with the ALD SiO<sub>2</sub> defects. This allows to demonstrate pFET BTI reliability on-par with the Si-channel nFET counterpart.

## ***Metallization Reliability***

### **MR.1 Influence of Ti-Al(Cu) Backend Layer Scheme on Repetitive-power-pulsing Robustness**

*A. Mann, H. Lohmeyer and Y. Joseph\*, Robert Bosch GmbH, Automotive Electronics, \*Technische Universität Bergakademie Freiberg*

We investigate thermomechanical robustness of Ti-Al(Cu) backend-of-line variants for application of smart-power IC using integrated power stages as low side switches for control of inductive loads, e.g. magnetic valves. In particular influence of layer thickness, Ti/TiN layer and barrier scheme is studied and trade-off with current density capability is discussed.

## **MR.2 Differences in Reliability Effects for Thick Copper and Thick Aluminum Metallizations**

*M. Pohl, M. Erstling, V. Hein, T. Chen\* and K. Weide-Zaage\*, X-FAB Semiconductor Foundries AG, \*Gottfried Wilhelm Leibniz Universität Hannover*

The use of a thick Copper layer on top of a AlCu-metallization stack instead of common thick Aluminum triggers a need for a change in the reliability characterization and test strategy. The paper describes the differences for reliability test structure layouts, test methods and reliability assessment strategies. Especially the requirements for a reliability test and assessment strategy for non-passivated Copper will be explained.

## **MR.3 Effect of Passivation Annealing on the Electromigration Properties of Hybrid Bonding Stack**

*J. Jourdon, S. Moreau, D. Bouchu\*, S. Lhostis, N. Bresson\*, D. Guiheux, R. Beneyton, S. Renard and H. Frémont\*\*, STMicroelectronics, \*CEA-Léti, \*\*University of Bordeaux*

EM tests performed on a hybrid bonding stack leads to typical values of Black's parameters for a Cu BEOL. Significant influence of passivation annealing is observed on electromigration lifetime. Chemical analyses evidence the effect annealing atmosphere. A discussion is lead on the chemical species concentration at different locations of the stack and the reduction of the Time to Failure with passivation final annealing.

## **MR.4 Atomically Thin Diffusion Barriers for Ultra-Scaled Cu Interconnects Implemented by 2D Materials**

*C.-L. Lo, K. K. H. Smithe\*, R. Mehta, S. Chugh, E. Pop\* and Z. Chen, Purdue University, \*Stanford University*

Sub-1 nm Cu diffusion barriers are realized by using transferred CVD-grown hexagonal boron nitride and directly deposited molybdenum disulfide, for the first time. Based on time-dependent dielectric breakdown measurements, the diffusion barrier properties of these 2D materials are explored to address the barrier/liner scaling challenge for the ultra-scaled interconnect technology. The predicted lifetime of devices with directly deposited 2D barriers can achieve 3 orders of magnitude improvement compared to control devices.

## ***Photovoltaics***

### **PV.1 Effects of Thermal Stress on Hybrid Perovskite Solar Cells with Different Encapsulation Techniques**

*A. Rizzo, L. Ortolan, S. Murrone, L. Torto, M. Barbato, N. Wrachien, A. Cester, F. Matteocci\* and A. Di Carlo\*, University of Padova, \*University of Rome Tor Vergata*

We subjected to both storage and thermal stress solid state solar cells based on organometal perovskites and using Spiro-OMeTAD as hole transport material. We applied two different sealing techniques to encapsulate devices, in order to study the differences during the experiment. Applying both fast cyclic voltammetry, transient measurement and very slow DC measurements for device characterization, we correlated the results obtained during the 540h experiment to the different degradation dynamics within the cell structure.

### **PV.3 Interlaboratory Comparison of Photovoltaic Performance Measurements Using CIGS Solar Cells**

*G. de Amorim Soares, M. Theelen, D. Roosen, M. Daenen\*, J. Carolus\*, M. Meuris\* A. Masolin\*\*, L. Franssen\*\*, T. Birrenbach\*\*\*, A. Gerber\*\*\*, A. Wrigley\*\*\*, and, TNO Solliance, \*IMO-IMOMECE, \*\*Zuyd Hogeschool, \*\*\*Forschungszentrum Jülich GmbH*

An interlaboratory test was carried out to compare performance measurements between four labs in the Netherlands, Germany and Belgium, as a preliminary step to a stress test comparison. 15 commercial CIGS solar cells were distributed between Labs 2-4 for the performance measurements and the results compared to the initial values obtained by Lab 1. The test showed large differences between the labs for all cell parameters, associated both to equipment and methodology applied.

### ***Product/Memory***

#### **PM.1 Failure Mechanism of E-FUSE for a Production Chip During the ESD Zapping Event**

*H. Linewih, J. H. Lee, T.-H. Chan and S. Marimuthu, GLOBALFOUNDRIES*

On-chip electrical fuse (E-FUSE) with electrostatic discharge (ESD) protection scheme failure during point-to-point ESD stress has been reported and analyzed. ESD current flowing through the bus-line and back-to-back diode induces the potential difference between two ground domains that induces activation of the control circuitry to programming mode thus allowing E-FUSE as part of ESD discharge path.

#### **PM.2 Guidance to Reliability Improvement in CBRAM using Advanced KMC Modelling**

*J. Guy, G. Molas, C. Cagli, M. Bernard, A. Roule, C. Carrabasse, A. Toffoli, F. Clermidy, B. De Salvo and L. Perniola, CEA, LETI, MINATEC Campus*

In this paper, we use Kinetic Monte Carlo (KMC) simulations to investigate CBRAM variability. A full auto-consistent model able to simulate SET, RESET, retention and endurance characteristics is proposed for the 1st time, allowing to describe experimental data obtained on Al<sub>2</sub>O<sub>3</sub>/CuTex based CBRAM.

#### **PM.3 Statistics of Disturb Events in OxRAM Devices – A Phenomenological Model**

*N. Raghavan, Singapore University of Technology and Design (SUTD)*

We present here a fundamental derivation of the disturb voltage / time distribution for OxRAM devices using the percolation cell framework for our model, accounting for the localized electric field distributions and inherent variability in the HRS state vacancy configuration for different switching cycles that play a major role in determining the statistical nature of the read disturb phenomenon. The clustering model is shown to be the best choice for fitting the read disturb data.

#### **PM.4 MTPM Ramped Programming Optimization Methodology**

*Y. M. Randriamihaja, W. McMahon\*, A. Kerber, Z. Chbili, B. Parameshwaran, T. Kirihata, A. Cestero, N. Robson, D. Moy, R. Katz, D. Anand, D. Tomasky, J. Pape and S. Iyer\*\*, Globalfoundries, \*Roivant Sciences, \*\*University of California*

In this paper, we introduce a methodology to optimize Multi-Time Programmable Memory (MTPM) ramped programming to obtain a breakdown free programmed chip, which allows leveraging existing inline device-level Voltage Ramp Stress data to monitor process impact on programmability and BD-risk reduction.

#### **PM.5 Uniform and Concentrated Read Disturb Effects in Mid-1X TLC NAND Flash Memories for Enterprise Solid State Drives**

*C. Zambelli, P. Olivo, L. Crippa\*, A. Marelli\* and R. Micheloni\*, Università degli Studi di Ferrara, \*Microsemi Corp.*

In this work we will show, through an extensive read disturb characterization on mid-1X TLC NAND Flash memories, that different read usage models of NAND Flash blocks (i.e., uniform versus concentrated) in an SSD lead to different constraints and guard band strategies against the disturb. The variability of the disturb entity among different pages and wordlines of a block are presented and related to specific properties as well as the impact on SSD reliability.

#### **PM.6 Investigation of Read Disturb Error in 1Ynm NAND Flash Memories for System Level Solution**

*A. Kobayashi, H. Watanabe, Y. Sakaki, S. Aritome and K. Takeuchi, Chuo University*

Read-disturb characteristics in 1Ynm NAND flash memories have been investigated. The error regularity among word-lines is observed in 1Ynm triple-level cell (TLC) NAND flash. Consequently, unreliable page which exceeds error-correcting code (ECC) capability is occurred. To optimize ECC capability, system level solution with Bose-Chaudhuri-Hocquenghem (BCH) ECC is introduced. By adding parity bit to the unreliable pages for ECC calculation, a correctable bit-error rate (BER) can be increased by 1.3-times.

#### **PM.7 A New Methodology for Assessment of the Susceptibility to Data Retention in Floating Gate Non-Volatile Memories**

*C.-C. Shih, M.-Y. Lee, S.-H. Ku, L.-F. Lee, L.-K. Kuo, W.-J. Tsai, D.J. Lin, W.P. Lu, T.C. Lu, K.C. Chen, Y.H. Chao and C.-Y. Lu, Macronix International Co. Ltd*

We have developed a new methodology with statistical simulation of leakage current resulting in  $V_t$  shift over time of tail bits for assessment of the susceptibility to data retention in floating gate flash memories. The simulator can effectively predict the  $V_t$  distribution of programmed bit for determining the failure rate of flash memories without multi-year bakes and analyzing the leakage mechanism of concern for our process and design.

#### **PM.8 Scaling Perspective and Reliability of Conductive Filament Formation in Ultra-Scaled HfO<sub>2</sub> Resistive Random Access Memory**

*F. M. Puglisi, U. Celano\*, A. Padovani\*\*, W. Vandervorst\*, L. Larcher and P. Pavan, Università di Modena e Reggio Emilia, \*imec, \*\*MDLab s.r.l.*

In this work, we combine device-level measurements, Conductive Atomic-Force Microscopy (C-AFM), and physics-based simulations of HfO<sub>2</sub> RRAM devices to investigate the nature of reported instabilities of the conductive filament at small device dimensions. We provide insights in the scaling perspectives of

RRAMs in terms of operation reliability at ultra-low size ( $< 10 \times 10 \text{ nm}^2$ ). Results show that the formation of the CF in confined volumes and/or at very low CC results in severe ON state reliability issues.

### **PM.9 Optimization of Programming Conditions and Endurance Enhancement of SuperFlash® Memory**

*V. Markov, J.-W. Yoo and A. Kotov, Silicon Storage Technology, Inc., A subsidiary of Microchip Technology, Inc.*

We implemented an effective design-friendly endurance improvement solution on the 3rd-generation SuperFlash®, which provides 1M and higher endurance. It consists in two-step programming with lower coupling gate voltage at the first step. This method also makes possible the increase of programming speed without the endurance penalty, fast programming, lower write energy consumption and higher PD immunity.

### **PM.10 Impact of the Electronic Band Structure on the Reliability of Triple-Layer a-VMCO Devices**

*A. Belmonte, B. Govoreanu, L. Di Piazza, L. Goux and G. S. Kar, imec*

Recently, self-rectifying RRAM cells (SRC) have attracted large interest as suitable candidates for high-density memory applications. We already reported a self-rectifying, self-compliant triple-layer (3L) a-VMCO device, ensuring controlled variability at low-current. However, the physical mechanisms driving the reliability in such devices have not been identified. In this paper, we systematically relate the endurance and retention failures of 3L a-VMCO devices to the electronic band structure of the device, providing guidelines for materials stack optimization.

### **PM.11 SRAM PUF Quality and Reliability Comparison for 28 nm Planar vs. 16 nm FinFET CMOS Processes**

*B. Narasimham, D. Reed, S. Gupta, E. Ogawa, Y. Zhang and J. K. Wang, Broadcom Limited*

SRAM physical unclonable function (PUF) provides a low-cost security and reliability key. In this work the quality and ageing reliability of 28-nm planar and 16-nm FinFET based SRAMs are discussed in detail. Data indicates that 16-nm FinFET process has a better SRAM PUF quality without any design modifications compared to the 28-nm planar process. In addition, the ageing-induced bit instability is shown to be a reasonably small percentage of the overall bit counts.

### **PM.12 Real Usage-based Precise Reliability Test by Extracting Read/Write/Retention-Mixed Real-life Access of NAND Flash Memory from System-level SSD Emulator**

*Y. Yamaga, C. Matsui, Y. Sakaki, A. Kobayashi and K. Takeuchi, Chuo University*

Real usage-based precise reliability test for NAND flash of SSDs are proposed. Conventional simple reliability tests of data-retention and read-disturb cannot reproduce the real-life VTH shift and memory cell errors. The proposed reliability test method precisely reproduces the real memory cell failures by emulating the complicated read, write, and data-retention with SSD emulator. The guidelines of read reference voltage shift are proposed to achieve the highest memory cell reliability for two kinds of real workloads.

### **PM.13 RTN Impact on Data-Retention Failure/Recovery in Scaled (~1Ynm) TLC NAND Flash Memories**

*S. Aritome, T. Takahashi, K. Mizoguchi and K. Takeuchi, Chuo University*

RTN impact on data-retention failure/recovery mechanism has been investigated in 2D TLC NAND flash memories. The data-retention failure is caused by the electron de-trapping from the tunnel oxide in memory cells, which have 5~8 times higher population of large VTH shift by RTN than normal memory cells. In addition, the scaling trend of RTN is evaluated. It is shown that  $dV_{TH\_RTN}$  is increased along with  $1/(WL)^{0.84}$ , which has much severer scaling projection than previous reports.

### ***Reliability Testing***

#### **RT.1 Memory Reliability Estimation Degraded by TDDB Using Circuit-Level Accelerated Life Test**

*D.-H. Kim and L. Milor, Georgia Institute of Technology*

To guarantee reliable operations of circuits and systems, we need to accurately estimate lifetime of a memory system at a circuit or a system level. In this paper, we propose a method that accurately characterizes TDDB wearout mechanisms at use condition using proposed DOEs for system-level accelerated life test.

#### **RT.3 A Thin Film TaN Resistor Reliability Evaluation**

*A. G. Baca, M. E. Overberg, T. R. Fortune and S. L. Wolfley, Sandia National Laboratories*

Bias and thermal stress experiments of thin film TaN resistors were carried out and shown to be consistent with a simple 2-layer degradation model that hypothesizes an interfacial oxidation reaction that consumes conducting TaN. In spite of the observed degradation, the TaN resistors can be consistent with high reliability, since the degradation rate is associated with a high activation energy, 1.55 eV, and can be slow at typical operating junction temperatures.

#### **RT.4 Self Heating Effect on Hot Carrier Degradation Characteristic in High Voltage n-channel LDMOS**

*J. Hao, M. Pelletier, R. Murphy, B. McGowan and T. Kopley, ON Semiconductor*

This paper reports on self heating caused by hot-carrier (HC) stress in packaged thick gate oxide HV LDMOS devices, and how self heating significantly affects HC degradation characteristics. The time delay between the removal of the HC stress and the parameter measurement significantly affected the measured HC  $I_{dlin}/R_{dson}$  degradation with longer delay times resulting in less observed  $I_{dlin}$  degradation. This recovery of degradation observed with longer delay times was mainly due to self heating effects.

## **RT.5 PBTI and PBTS Testing of 0.25 $\mu\text{m}$ pMOSFET Devices for Analog Circuits**

*G. Hall, T. Myers, L. Ou, J. Slezak, A. Litschmann, D. Price, T. Clear and J. Gambino, ON Semiconductor*

PBTI is observed in 0.25  $\mu\text{m}$  pMOS devices in a sense amp after HTOL stress. The HTOL stress causes a negative shift in the threshold voltage of the 5V pMOS devices and a mismatch in the transconductance of the differential pair. PBTI is also observed for 5V pMOS test structures for devices with no protect diodes (antenna ratio = 1000:1). The PBTI is caused by positive charge from interface states and bulk oxide traps.

## ***Soft Error***

### **SE.1 Soft Error Rate Analysis for Incident Angle and N-well Structure Dependencies using Small-sized Alpha Source in 10nm FinFET Technology**

*S. Lee, T. Uemura, U. Monga, J. Choi, G. Kim and S. Pae, Samsung Electronics*

This paper presents the 10-nm FinFET soft error rate with small-sized alpha source. The test result provides the SER difference for particle incidence direction as well as incident angle effect. In supply voltage from 0.5V to 1.4V, the SER of high voltage was mainly reduced in work-line direction and perpendicular incidence angle. N-well geometry and angle of particle incidence affect to the charge collection, and its phenomenon was explained by TCAD simulation.

### **SE.2 A 16 nm FinFET Radiation-hardened Flip-Flop, Bistable Cross-coupled Dual-Modular-Redundancy FF for Terrestrial and Outer-Space Highly-reliable Systems**

*K. Kobayashi, J. Furuta, H. Maruoka, M. Hifumi, S. Kumashiro\*, T. Kato\*\* and S. Kohri\*\*\*, Kyoto Institute of Technology, \*Renesas System Design, \*\*Socionext, \*\*\*STARC*

We fabricated a variation-tolerant and radiation-hardened flip-flop in a 16-nm FinFET technology called Bistable Cross-coupled Dual-Modular-Redundant (BCDMR) FF, which is an improvement on the BCDMR in 65 nm bulk. The 16 nm BCDMR FF exhibits cross sections below  $1\text{e-}11 \text{ cm}^2/\text{FF}$  at 0.8 V by Ag ions, which is 1/100 and 1/4,000 smaller than a conventional D-FF in 16-nm FinFET and 65-nm planer processes respectively. It can be used for highly-reliable and high-performance systems.

### **SE.3 Soft Error Study with DDR4 SDRAMs Using 480 MeV Proton Beam**

*M. Park, S. Jeon, G. Bak, C. Lim, S. Baeg, S. Wen\*, R. Wong\* and N. Yu\*, Hanyang University, \*Cisco Systems Inc.*

Soft error study for DDR4 SDRAMs through proton beam is conducted. Variance in logic upsets were observed in DDR4 SDRAMs. Comparative study against DDR3 SDRAMs show a similar SEU cross-section. Also, result showed that design has a significant factor in both logic upsets occurrence rate as well as its pattern and location. Furthermore, analysis of the logic upsets shows catastrophic failures does not depend only on error size or quantity.

### **SE.4 Single-Event Effects on SSD Controllers**

*B. Bhuvu, S.-J. Wen\*, R. Wong\* and A. Garza\*, Vanderbilt University, \*Cisco Systems, Inc*

With designers employing FF hardening techniques to mitigate soft errors in complex ASICs, low-cost controller ICs have become one of the most vulnerable parts at the system-level. In this paper, SSD controllers are evaluated for neutron soft error performance to estimate their vulnerability. Results show such ubiquitous controller ICs contribute significantly to the system-level SER.



### **SE.5 Influence of Layout Structures to Soft Errors Caused by Higher-energy Particles on 28/65 nm FDSOI Flip-Flops**

*M. Hifumi, H. Maruoka, S. Umehara, K. Yamada, J. Furuta and K. Kobayashi, Kyoto Institute of Technology*

We investigate the influence of layout structures of flip-flops for soft errors. Three flip-flops with different layouts are fabricated in 28/65nm FDSOI. Heavy ion irradiation reveals that the layout with separated diffusion in 28nm have 2x cross section than that with shared diffusion by 40 MeV-cm<sup>2</sup>/mg. Flip-flops in 65nm have almost equivalent cross sections at any energy. It is due to fluctuations of soft error tolerance caused by layout structures of the highly-scaled 28nm.

### **SE.6 On the Efficacy of Using Proton Beams For Estimating Neutron-Induced Soft Error Rates**

*S. Jahinuzzaman, N. Seifert, S. Sekwao and A. Neale, Intel Corporation*

We demonstrate that monoenergetic proton beams can be used to complement neutron-induced soft error rates (SER). This conclusion is supported by proton cross section data collected at various proton facilities on testchips designed and manufactured in planar and FinFET technologies and by Geant4 based LET distribution simulation results.

### **SE.7 A Compact High-Sensitivity 2-Transistor Radiation Sensor Array**

*Q. Tang, S. Kumar, D. E. Fulkerson\* and C. H. Kim, University of Minnesota, \*Independent Consultant*

A compact 2 Transistor (2T) radiation sensor with tunable measurement sensitivity was implemented in a 65nm LP bulk process. Alpha particle testing results show that the proposed sensor array has a 117x higher measurement sensitivity as compared to a 6T SRAM cell. Simulation results show that Qcrit of the proposed 2T sensor cell is 17x-60x smaller than that of an inverter chain and SRAM cell for supply voltages ranging from 0.75V to 1.5V.

## ***System Reliability***

### **SR.1 On the Relationship between Semiconductor Manufacturing Volume, Yield, and Reliability,**

*J. Siddiqui, J. Ortega, B. Albus, Defense Microelectronics Activity*

Suppliers developing semiconductor technologies for consumer electronics have been operating in a high-volume manner for decades. There is a generally accepted link between high volume, high yield, and high reliability. A concerning misconception is that low-volume manufacturers then cannot achieve high reliability. However, many 'high reliability' markets source their parts from low-volume manufacturers. The misconception stated above is explored in terms of economic factors involved, and engineering Practices used to deliver reliable parts.

## *Transistors/Beyond CMOS*

### **XT.1 Resolution of Disputes Concerning the Physical Mechanism and DC/AC Stress/Recovery Modeling of Negative Bias Temperature Instability (NBTI) in p-MOSFETs**

*N. Parihar, U. Sharma, S. Mukhopadhyay, N. Goel, A. Chaudhary, R. Rao and S. Mahapatra, Indian Institute of Technology Bombay*

NBTI is believed due to interface trap generation and hole trapping in gate insulator traps. However, the extraction methods and relative dominance of the above two, their time constants of during stress and recovery and the associated T activation, and whether interface traps recovers or remains permanent after stress, are widely debated. The resolution of such disputes is necessary to develop reliable NBTI model for DC and AC NBTI stress in p-MOSFETs.

### **XT.2 New Insights into 10nm FinFET BTI and its Variation with Considering the Local Layout Effects**

*C. Liu, M. Jin, T. Uemura, J. Kim, J. Kim, U. Jung, H. C. Sagong, G. Kim, J. Park, S. Shin and S. Pae, Samsung Electronics*

BTI variation of 10nm FinFET is experimentally studied taking into account of the local layout effects. Although Fin shape is further optimized in 10nm compared with 14nm, the BTI and its variation show no obvious differences from the previous node. In addition, the impacts of local layout effects on reliability are also investigated. Through Si data, BTI and its variation are not very sensitive to the layout effects.

### **XT.3 Analyzing the Effects of Boron Transient Enhanced Diffusion on Low Frequency Noise in NMOSFETs**

*S. Fujii, T. Yagi, S. Hamada, I. Maru, Y. Okuaki, T. Chiaki, A. Okamoto, T. Sakamoto and T. Miyazaki, Asahi Kasei Microsystems Corporation*

The effects of boron transient enhanced diffusion on low frequency noise (LFN) were investigated. For the first time, it was experimentally found that higher boron concentration regions induced by TED, especially around source regions, degrade LFN. Reverse short channel effect characteristics, boron re-distribution induced by interstitial Si atoms, and LFN of asymmetric deep S/D devices were investigated. Mechanism of LFN was discussed using asymmetric channel devices.

### **XT.4 Combined Variability/Sensitivity Analysis in III-V and Silicon FETs for Future Technological Nodes**

*N. Zagni, F. M. Puglisi, G. Verzellesi and P. Pavan, Università di Modena e Reggio Emilia*

In this paper we present a study on sensitivity and variability in Si and InGaAs nMOSFETs in both Dual Gate Ultra-Thin Body and FinFET structures. The proposed combined variability/sensitivity analysis highlights how the two different material systems are characterized by different dominant variability sources. Results show that the alleged superior electrical performances of InGaAs devices at reduced device sizes might be counterbalanced by increased variability and sensitivity to process variations.

### **XT.5 Interaction Between Hot Carrier Aging and PBTI in nMOSFETs: Characterization, Modelling and Lifetime Prediction**

*M. Duan, J. Zhang, J. C. Zhang, W. Zhang, Z. Ji, B. Benbakhti, X. Zheng\*\*, Y. Hao\*\*, D. Vigar\*\*\*, F. Adamu-Lema\*, V. Chandra^, R. Aitken^, B. Kaczer^^, G. Groeseneken^^ and A. Asenov\*, Liverpool John Moores University, \*University of Glasgow, \*\*XiDian University, \*\*\*Qualcomm, UK, ^ARM Research, ^^imec*

The key advance of this work is to develop a methodology that enables accurate modelling of Interacted HCA-PBTI Degradation (IHPD) through understanding the charging/discharging and generation kinetics of different types of defects. A comprehensive model has been developed by taking into account the HCA-PBTI interaction. Good agreement has been achieved between test data and simulation results for different channel lengths devices. Not considering the HCA/PBTI interaction can underestimate device lifetime by over one decade.

#### **XT.6 Investigation of Hot Carrier Degradation in Bulk FinFETs**

*E.-A. Chung, K.-J. Nam, T. Nakanishi, S. Park, H. Yang, T. Kauerauf, G. Jiao, H. Kim, H. Lee, S. Pae, D.-W. Kim and K. H. Hwang, Samsung Electronics*

A physical mechanism for HCI induced trap generation and degradation in bulk FinFETs is investigated and verified with both experiment and simulation. HCI degradation is mainly caused by interface states generated by DAHC injection. HCI characteristics in I/O FinFETs is severely degraded with respect to planar FETs because enhanced capability of the gate to control the channel potential profiles increases the intensity of the lateral E-field in comparison with those of planar devices.

#### **XT.7 New Insights on Strained SiGe Channels pFET NBTI Reliability**

*C. Ndiaye, A. Bravaix\*, M. Arabi, R. Berthelon, V. Huard, X. Federspiel, C. Diouf, F. Andrieu\*\*, S. Ortholland, M. Rafik, and F. Cacho, STMicroelectronics, \*ISEN REER-IM2NP, UMR CNRS, \*\*CEA-LETI*

In this paper, we analyse the impact of the variation of LOD found in pMOSFET transistors on 14nm UTBB FDSOI CMOS technology. Experiments show that changing SA has an impact on threshold Voltage ( $V_{th}$ ), on NBTI reliability and on Ring Oscillator (RO) Frequency Drift. We also study the impact of SiGe and gate Stack changing on NBTI.

#### **XT.8 BTI Reliability of InGaAs nMOS Gate-stack: On the Impact of Shallow and Deep Defect Bands on the Operating Voltage Range of III-V Technology**

*V. Putcha, J. Franco\*, A. Vais, S. Sioncke\*, B. Kaczer\*, Q. Xie\*\*, P. Calka\*\*, F. Tang\*\*, X. Jiang\*\*, M. Givens\*\*, N. Collaert\*, D. Linten\* and G. Groeseneken, KU Leuven, \*imec, \*\*ASM*

We show that reliability of InGaAs MOS devices depends not only on density of shallow defect states, but also on density of deep defect states. Hence, it is necessary to characterize both shallow and deep defect densities, to determine the maximum underdrive and overdrive voltages of III-V devices. A gate-stack comprising of a new ASM interface layer (ASM-IL), a LaSiO<sub>x</sub> interlayer and high-k dielectric is shown to achieve the required reliability targets for III-V technology.

#### **XT.9 Relaxation of Time-dependent NBTI Variability and Separation from RTN**

*P. Weckx, B. Kaczer, C. Chen\*, P. Raghavan, D. Linten and A. Mocuta, imec, \*Intel Corp.*

In this paper it is shown that the  $\Delta V_{TH}$  is Exponential-Poisson distributed, independent on the relaxation time. Furthermore, by separating the RTN induced variance from the NBTI relaxation, the true average impact per defect  $\eta$  can be extracted. It is shown not to be correlated to the stress nor relaxation time with no difference with respect to permanent or recoverable degradation.

### **XT.10 The Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on Single Oxide Defects**

*B. Ullmann, M. Jech, S. Tyaginov, M. Waltl, Y. Illarionov, A. Grill, K. Puschkarsky\*, H. Reisinger\* and T. Grasser, TU Wien, \*Infineon*

Here we summarize the results of the first study of mixed NBTI and hot carrier (HC) stress at the single oxide defect level in nano-scale SiON pMOSFETs. We found that less defects contribute to a threshold voltage shift during recovery than would be expected from a simple electrostatic model. We show that this behavior can be consistently explained by non-equilibrium processes induced by the large drain voltage such as impact ionization.

### **XT.11 Efficient Physical Defect Model Applied to PBTI in High-k Stacks**

*G. Rzepa, J. Franco\*, A. Subirats\*, M. Jech, A. Chasin\*, A. Grill, M. Waltl, T. Knobloch, B. Stampfer, T. Chiarella\*, N. Horiguchi\*, L.-A. Ragnarsson\*, D. Linten\*, T. Grasser and B. Kaczer\*, TU Wien, \*imec*

Recent advances in physical defect modeling are difficult to employ because these models require time-consuming TCAD simulations and have numerous physical model parameters. Here we present and verify an efficient BTI model which captures the essence of full physical models while reducing the complexity down to six physical parameters. With this model we investigate the effect of an anneal on a high-k stack and simulate realistic life times.

## ***Wide Band-Gap***

### **WB.1 End User Reliability Assessment of 1.2 - 1.7 kV Commercial SiC MOSFET Power Modules**

*C. Ionita and M. Nawaz, ABB Corporate Research*

This paper presents the reliability assessment of commercial SiC MOSFET power modules with voltage ratings of 1.2-1.7 kV and current rating from 120-800 A. Following JEDEC standards, the reliability assessment is carried out with High Temperature reverse bias test (HTRB), High Temperature gate bias test (HTGB), High humidity, High Temperature, High reverse bias test (H3TRB) and Thermal cycling (TC) tests. Variations in electrical device parameters such as leakage current, threshold voltage, on-resistance has been recorded.

### **WB.2 Influence of the Built-in Electric Field Induced by Low Power Fluorine Plasma Implantation on the Reliability of AlGaIn-GaN HEMTs**

*L. Yang, B. Hou, M. Mi, J. Zhu, M. Zhang, Q. Zhu, Y. L. He, L. Chen, X. W. Zhou, X. H. Ma and Y. Hao, Xidian University*

This paper presents a novel degradation mechanism for the low power fluorine ions implanted ion into traditional T-gate AlGaIn/GaN HEMT. The migration phenomenon of fluorine ions and built-in electric field induced by drift fluorine ion are validated by the electron redistribution and breakdown voltage enhancement after off-state stress.

### **WB.3 A Novel Test Methodology for $R_{ON}$ and $V_{TH}$ Monitoring in GaN HEMTs During Switch-mode Operation**

*F. Iucolano, A. Parisi, S. Reina, G. Meneghesso\*, G. Verzellesi\*\* and A. Chini\*\*, STMicroelectronics, \*University of Padova, \*\*University of Modena and Reggio Emilia*

One of the critical issues of AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructures is the Ron increment due to high drain-source voltages application. Therefore, it is often necessary to evaluate RON and VTH variation by emulating the final operating scenario. Standard measurement equipment does not allow to perform it. Aim of this paper is to present a novel testing methodology which allows the simultaneous monitoring of device RON and VTH during switch-mode operation starting from the very first switching cycles.

#### **WB.4 Temperature-Dependent Threshold Stability of COTS SiC MOSFETs During Gate Switching**

*D. Habersat, R. Green and A. Lelis, U.S. Army Research Laboratory*

We used fast I-V methods to characterize the threshold voltage of commercial-off-the-shelf SiC DMOSFETs during high temperature gate switching. Although the devices were all stable at room temperature, threshold voltage degradation was observed in under 100 hours of stress beginning at 150 °C and near or within datasheet specifications for biasing. This effect has an activation energy of ~1.2 eV and is not observable when using standard parameter analyzer equipment for measurement.

#### **WB.5 Trap Assisted Avalanche Instabilities and Safe Operating Area Concerns in AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs**

*B. Shankar, A. Soni, M. Singh, R. Soman, H. Chandrasekar, N. Mohan, N. Mohta, N. Ramesh, S. Prabhu, A. Kulkarni, D. Nath, R. Muralidharan, K.N. Bhat, S. Raghavan, N. Bhat and M. Shrivastava, Indian Institute of Science*

This work reports very first systematic study on physics of avalanche instability and SOA concerns in AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT using sub-us pulse characterization, post stress degradation analysis, well calibrated TCAD simulations and failure analysis by SEM and TEM. Electrical and thermal effects on SOA boundary and avalanche instability are investigated. Trap assisted cumulative degradation is found as root cause of avalanche. Post failure SEM/TEM analysis reveal distinct failure modes in presence and absence of carrier trapping.

**Thursday, April 6, 2017**

#### ***Session 5A - Product/Memory***

Session Chairs: *Alessandro Spinelli, Politecnico di Milano, Brian Pedersen, Intel*

Thursday, April 6

Regency Main

8:00 a.m. - Session Introduction

8:05 a.m.

#### **5A.1 Impact of Processing and Stack Optimization on the Reliability of Perpendicular STT-MRAM**

*S. Van Beek\*, K. Martens\*, P. Roussel, S. Couet, L. Souriau, J. Swerts, W. Kim, S. Rao, S. Mertens, T. Lin, D. Crotti, R. Degraeve, E. Bury, D. Linten, G. Kar and G. Groeseneken\*, imec, \*KU Leuven*

Ultra-thin MgO and >1MAcm<sup>-2</sup> write currents for STT-MRAM, result in an endurance bottle neck due to oxide breakdown. We do an in-depth analysis of the impact of processing on barrier breakdown, including etch techniques, post etch treatments and variations of the MRAM stack. We find that variability in breakdown characteristics can be significantly reduced using an optimized etch. Secondly we propose an oxygen scavenging model to explain the different reliability behavior for various stack configurations.

8:30 a.m.

### **5A.2 Impact of Discrete Trapping in High Pressure Deuterium Annealed and Doped Poly-Si Channel 3D NAND Macaroni**

*A. Subirats, A. Arreghini, L. Breuil, R. Degraeve, G. Van den bosch, D. Linten and A. Furnemont, imec*

In this paper, the influence of different processes on electron trapping in vertical 3D NAND macaroni has been investigated. Through slow Id-Vg measurements and RTN analysis, it is shown that doping can cure poly-Si channel defects while deuterium (D2) anneal can passivate both traps present in the channel and in the ONO gate stack. Finally, it is shown that the D2 anneal curing can also help to improve retention after cycling.

8:55 a.m.

### **5A.3 Statistical Study of RRAM MLC SET Variability Induced by Filament Morphology**

*C.-W. Hsu, X. Zheng, Y. Wu, T.-H. Hou\* and H.-S. Philip Wong, Stanford University, \*National Chiao Tung University*

This paper establishes the correlation between RRAM multilevel-cell (MLC) stochastic SET variability and random telegraph noise (RTN). We show that a smaller diameter (dD) of locally connecting/rupturing CF and larger distance of gap (dG) between CF and electrode demonstrate both steeper Weibull slope  $\beta$  with a relaxed SET-disturb margin by 0.4 V and 36 $\times$  improvement in RTN robustness. Results from the Kinetic Monte Carlo (KMC) modeling also support these findings.

9:20 a.m.

### **5A.4 Error Recovery of Low Resistance State in 40nm TaOx-based ReRAM**

*K. Maeda, S. Fukuyama, R. Yasuhara\*, S. Mishima\* and K. Takeuchi, Chuo University, \*Panasonic Semiconductor Solutions Co., Ltd.*

Error recovery effect of low resistance state (LRS) has been observed in set/reset cycling endurance in TaOx based ReRAM cell. LRS error cells are recovered to normal LRS by the relaxation time between set and reset. This phenomenon can be explained by oxygen vacancy diffusion to reconstruct the conductive filament in error cells. Based on this phenomenon, the bit error rate in ReRAM is reduced by the dispersed data writing with the wear-leveling.

9:45 a.m.

### **5A.5 Kinetic Defect Distribution Approach for Modeling the Transient, Endurance and Retention of a-VMCO RRAM**

*S. Subhechha\*, R. Degraeve, P. Roussel, L. Goux, S. Clima, K. De Meyer\*, J. Van Houdt\* and G. S. Kar, imec \*also with KU Leuven*

Amorphous-Si Vacancy Modulated Conductive Oxide resistive switching devices achieve switching by electrical modulation of the defect distribution. We propose a quantitative model in which defects are accelerated by lowering of the potential barrier under electric field. Using this model, we explain the observed characteristics of gradual switching, reset during set bias, and also its endurance and retention characteristics.

## *Session 5B - Dielectrics-Gate, MOL, BEOL*

Session Chairs: *Yung-Huei Lee, TSMC, Nagarajan Raghavan, Singapore University of Technology*

Thursday, April 6

Regency I

8:00 a.m. - Session Introduction

8:05 a.m.

### **5B.1 A Percolation Defect Nucleation And Growth Model For Assessment Of The Impact Of Low-K Dielectric Breakdown On Circuit Reliability**

*S.-C. Lee and A. S. Oates, TSMC*

We postulate that BEOL dielectric breakdown can be described in terms of the nucleation and subsequent growth of percolation defects. We develop a semi-empirical model to describe the statistics of post-breakdown current growth. The model predicts a Poisson area dependence of the time to hard breakdown, and percentile dependent area dependence of the growth time. These findings provide a new methodology for prediction of TDDB reliability that exhibits substantial increases compared to industry standard methods.

8:30 a.m.

### **5B.2 Generalized Model of Dielectric Breakdown for Thick and Thin SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> Films Combining Percolation Model and Constant-ΔE Model**

*K. Okada, K. Narita, M. Kamei, S. Ohno, Y. Ito and S. Suzuki, TowerJazz Panasonic Semiconductor Co., Ltd.*

To realize accurate prediction of TDDB lifetimes, appropriate extraction of various parameters is indispensable. While TDDB statistics such as the thickness dependence of Weibull slope have been successfully described by the percolation model, it has been revealed that the percolation model is not capable to explain the TDDB statistics of thick SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> films and, therefore, we propose a generalized model by combining with the constant ΔE model we proposed for Si<sub>3</sub>N<sub>4</sub> MIM structures.

8:55 a.m.

### **5B.3 Low-k Dielectric Degradation Study with Polarity Switch**

*Q. Yuan, A. Patel, L. H. Brown, Y. Zhao, Z. T. Mai, and S. English, Samsung Austin Semiconductor*

This paper studies bipolar TDDB degradation process for Back-End-of-Line (BEOL) Cu interconnect with low-k material. For Cu comb structure, we find the change of leakage current  $\Delta I/I$  per polarity switch and its changing rate has correlation with bipolar TDDB lifetime. Using  $\Delta I/I$  as an indicator we studied low-k material degradation and recovery under thermal stress. We built a simple model to simulate leakage current with major characteristics reproduced.

9:20 a.m.

### **5B.4 A Process-Variation-Cognizant Efficient MOL and BEOL TDDB Evaluation Method**

*A. Kim, R. Bolam, B. Li, B. Linder and E. Wu, IBM Systems*

We present efficient TDDB evaluation methods to optimize test time and improve accuracy of TDDB model parameter estimation. The proposed methods include dual ramped voltage stress (DRVS) for estimation of voltage acceleration, V<sub>bd</sub>-based sample grouping to minimize skewness of thickness variation effect among test groups of samples, and TDDB stress sequencing to optimize test duration.

945 a.m.

**5B.5 A New and Holistic Modelling Approach for Impact of Line-Edge Roughness on Dielectric Reliability (Late News)**

*E. Wu, R. Muralidhar, T. Shaw, G. Bonilla, J. Stathis, B. Li and A. Kim, IBM Research Division*

The realistic simulation of line-edge roughness profiles is carried out based on power-spectrum density (PSD) function including the effects of both roughness and correlation-length. In contrast to the previous reports, we show that LER roughness causes a significant reduction not only in T63 but also in Weibull slopes. Our LER simulation has achieved quantitative agreement with experimental statistical data, revealing an in-depth knowledge for the separate roles of LER profiles and field-enhancement effect.

***Session 5C - Failure Analysis/Process Integration***

Session Chairs: *Bryan Tracy, EAG Laboratories, Kevin Johnson, Intel*

Thursday, April 6

Regency IV

8:00 a.m. - Session Introduction

8:05 a.m.

**5C.1 Failure Analysis of Aluminum Electrolytic Capacitors based on Electrical and Physicochemical Characterizations**

*C. Lachkar, M. Kadi, J.-P. Kouadio, M. Presle\*, S. El Yousfi\*, J.-F. Goupy\*\* and P. Eudeline\*\*, Normandie University, \*Laboratoire national de métrologie et d'essais, \*\*Thales Air Systems*

Over the past few years, manufacturers had tried to improve reliability of aluminum electrolytic capacitors by changing the shape of packaging and the composition of electrolyte. In this paper, we have used capacitors having wholly sealed cubic case and containing gamma-butyrolactone-based solution. These components are tested under thermal and electrical stress to determine failure mechanisms. The proposed analysis method is based on the combination of electrical measurement results and physicochemical characterizations of capacitors.

8:30 a.m.

**5C.2 One-to-One Correspondence between nm-resolution Channel Crystallinity and Electrical Property of Poly-Si TFT Revealed by NBD Two-Dimensional Imaging (Late News)**

*T. Asano, R. Takaishi, M. Oda, K. Sakuma, M. Saitoh and H. Tanaka, Toshiba Corp.*

We successfully established the direct correspondence between the channel crystallinity and electrical property in one and the same poly-Si nanowire TFTs. Our new techniques realize site-specific preparation of NBD specimen of the electrically evaluated TFT and a large map of diffraction patterns to reveal the crystallinity of whole channel area. We found that drain current in individual TFTs is determined by whether the electrons can travel without passing through the grain boundaries inside the channel.

8:55 a.m.

**5C.3 High Resolution Thermal Imaging of Pre-Breakdown in Power AlGaIn/GaN MOSHEMTs**

*K. Maize, H. Zhou, P. D. Ye and A. Shakouri, Purdue University*

Thermoreflectance imaging microscopy is demonstrated for thermal failure analysis of AlGaIn/GaN MOSHEMTs stressed to catastrophic breakdown. High resolution thermal images reveal direct correlation between localized hot spots/cold spots during bias stress cycle and material breakdown at the fail site.



Quantitative, rapid in situ inspection of thermal distribution in relation to catastrophic device breakdown assists study of underlying thermal mechanisms and facilitates simulation, design and process optimization.

9:20 a.m.

#### **5C.4 BTI Reliability and Time-Dependent Variability of Stacked Gate-All-Around Si Nanowire Transistors**

*A. Chasin, J. Franco, B. Kaczer, G. Rzepa\*, V. Putcha, P. Weckx, R. Ritzenthaler, H. Mertens, N. Horiguchi and D. Linten, imec, \*TU Wien*

We report experimental results of the N/PBTI reliability of stacked silicon nanowire MOSFETs. We benchmark the lifetime of these devices against FinFETs with similar gate-stack. We do not only compare the average degradation, but also the time-dependent variability. Finally, we forecast the impact of the nanowire diameter on the reliability using TCAD simulations. Both the experimental results and the simulations indicate that BTI reliability is not negatively impacted down to a nanowire diameter of 6nm.

9:45 a.m.

#### **5C.5 Ultrafast PBTI Characterization on Si-free Gate Last Ge nFETs with Stable and Ultrathin Al<sub>2</sub>O<sub>3</sub> IL**

*C. Joishi, S. Kothari, S. Ghosh, S. Mukhopadhyay, S. Mahapatra and S. Lodha, Indian Institute of Technology Bombay*

This work for the first time reports PBTI on Ge nFETs with stable, ultrathin Al<sub>2</sub>O<sub>3</sub> IL using ultrafast characterization techniques. The fabricated gate stack is Si cap-free making it attractive for scaled FinFETs. Microseconds delay time employed captures all possible signatures of trap generation and trapping. Trap generation behavior studied using a detrapping technique shows trap-generation at IL/high-k interface. PBTI is shown to improve with decrease in high-k thickness, increase in IL thickness and FGA.

### ***Session 6A - Transistors/Beyond CMOS***

Session Chairs: *Souvik Mahapatra, India Institute of Technology, Steve Ramey, Intel*

Thursday, April 6

Regency Main

10:40 a.m. - Session Introduction

10:45 a.m.

#### **6A.1 Boundaries, interfaces, point defects, and strain as impediments to thermal transport in nanostructures (Invited)**

*S. Mei, C. J. Foss\*, L. N. Maurer, O. Jonasson, Z. Aksamija\*, and I. Knezevic, University of Wisconsin, \*University of Massachusetts*

The ability to grow heterostructures with atomically smooth interfaces brings great flexibility to the design and development of modern electronic and optoelectronic devices. While nearly perfect from an electronic standpoint, these interfaces are exceedingly disruptive to thermal transport and are a major contributor to anisotropic heat conduction and localized heating. Doping, alloying, and strain — all commonly employed when tailoring electronic properties of heterostructures — are also highly detrimental to the transport of phonons, the dominant carriers of heat in semiconductors. From the theoretical standpoint of phonon dynamics in disordered systems, I will present the state-of-the-art in how we understand nanoscale thermal transport and its profound sensitivity to any deviation from single-crystallinity. On several examples of semiconductor nanostructures and devices, such as nanowires, superlattices, and quantum cascade lasers, I

will discuss the energy exchange between the electronic and lattice systems, with focus on the development of thermal stress and ultimate mechanical failure in the structures that have high thermal mismatch between different parts and are exposed to long-term nonequilibrium electronic transport conditions

11:10 a.m.

**6A.2 Implications of Gate-Sided Hydrogen Release for Post-Stress Degradation Build-Up after BTI Stress**, *T. Grasser, M. Watzl, K. Puschkarsky\*, B. Stampfer, G. Rzepa, G. Pobegen\*\*, H. Reisinger\*, H. Arimura\*\*\* and B. Kaczer\*\*\*, TU Wien, \*Infineon, \*\*KAI, \*\*\*imec*

Degradation after BTI stress typically recovers monotonically. We will show here that - consistent with a gate-sided hydrogen release mechanism - additional degradation can apparently build-up during recovery also after BTI stress, which can under certain circumstances even exceed the post-stress degradation levels. This additional degradation may invalidate existing lifetime extrapolation methods. Our results demonstrate that although post-stress degradation build-up is only visible under certain conditions, it is an essential feature of BTI.

11:35 a.m.

**6A.3 Predictive TCAD for NBTI Stress-Recovery for Different Device Architectures and Channel Materials**,

*S. Mishra, H. Y. Wong\*, N. Parihar, V. Moroz\* and S. Mahapatra, IIT Bombay, \*Synopsys Inc.*

TCAD implementation of stress and recovery for different architectures. Calibrated TCAD with planar SiGe MOSFETs used for simulation of SiGe FinFETs and GAA NWFETs. It is shown(1) reduced fin and nanowire width increases degradation magnitude and reduces Voltage Acceleration Factor(2) FinFETs and GAA NWFETs having SiGe channel offer superior reliability as compared to Si channel(3) GAA NWFETs are less reliable than planar and bulk FinFETs(4) Constant VG and Vov stress are discussed for fair benchmarking.

1:50 p.m.

**6A.4 Self-Heating in Advanced CMOS Technologies (Invited)**

*C. Prasad, S. Ramey, L. Jiang, Intel*

On advanced technology nodes, increases in power density as well as non-planar architectures cause local self-heating due to active power dissipation, which can affect device performance and reliability in various ways. This paper presents an overview of the research on self-heating in transistors and discusses modulators, measurement schemes, modeling methods, and impacts on performance and reliability. As we continue to scale dimensions and power densities, the significance of self-heating effects will continue to grow, and a robust frame-work to assess it and deal with its impacts are essential.

2:15 p.m.

**6A.5 Anomalous Bias Temperature Instability on Accumulation-Mode Ge and III-V MOSFETs**

*M. Si, H. Wu, S. Shin, W. Luo, N. Conrad, J. Zhang, W. Wu, M. A. Alam and P. Ye, Purdue University*

In this work, we report the observation of anomalous bias temperature instability (ABTI) phenomenon on InGaAs accumulation-mode nMOSFET with Al<sub>2</sub>O<sub>3</sub> as dielectric and Ge accumulation-mode pMOSFET with Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub> gate stack. A simple model is proposed to explain the experimental observation. It is understood that trap neutral level (TNL) alignment and donor-like and acceptor-like traps generation and recovery are the major origins of the ABTI behavior.

2:40 p.m.

## **6A.6 Reliability of Black Phosphorus Field-Effect Transistors with Respect to Bias-Temperature and Hot-Carrier Stress**

*Y. Illarionov, M. Waltl, M. Jech, J.-S. Kim\*, D. Akinwande\* and T. Grasser, TU Wien, \*The University of Texas at Austin*

We perform a detailed study of BTI and HCD on highly-stable black phosphorus FETs and capture the correlation between these phenomena. We show that the hot-carrier stress applied in conjunction with BTI leads neither to a considerably stronger degradation nor to dramatically different recovery dynamics, in contrast to graphene and Silicon FETs. This allows us to conclude that the BP/SiO<sub>2</sub> system presents a significant step forward in terms of reliability improvement of next-generation 2D devices.

## ***Session 6B - Metallization Reliability***

Session Chairs: *Ki-Don Lee, Samsung, Gavin Hall, ON Semi*

Thursday, April 6

Regency I

*10:40 a.m.* - Session Introduction

*10:45 a.m.*

### **6B.1 Characterization of Self-Heating and Current-Carrying Capacity of Intercalation Doped Graphene-Nanoribbon Interconnects**

*J. Jiang, J. Kang and K. Banerjee, Univ. of California, Santa Barbara*

*11:10 a.m.*

### **6B.2 Reliability Study on Cobalt and Ruthenium as Alternative Metals for Advanced Interconnects**

*O. V. Pedreira, K. Croes, A. Leśniewska, C. Wu, M. H. Van Der Veen, J. de Messemaeker, K. Vandersmissen, N. Jourdain, L. G. Wen, C. Adelman, B. Briggs, V. V. Gonzalez, J. Bömmels and Z. Tókei, imec*

Intrinsic TDDDB studies of systems with Co and Ru fill show that Co needs a barrier to prevent drift into SiO<sub>2</sub>, contrarily to Ru for which no drift into any studied dielectric was observed. Intrinsic EM results show a slightly better performance of Co filled lines compared to Cu fill lines, where a much better performance of Ru filled lines is observed. Via failures on Ru schemes show ~5x higher lifetime compared with Cu schemes

*11:35 a.m.*

### **6B.3 Direct Correlation between Low Frequency Noise Measurements and Electromigration Lifetimes**

*S. Beyne, K. Croes\*, I. De Wolf and Z. Tokei\*, KU Leuven, \*imec*

In this paper we show that using low frequency (LF) noise measurements as a new, faster technique for electromigration (EM) characterization is not limited to providing EM activation energies (which we demonstrated in the previous IRPS) but can also explain and even predict EM lifetimes of interconnect lines. Therefore, two models are proposed to predict void nucleation and growth times for individual interconnects subjected to electromigration, based on the results of non-destructive LF noise measurements.

1:50 p.m.

**6B.4 Interactions and Self-Healing of Cu Vias During Stress Migration Tests and Implications for Burn-In and Design Rule Formulations**

*G. Hall and D. Allman, ON Semiconductor*

During High Temperature Storage (HTS), previously failed vias due to open failures from voids appear to self-heal and never fail again. The propensity for self-healing and subsequent “immortality” depends on the fact that the stress induced voids interact in a manner similar to growing and ripening nuclei in a late-stage phase transition. We demonstrate the implications for reliability and engineering design through scaling relationships well as indicate directions for further experimental and theoretical study

2:15 p.m.

**6B.5 Theoretical Predictions of EM-induced Degradation in Test-structures and On-Chip Power Grids with Analytical and Numerical Analysis (Invited)**

*V. Sukharev, A. Kteyan, J.-H. Choy, S. Chatterjee\* and F. Najm\*, Mentor Graphics, \*University of Toronto*

The talk discusses the state of the art physics-based analytical modeling and numerical analysis techniques developed for the prediction and description of EM induced conductance degradation of individual interconnect metal lines and on-chip power grids. Mechanical stress evolution caused by an electric current driven redistribution of vacancies and plating atoms, which populates the metal grain boundaries (GB) and interfaces, initiates the growth of preexisted crystal imperfections such as micro caverns and interfacial/inter-granular delamination. It is described as a major cause of the failure. A role in the failure development played by the texture, interfacial and GB atomic diffusions and their variation is covered. A close relation between the interfacial-adhesion energy and so-called “critical stress” is clarified. A physics-based statistical formulation of EM phenomenon is discussed.

Different kind of analytical/numerical techniques employed for analysis of EM degradation in different cases characterized by the scales varying from the size of an individual line to the multibillion segment power grids are discussed. Conditions for employment of 1D EM approximation (Korhonen’s equation) are validated by direct comparison with results of 3D FEA simulations. Implementation of the novel compact model- and FDA-based approaches for analyzing EM-induced IR-drop degradation in power nets is demonstrated.

2:40 p.m.

**6B.6 Effect of Joule Heating on Electromigration in Dual-Damascene Copper Low-k Interconnects**

*K.-D. Lee, J. Kim\*, T.-Y. Jeong\*, Y. Zhao, Q. Yuan, A. Patel, Z. Mai, L. Brown, S. English and D. Sawyer, Samsung Austin Semiconductor, \*Samsung Electronics*

The effect of Joule heating (JH) on electromigration (EM) was investigated using copper low-k interconnects, and confirmed Black’s EM model works at a very wide range of temperatures (185°C ~ 365°C) and currents (0.03mA ~ 3.5mA) after JH corrections: EM  $E_a = 1.05\text{eV}$  and  $n = 1.4$ . TEM PFA confirms a similar EM voiding mechanism regardless of JH. For JH-assisted EM, lifetime distributions are increased, possibly because there are more factors of JH impacting EM.

3:05 p.m.

**6B.7 BEOL Reliability Enhancement by Applying New Capping Materials**

*H. Chang and C. T. Chang, National Chiao Tung University*

We surmise that the thinner the ESL thickness combined with post SiH<sub>4</sub> treatment of the CoWP cap the higher the TDDB performance. In this study, Low-resistivity ALD-W exhibited medium EM enhancement with reduced variability. Post-treatment of CoWP with SiH<sub>4</sub> improved EM and TDDB performance

(relative to the control) by 10 and 100 fold, respectively. The significantly increased EM and improved TDDB performance indicate the feasibility of using cap materials.

### ***Session 6C - System Reliability***

Session Chairs: *Ajay Kamath, Google, Guneet Sethi, Amazon Lab126*

Thursday, April 6

Regency IV

10:40 a.m. - Session Introduction

10:45 a.m.

#### **6C.1 NASA Past, Present, and Future: the Use of COTS in Space (Invited)**

*K. LaBel and S. Guertin, NASA*

NASA has a long history of using commercial grade electronics in space. In this submission, we will provide a brief history of NASA's trends and approaches to commercial grade electronics focusing on processing and memory systems. This will include providing summary information on the space hazards to electronics as well as NASA mission trade space. We will also discuss developing recommendations for risk management approaches to Electronic and Electromechanical (EEE) parts usage in space. Two examples will be provided focusing on a near-earth Polar-orbiting spacecraft as well as a mission to Mars. The final portion will discuss emerging trends impacting usage.

11:10 a.m.

#### **6C.2 Telemetry for Reliability**

*R. Kwasnick, P. Karayacoubian, P. Polasam, A. Wang, A. Biswas, J. Tayeb and R. Mattani, Intel Corporation*

Knowledge of customer usage of IC products is an important part of establishing accurate use conditions inputs for product reliability modeling. We present a multi-stage framework for achieving this: derive telemetry metrics; develop telemetry software; acquire users; manage and store telemetry data; perform data analytics and visualization; decide use conditions. We discuss each stage's objectives and requirements, and provide information relevant to successful implementation. Server telemetry examples are presented to elucidate the framework and its role in evaluating product reliability.

11:35 a.m.

#### **6C.3 Hybrid Physics Based-Data Driven Approach for Reliability Allocation of Early Stage Products**

*A.Kale, A. Marathe, J. Meng, A. Kamath, M. Rogge and A.-R. Bahmandar, Google Inc*

This paper presents a novel approach for reliability demonstration of a product operating in dynamic time varying environment. The device is subjected to mechanical loads, humidity and temperature swings whose magnitude is uncertain a-priori. The goal of this paper is to extract mission profile from field data and develop a framework to iteratively update reliability test plan based on failure mechanisms observed in field and lab tests.

1:50 p.m.

#### **6C.4 Today's Functional Electronic Clones (Invited)**

*T. Sharpe, SMT Corp.*

The entire electronics industry is now facing a much more insidious counterfeit threat than at any time in the past. The existence of cloned electronic components bearing the markings of major component manufacturers in today's global supply chains has been clearly established within SMT's labs over the past 5 years. The most worrisome aspect of these "made from scratch" fakes is their ability to easily pass current inspection processes AND electrical testing to the manufacturers data sheet. Advanced counterfeiters today are performing both "reverse-engineering" and "functional-die-emulation" manufacturing processes. This presentation will share several actual examples of this most concerning counterfeiter capability and some of the cutting-edge inspection and test processes utilized by SMT as an obsolescence component supplier and testing lab to mitigate this new and quickly growing threat from making it to our OEM, EMS & CM customers.

2:15 p.m.

### **6C.5 Failure Models for Low-Voltage Ceramic Capacitors with Defects**

*A. Teverovsky, ASRC Space and Defense*

A physical model that relates the presence of defects to reduction of breakdown voltages and decreasing times to failure (TTF) of ceramic capacitors has been suggested. The model allows estimations of TTF distributions based on reliability voltage acceleration factors and distributions of breakdown voltages. The effect of the defect size has been analyzed using a thermal runaway model of failures. The applicability of HALT to predict failures at normal operation conditions has been analyzed.

2:40 p.m.

### **6C.6 Fast Cell Level Characterization and Reliability Evaluation for Advanced Flexible Mobile Display**

*H. Kim, J. Lee, K. Lee\*, J. Bang, B. Lee, Y. Hwang, D.-S. Shin\* and J. Park, Samsung Display Corporation, \*Hanyang University*

For advanced flexible mobile display, elucidation of charge transfer mechanism of an emissive layer (EL) in organic light-emitting diode (OLED) is crucial to assure performance and reliability. Two different ELs were exposed to accelerated stress test in a cell level, then characterized by the luminescence-current-voltage (L-I-V), capacitance-voltage (C-V), and impedance measurements. With a specific test structure, we were able to accelerate EL degradation, providing fast turnaround results compared to conventional aging test in a module level.

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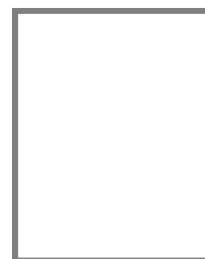


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*Intel*



Vice-Chair, Sudarshan Rangaraj  
*Amazon Lab 126*

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Georgios Konstadinidis, *Oracle*  
Haldun Kufluoglu, *Qualcomm*  
Pong-Fei Lu, *IBM*  
Jim Tschanz, *Intel*

## Dielectrics - Gate, MOL, BEOL



Co-Chair, Yung-Hei Lee  
*TSMC*

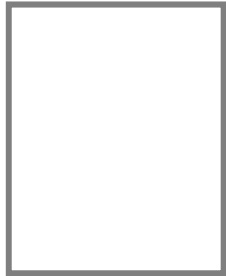


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*Singapore University of Technology and Design*

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Lin Cong, *NVidia*  
Martin Gall, *Fraunhofer Institute*  
Ru Huang, *Peking University*  
Andrew Kim, *IBM*  
James Lloyd, *SUNY Poly*  
Maria Luque, *Samsung*  
Enrique Miranda, *UAB*

Paul Nicollian, *Semiconductor Reliability*  
Chetan Prasad, *Intel*  
Francesco Maria Puglisi, *Unimore*  
Naohito Suzumura, *Renesas*  
Christophe Vallee, *CEA*  
Dmitry Veksler, *NIST*  
Bonnie Weir, *Avago*  
Shnji Yokogawa, *UEC*

## ESD/Latchup



Chair, Farzan Farbiz  
*Texas Instruments*



Vice-Chair, Michael Khazhinsky  
*Silicon Labs*

Zhong Chen, *University of Arkansas*  
Kai Esmark, *Infineon*  
Nathan Jack, *Intel*  
Mujahid Muhammad, *GlobalFoundries*  
Nicolas Nolhier, *Laboratoire d'analyse et  
d'architecture des systèmes*

Guido Notermans, *NXP Semiconductors*  
Moto Okushima, *Renesas*  
Alan Righter, *Analog Devices*  
Mayank Shrivastava, *Indian Institute of Science*

### Failure Analysis/Process Integration



Chair, Bryan Tracy  
*EAG Laboratories*

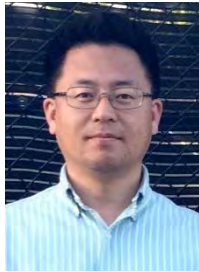


Vice-Chair, Kevin Johnson  
*Intel*

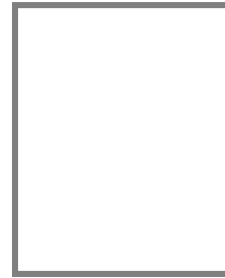
Eckhard Langer, *GlobalFoundries*  
Jane Li, *NVidia*

Ken Rodbell, *IBM*

### Metallization Reliability



Chair, Ki-Don Lee  
*Samsung*



Vice-Chair, Gavin Hall  
*ON Semi*

Ming-Hsien Lin, *TSMC*  
Linjun Cao, *GlobalFoundries*  
Howard Gan, *SMIC*  
Baozhen Li, *IBM*

Cher Ming Tan, *Chang Gung University, Taiwan*  
Zsolt Tokei, *IMEC*  
Feng Xia, *Intel*

## Photovoltaics



Chair, Andrea Cester  
*University of Padova*



Vice-Chair, Michael Daenen  
*Hasselt University*

Fernando A. Castro, *National Physical Laboratory*

Cosimo Gerardi, *Enel Green Power S.p.A., 3Sun*

Suren Gevorgyan, *DTU Energy, Technical University of Denmark*

Salvatore Lombardo, *CNR-IMM, Italy*

Eszter Voroshazi, *IMEC*

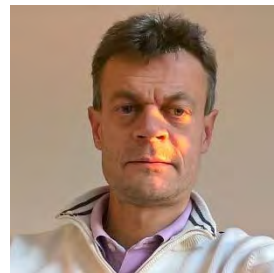
Martin Weis, *Institute of Electronics and Photonics, Slovak University of Technology*

Karl-Anders Weiß, *Fraunhofer-Institut für Solare Energiesysteme ISE*

## Product/Memory



Chair, Brian Pedersen  
*Intel*



Vice-Chair, Alessandro Spinelli  
*Politecnico di Milano*

John Agness, *Rohm Semiconductor*

Jae-Gyung Ahn, *Xilinx*

Marc Aoulaiche, *Micron*

Pierre Chor-Fung Chia, *Cisco*

Eric (Ming-Hsiu) Lee, *Macronix*

Luca Perniola, *CEA*

Nagarajan Raghavan, *Singapore University of Technology and Design*

Richard Rao, *Microsemi*

Aamer Shaukat, *Freescale*

Peng Su, *Juniper*

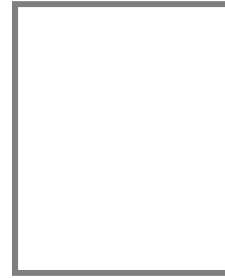
Jan Van Houdt, *IMEC*

Cristian Zambelli, *University of Ferrara*

## Reliability Testing



Chair, Hosain Farr  
*QualiTau*



Vice-Chair, Kevin Manning  
*Analog Devices*

Pascal Salome, *Serma Technologies*  
Stéphane Moreau, *CEA-Leti*

Fiorella Pozzobon, *STMicroelectronics*  
Dirk Rudolph, *GlobalFoundries*

## Soft Error



Chair, Balaji Narasimham  
*Broadcom*



Vice-Chair, Marta Bagatin  
*University of Padova*

Thiago Assis, *RCI*  
Bharat Bhuvu, *Vanderbilt University*  
Indranil Chaterjee, *Airbus*  
Mike Dion, *Rockwell Collins*  
Adrian Evans, *iRoC*  
Yi-Pin Fanga, *TSMC*  
Christopher Frost, *Rutherford Appleton  
Laboratory*  
Gilles Gasiot, *STMicroelectronics*

Shah Jahinuzzaman, *Intel*  
Michael King, *Sandia Labs*  
Nihaar Mahatme, *NXP Semiconductors*  
Phil Oldiges, *IBM*  
Heather Quinn, *LANL*  
Taiki Uemura, *Samsung*  
Shi-Jie Wen, *Cisco*

## System Reliability



Chair, Ajay Kamath  
*Google*



Vice-Chair, Guneet Sethi  
*Amazon Lab 126*

Randy Crutchfield, *Medtronic*  
Aamir Kazi, *Dell*  
Amit Marathe, *Google*

Raj Pendse, *Qualcomm*  
Shalabh Tandon, *Intel*

## Transistors/Beyond CMOS



Chair, Souvik Mahapatra  
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Stanislav Tyaginov, *TU Wien*  
Dhanoop Varghese, *Texas Instruments*  
Miaomiao Wang, *IBM*

## Wide Band Gap



Chair, Denis Marcon  
*IMEC*



Vice-Chair, Sandeep Bahl  
*Texas Instruments*

Andrew Barnes, *ESA*

Partha Sarathi Chakraborty, *NXP Semiconductors*

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Peter Moens, *ON Semiconductor*

David Sheridan, *Alpha and Omega  
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