IRPS

International Reliability Physics Symposium

2018 IRPS Conference Proceedings

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Intro

For 59 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world.

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Shah Jahinuzzaman - Intel

Michael King - Sandia Labs
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Haibin Wang - Hohai U.
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Amit Marathe - Google
Jay Sarkar - Western Digital
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Jason Campbell - NIST
Eun-Ae Chung - Samsung
Suman Datta Norte Dame U.
Xavier Federspiel - STMicroelectronics
Jacopo Franco - IMEC
Luca Larcher - U. of Modena
Chris Liu - Huawei
Souvik Mahapatra - India Institute of Technology
Montserrat Nafria - U. Autonoma de Barcelona
Jurriaan Schmitz - U. of Twente
Ricki Southwick - IBM
Purushothaman Srinivasan - Globalfoundries
Bonnie Weir - Broadcom
Chad Young - UT

Wide Band Gap

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Abhishek Banerjee - ON
Alberto Castellazzi - U. Nottingham
Ferdinando Iucolano - ST
Tsunenobu Kimoto - Kyoto U.
Martin Kuball - U. Bristol
Aivars Lelis - US Army Research Labs
Peter Losee - GE
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Kurt Smith - Transphorm
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Kenichiro Tanaka - Panasonic
Deepak Veereddy - Infineon
Shireen Warnock - MIT Lincoln labs

Topics of Interest

SPECIAL FOCUS TOPICS

IRPS18 is soliciting increased participation in the following areas: reliability of wide bandgap semiconductor power devices, circuit aging, consumer electronics, reliability of 2D NAND flash replacement technologies, 2.5D & 3D packaging

Circuits, Products, and Systems

Circuit Reliability – Includes digital, mixed-signal, power and RF applications; design for reliability, variability-aware design

Circuit Aging Simulation – Includes compact modeling; statistical methods

Product IC Reliability – Includes burn-in; defect detection; on-chip sensors; modeling

Consumer Electronics Reliability – Includes smart phones; wearable devices; tablets; healthcare devices

Electronic System Reliability – Includes automotive, space, communications, medical, energy, and photovoltaic applications; screening techniques; reliability-aware circuit design and optimization, system monitoring; failure root cause determination; modeling methodologies, product qualification vs reliability

Soft Errors – Includes neutron and alpha particle SER; multi-bit SER/SEU; mitigation techniques; simulation

ESD and Latchup – Includes component and system-level ESD design; modeling and simulation

3D Assembly – Includes multichip modules; 3D integration with TSV; thermomechanical stress; wafer thinning effects

Packaging – Includes chip-package interaction; fatigue; power dissipation issues, Reliability 2.5D and 3D IC packaging and interconnects

Reliability Testing – Includes reliability equipment, tools, and test methods

Materials, Processing, and Devices

Transistors – Includes hot carrier phenomena; BTI; RTN; advanced transistor scaling, variability, Ge and III-V channels

Gate Dielectrics – Includes TDDB modeling; reliability of novel gate dielectrics; modeling of progressive breakdown; gate dielectric reliability for III-V FETs

Beyond CMOS Devices – Includes reliability of tunnel FETs, transistors with 2D semiconductors (graphene, MoS2), Ferroelectric FETs, and spintronics

Wide bandgap semiconductors (WBG) – Includes reliability of WBG-based power devices (GaN, SiC, Ga2O3)

Compound and Optoelectronic devices – includes reliability of III-V-based devices, optoelectronics devices, silicon photonics, far infrared detectors

Back-End Reliability – Includes Electromigration; Joule heating; stress migration; low-k dielectric breakdown; middle-of-the-line reliability, MIM/MOM capacitors

Process Integration – Includes new process-related reliability issues; foundry reliability challenges

Failure Analysis – Includes evidence of new failure mechanisms; advances in failure analysis techniques

Memory Reliability – Includes DRAM and NVM, novel memory devices: 3D Flash and ReRAM

Photovoltaics – Includes reliability of solar cell devices in silicon, CdTe, CIGS, organics, multi-junctions, etc.

MEMS – Includes reliability of sensors and actuators; reliability testing; analysis & modeling, BioMEMS

Program

NOTE – For full Program, including Abstracts and Speaker information, view Appendix

VIDEOS – https://www.youtube.com/user/IEEEIRPS/videos

Keynote & Invited Speakers

First Keynote: The Road to Resilient Computing in Autonomous Driving is Paved with Redundancy

Dr. Nirmal Saxena, NVIDIA

8:45 AM, Tuesday March 13th

Abstract: Deep neural networks use the computational power of massively parallel processors in applications such as autonomous driving. Autonomous driving demands resiliency (as in safety and reliability) and trillions of operations per second of computing performance to process sensor data with extreme accuracy. This keynote examines various approaches to achieve resiliency in autonomous cars and makes the case for design diversity based redundancy.

Biography: Nirmal R. Saxena is currently a distinguished engineer at NVIDIA and is responsible for HPC and automotive resilient computing. From 2011 through 2015, Nirmal was associated with Inphi Corp as CTO for Storage & Computing and with Samsung Electronics as Sr. Director working on fault-tolerant DRAM memory and storage array architectures. During 2006 through 2011, Nirmal held roles as a Principal Architect, Chief Server Hardware Architect & VP at NVIDIA. From 1991 through 2009, he was also associated with Stanford University's Center for Reliable Computing and EE Department as Associate Director and Consulting Professor respectively. During his association with Stanford University, he taught courses in Logic Design, Computer Architecture, Fault-Tolerant Computing, supervised six PhD students and was co-investigator with Professor Edward J. McCluskey on DARPA's ROAR (Reliability Obtained through Adaptive Reconfiguration) project. Nirmal held senior technical and management positions at Alliance Semiconductors, Chip Engines, Tiara Networks, Silicon Graphics, HaL Computers, and Hewlett Packard.

Nirmal received his Ph.D. EE degree (1991) from Stanford University. He is a Fellow of the IEEE (2002) and was cited for his contributions to reliable computing.

Second Keynote: Reliable Ultra-Low Energy Security Circuit Primitives for IoT Edge Systems

Dr. Sanu Mathew, Intel Corporation

9:30 AM, Tuesday March 13th

Abstract: Low-area energy-efficient security primitives are key building blocks for enabling end-to-end content protection, user authentication and data security in IoT platforms. This talk describes the design of reliable security circuit primitives with optimal arithmetic for seamless integration into area/battery constrained IoT systems: 1) A 2040-gate AES accelerator achieving 289Gbps/W efficiency in 22nm CMOS, 2) Hardened hybrid Physically Unclonable Function (PUF) circuit to generate a 100% stable encryption key. The talk will also discuss design issues related to side-channel leakage of embedded secret keys, and how they may be addressed during design of encryption circuits. We will also discuss the effect of aging on PUF circuits and techniques to handle aging issues over the lifetime of the die.

Biography: Sanu Mathew is a Senior Principal Engineer with the Circuits Research Labs at Intel Corporation, Hillsboro, Oregon, where he leads research and development of energy-efficient hardware accelerators for encryption and security. Sanu obtained his Ph.D. degree in Electrical and Computer Engineering from State University of New York at Buffalo in 1999. He holds 41 issued patents, with another 63 patents pending and has published over 77 conference/journal papers. He has been with Intel for the past 18 years. Sanu is a Fellow of the IEEE.

Invited Speakers

- The effects of radiation on the terrestrial operation of SiC MOSFETs – Bakin Akturk, CoolCAD
- Reliability Challenges in 2.5D Packaging and Embedded Silicon Bridge – Emre Armagan, Intel
- Protective nanometer films for reliable Cu-Cu connections – Berthold, Fraunhofer
- p-GaN gate reliability including short-circuit robustness – Alberto Castelazzi, Univ. Nottingham
- SiC Power MOSFET Gate Oxide Breakdown Reliability – Current Status – Charles Cheung, NIST
- Reliable and damage-resistant optics and detectors for x-ray free-electron lasers – Stefan Hau-Riege, Lawrence National Laboratory
- Next Generation Interconnect Reliability Metallization Integration – Chao-Kun Hu, IBM
- Reliability of MEMS sensors through self calibration – Amit Lal, Cornell University
- Reliability Studies of SiC Vertical Power MOSFETs – Daniel J. Lichtenwalner, Wolfspeed
- Exascale Fault Tolerance Challenge and Approaches – Cameron McNairy, Intel
- Reliability issues of GaN commercialization – Umesh Mishra, UC Santa Barbara
- Cathodoluminescence spectroscopy for failure analysis and process development of GaN-based microelectronic devices – Christian Monachon, Attolight
- COTS Electronics Reliability for Space Applications – Jonny Pellish, NASA
- System level ESD and its implications on I/O protection – David Pommerenke, Missouri University of Science and Technology
- Reliability Challenges on 2.5D/3D chip integration – an Overview – C S Premachandran, Global Foundries
- Airplane Systems Design for Reliability & Quality – Anapathur Ramesh, Boeing
- Recent Advances in In-situ and In-field Aging Monitoring and Compensation for Integrated Circuits – Mingoo Seok, Columbia University
- Role of electron and hole trapping in degradation and breakdown of oxide films – Alex Shluger, University College, London
- Permanent shunting from passing shadows: Reverse-bias damage in thin-film photovoltaic modules – Timothy Silverman, NREL
- Defects Affecting SiC Power Device reliability – Bob Stahlbush, NRL
- The Physics of NBTI: What Do We Really Know? – Jim Stathis, IBM
- Estimating transistor channel temperature using time-resolved and time-integrated NIR photoemission – Franco Stellari, IBM
- Reliability perspective of resistive synaptic devices on the neuromorphic system performance – Shimeng Yu, Arizona State University

Distinguished Lecturer

Real Limits to Nanoelectronics: Interconnects and Contacts

Prof. Krishna Saraswat, Stanford University

1:30 PM, Wednesday March 14th

Abstract: As device scaling continues, parasitic source resistance largely dominated by contact resistance is beginning to limit the device performance. While novel structures and materials have enhanced the transistor performance, the opposite is true for the interconnects that link these transistors. This talk will address effects of scaling on the performance of conventional contacts and interconnects, and explore alternate contact and interconnect schemes

Biography: Prof. Krishna Saraswat is Rickey/Nielsen Professor in the School of Engineering, Professor of Electrical Engineering and by courtesy Professor of Materials Science & Engineering at Stanford University.

He received his B.E. degree in Electronics in 1968 from BITS, Pilani, India, and his M.S. and Ph.D. degrees in Electrical Engineering in 1969 and 1974 respectively from Stanford University, Stanford, CA. During 1969-70, he worked at Texas Instruments. After graduating he joined Stanford University as a Research Associate in 1975 and later became a Professor of Electrical Engineering in 1983. He also has an honorary appointment of an Adjunct Professor at BITS, Pilani, India since January 2004.

His research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III-V devices and interconnects for VLSI and nanoelectronics. Areas of his current interest are: new device structures to continue scaling MOS transistors and memories to nanometer regime, 3-D ICs, optical interconnections and high efficiency and low cost solar cells.

He has supervised more than 85 doctoral students, 30 post doctoral scholars and has authored or co-authored 15 patents and over 790 technical papers. He is a Life Fellow of the IEEE. He received the Thomas Callinan Award from The Electrochemical Society in 2000, the 2004 IEEE Andrew Grove Award, Inventor Recognition Award from MARCO/FCRP in 2007, the Techno-visionary Award from the India Semiconductor Association in 2007, BITS Pilani Distinguished Alumnus Awards in 2012 and the Semiconductor Industry Association Researcher of the Year Award in 2012. He is listed by ISI as one of the Highly Cited Authors in his field.

Tutorials

- Semiconductor Reliability and Product Qualification - Chris Henderson, Semitracks
- Soft Error Fundamentals - Norbert Seifert, Intel
- FEOL Reliability - Barry Linder, IBM
- Introduction to ESD and Latchup Design and Test Methods - Nathan Jack, Intel
- Back-End of Line (BEOL) Reliability - Baozhen Li, IBM
- Testing of Automotive IC's: Introduction and Advances - Davide Appello, STMicroelectronics
- An Overview of Chip to Package Interaction and its Impact on Reliability - Scott Pozder, GLOBALFOUNDRIES
- System Reliability - Amit Marathe and Amit Kale, Google
- Self-Heating in 10nm-class FinFET - Chetan Prasad / Intel
- STT-MRAM: Past History, Current Status and Future Perspectives - Yiming Huai / Avalanche
- Ultra High Voltage LDMOS Device and Technology - Sameer Pendharkar, Texas Instruments
- Advanced BTI - Tibor Grasser, Univ. of TU Wien
- 3D Flash Memories: Overview of Cell Structures, Operations and Reliability - Makoto Fujiwara, Toshiba
- SiC Power MOSFETs: Application Benefits and Technology Validations Needs - Albert Castellazzi, Nottingham University
- Conductive Atomic Force Microscopy and its Use in Nanoelectronic Device Reliability - Mario Lanza, SUDA
- HBM Design, Test & Reliability Challenges for AI Applications - Daeyong Shim, SKHynix
- Validating the Robustness of GaN Power Transistors - Kenichiro Tanaka, Panasonic

Workshops

- 3D Transistor reliability - Hot Carrier - Chetan Prasad (INTEL) / Jacopo Franco (IMEC)
- Providing Enterprise-level System Reliability in the sub-10nm technology era - Ron Newhart (IBM) / Cameron McNairy (Intel)
- Emerging-memory-reliability-challenges and opportunities-in-MRAM, RRAM, 3D XP - Jon Slaughter (IBM) / Jerry Chung Wei Hsu (TSMC)
- Automotive: What are the challenges for new technologies? - Andreas Aal (VW) / Khai Nguyen (NVIDIA) / Shalabh Tandon (Intel)
- Circuit-Reliability-advanced-nodes-concerns and CAD tools flow - Matthew Hogan (Mentor) / Wonjae Kang (Intel) / Hiu Wong (Synopsys)
- GaN reliability for power and RF devices - What are the key issues and how to resolve? - Sandeep Bahl (TI) / Matteo Meneghini (U of Padova)
- Challenges and advances in advance node interconnect reliability - Patrick Justison (Global Foundries) / Rahim Kasim

(Intel)

- 3D Transistor reliability: BTI - Souvik Mahapatra (IIT Bombay) / Chadwin Young (University of Texas at Dallas)
- Storage and Memory - SSD, SD, DIMM: Resiliency in design, system-level considerations and role of usage analytics - Jay Sarkar (Western Digital - HGST) / Haitham Hamed (SK Hynix)
- Synergies between GaN and SiC for reliability development and standardization - Sameh Khalil (Infineon) / Aivars Lelis (U.S. Army Research Laboratory)
- Advanced packaging reliability: 2.5D, 3D and fan-out packaging for system scale - Kangwook Lee (Amkor) / Emre Armagan (Intel)
- Circuit Reliability: In-field healing and repair - serious need or science fiction? - Jim Tschanz (Intel) / Alain Bravaix (ISEN-IM2NP & STM)

Year In Review

GaN and SiC Device Reliability Year-in-Review

GaN – 2017 was an important year for GaN, with product and technology announcements, the establishment of the JEDEC JC70 WBG standards committee, of progress in reliability physics and continued innovation in device design. We will review highlights from papers that are helping develop our reliability physics foundation, papers on device innovation and of a new loss mechanism important for future application usage.

SiC – Enabling progress towards (widespread) commercialisation: SiC advances in material, devices, package and application. In recent years, SiC technology has transitioned from being essentially a research focus area to showing credible promise as a commercial reality. This presentation will review key advances and results presented in 2017, which play a key role in enabling this important transition. The review will cover the whole range of underpinning development areas, from material and process to device design, bespoke package development and applications.

Sandeep Bahl is a distinguished member of technical staff in the High Voltage Power Business Unit of Texas Instruments. He has extensive experience with semiconductor technology development, and has worked on both silicon and compound semiconductor technologies. His present focus is to bring reliable GaN products to market, and to develop the methodology to know that they will be reliable under actual-use conditions. Sandeep helped kickoff the standardization effort of the GaN industry and is presently participating on the JC70 reliability committee as a task-group co-chair. He has served as chair of the Power and Compound Semiconductor subcommittee of the International Electron Devices meeting (IEDM) and of his local San Francisco/Santa Clara valley IEEE chapter. He is presently serving as chair of the IRPS Wide Bandgap Committee. Sandeep graduated with a PhD in Electrical Engineering from the Massachusetts Institute of Technology.

Alberto Castellazzi is an Associate Professor of Power Electronics at the University of Nottingham, UK. He has been active in power electronics R&D for over 15 years, collaborating with some of the main industrial and academic institutes worldwide. His research interests are power devices and the enabling technologies of power electronics. He has published over 180 papers in peer reviewed journals and conference proceedings and is a member of the Technical Program Committee of the IRPS, ISPSD, ESREF, ESTC and IPEC conferences.

MOL and BEOL Dielectrics Reliability Year-in-Review

Studies published in 2017 with respect to MOL and BEOL dielectrics will be reviewed. First, we will focus on studies addressing the understanding of different degradation mechanisms in MOL and BEOL dielectrics, both with respect to leakage current degradation as well as time to breakdown, where intrinsic dielectric breakdown needs to be decoupled from extrinsic like metal contamination, moisture, etc. Second, we will review work where proposals are made to deal with all kinds of variability issues like LER, L2L-variations and V2L-variations. As dielectric breakdown/metal drift is also a heavily studied phenomenon in FEOL and RRAM, a few learnings from these fields which are useful for MOL and BEOL will be cited as well.

Kristof Croes received his BSc in physics at the Catholic University of Louvain (Belgium) in 1993 and his MSc in biostatistics at the Limburgs Universitair Centrum (LUC) in 1994. In 1999, he obtained his PhD, concerning the development of statistical techniques for planning reliability experiments. After that, he joined the reliability business unit of XPEQT, first as the software responsible and then as the manager of the R&D. From 2003 till end 2006, he was product and application manager of the package level reliability products of the Singaporean based company Chiron holdings. Beginning 2007, he went back to research, working as a BEOL reliability engineer in imec. Currently, he is group leader of the Reliability, Electrical test and Modeling group working on test, characterization (electrical, thermal and (thermo)-mechanical) and reliability with main focus on advanced interconnects (2D, 3D, OIO). Kristof was an (invited/tutorial) speaker at several leading egde semi-conductor conferences (IRPS, IITC, IEDM, …). He also (co)-authored >100 papers in the field of reliability.

Circuit Reliability Year-in-Review

This session will focus on the past year of research in the following areas:

1. Unreliable issues at advanced technology nodes: layout, manufacturability, etc.
2. Monitoring and adaptive design techniques at the circuit level;
3. System techniques for energy-efficient reliable design;
4. On-chip machine learning in reliable design

Yu Cao received the B.S. degree in physics from Peking University in 1996. He received the M.A. degree in biophysics and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1999 and 2002, respectively. He is now a Professor of Electrical Engineering at Arizona State University, Tempe, Arizona. He has published numerous articles and two books on nanoscale CMOS design. His research interests include physical design of nanoelectronics, design solutions for reliability, and hardware integration for on-chip learning. He is an IEEE Fellow.

Highlighted Papers

- 2A.1 Transistor - The Physics of NBTI: What Do We Really Know? - Jim Stathis, IBM
- 3A.2 Dielectrics - Time-Dependent Dielectric Breakdown Statistics in SiO2 and HfO2 Dielectrics: Insights from a Multi-scale Modeling Approach - Andrea Padovani and Luca Larcher, MDLSoft, Inc.
- 3C.1 - Managing electrical reliability in consumer systems for improved energy efficiency - Vincent Huard, Souhir Mhira, Antony Barclais, Xavier Lecocq, Fabien Raugi, Marie Cantournet and Alain Bravaix, STMicroelectronics and ISEN-REER
- 3C.6 Systems - Machine Learning Based Dynamic Cause Maps for Condition Monitoring and Life Estimation - Jay Sarkar, Cory Peterson, Amir Sanayei, Western Digital Corporation
- 3D.1 Products - Resilient automotive products through process, temperature and aging compensation schemes - Souhir Mhira, Vincent Huard, Deepak-kumar Arora, Philippe Flatresse and Alain Bravaix, STMicroelectronics, SOITEC and ISEN-REER
- 3E.1 ESD/Latch-Up - Defect-Assisted Safe Operating Area Limits and High Current Failure in Graphene FETs - Nagothu Karmel Kranthi, Abhishek Mishra, Adil Meersha, Harsha Variar and Mayank Shrivastava, Indian Institute of Science
- 4A.1 Dielectrics - Mechanism of Soft and Hard Breakdown in Hexagonal Boron Nitride 2D Dielectrics - Alok Ranjan, Nagarajan Raghavan, Sean O' Shea, Sen Mei, Michel Bosman, Kalya Shubhakar and Kin Leong Pey, Singapore University of Technology and Design and A *STAR
- 4B.1 Wide Band Gap - Degradation of Vertical GaN FETs Under Gate and Drain Stress - Maria Ruzzarin, Matteo Meneghini, Carlo De Santi, Min Sun, Tomas Palacios, Gaudenzio Meneghesso and Enrico Zanoni, University of Padova, Massachusetts Institutute of Technology
- 4C.1 Soft Error - Scaling Trends and Bias Dependence of the Soft Error Rate of 16 nm and 7 nm FinFET SRAMs - Balaji Narasimham, Saket Gupta, Dan Reed, J. K. Wang, Nick Hendrickson and Hasan Taufique, Broadcom
- 4E.2 Wide Band Gap - Lifetime evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under practical switching operations - Ayanori Ikoshi, Masahiro Toki, Hiroto Yamagiwa, Daijiro Arisawa, Masahiro Hikita, Kazuki Suzuki, Manabu Yanagihara, Yasuhiro Uemoto, Kenichiro Tanaka and Tetsuzo Ueda, Automotive and Industrial Systems Company, Panasonic Corporation
- 5B.6 2.5D/ 3D / packaging - Device Reliability for CMOS Image Sensors with Backside TSVs - Jeff Gambino, Hamid Soleimani, Irfan Rahim, Brandon Riebeek, Lieyi Sheng, Hung Truong, Gavin Hall, Rick Jerome and David Price, ON Semiconductor
- 5C.2 Circuits - All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits - Gyusung Park, Bongjin Kim, Minsu Kim, Vijay Reddy and Chris H. Kim, University of Minnesota, Texas Instruments
- 5C.3 Circuits - Design of Aging Aware 5 Gbps LVDS Transmitter for Automotive Applications - Srikanth jagannathan, Kumar Abhishek, Tarun Goyal, Nihaar Mahatme, Gayathri Bhagavatheeswaran and Ender Yilmaz, NXP Semiconductors

- 6B.1 Failure Analysis - Solving Critical Issues in 10nm Technology using Innovative Laser-based Fault Isolation and DFT Diagnosis Techniques - Lesly Zaren Endrinal, Rakesh Kinger, Lavakumar Ranganathan and Amit Sheth, Qualcomm Technologies, Inc.
- 6C.4 Photovoltaics - Mechanical and chemical adhesion at the encapsulant interfaces during the lamination of photo-voltaic modules - Philippe Nivelle, Tom Borgers, Eszter Vöröshazi, Jef Poortmans, Jan D'Haen, Ward De Ceuninck and Michaël Daenen, University Hasselt
- 6D.5 Memory - Reliability Benefits of a Metallic Liner in Confined PCM - Wanki Kim, Yujun Xie, Yerin Kim, Takeshi Masuda, Sangbum Kim, Robert Bruce, Fabio Carta, Gloria Fraczak, Asit Ray, Koukou Suu, Chung Lam, Matt BrightSky, Judy Cha and Yu Zhu, IBM, ULVAC Inc., Yale University
- 6E.1 Testing - Lateral Profiling of HCI Induced Damage in Ultra-Scaled FinFET Devices with Id-Vd Characteristics - Miaomiao Wang, Richard Southwick, James Stathis and Kangguo Cheng, IBM
- 6F.4 Process Integration - Reliability Studies of a 10nm High-performance and Low-power CMOS Technology Featuring 3rd Generation FinFET and 5th Generation HK/MG - Anisur Rahman, Javier Dacuna Santos, Pinakpani Nayak, Gerald S Leatherman and Stephen M Ramey, Intel Corporation

Poster & Focus Sessions

See Appendix – Full Program for Poster & Focus Sessions

Exhibits & Exhibit Events

Exhibits are an integral part of the International Reliability Physics Symposium. Don't miss this opportunity to showcase your company's products and services in our VIRTUAL exposition.

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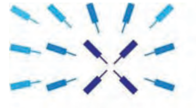

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Appendix - Abstracts, Bios & Technical Program

Session 2A - Transistors: Models and Characterization

Session Chairs: *Steve Ramey, Intel, Tibor Grasser, TUWien*
Tuesday, March 13

10:35 AM - Session Introduction

10:40 AM
2A.1 **The Physics of NBTI: What Do We Really Know? (Invited)**
Jim Stathis, IBM

11:05 AM
2A.2 **Characterization and Physical Modeling of the Temporal Evolution of Near-Interfacial States Resulting from NBTI/PBTI in nMOS/pMOS**
T. Grasser, B. Stampfer, M. Waltl, G. Rzepa, K. Rupp, F. Schanovsky, G. Pobegen**, K. Puschkarsky***, H. Reisinger, B. O'Sullivan#, and B. Kaczer#, TU Wien, *Global TCAD Solutions, **KAI, ***Infineon, #imec*

We use detailed CV/GV measurements to study NBTI/PBTI in nMOS/pMOS transistors. We extract a unique defect band inside the SiO2 insulator, which can describe the build-up of interfacial states over time in all four combinations using our recently suggested hydrogen release model.

11:30 AM
2A.3 **Self-heating-aware CMOS Reliability Characterization Using Degradation Maps**
E. Bury, A. Chasin, B. Kaczer, K. Chuang, J. Franco, M. Simicic, P. Weckx, D. Linten, imec

Based on a large statistical dataset, obtained by measurements on dedicated FET arrays, we i) propose a methodology to identify and de-convolute the active degradation mechanisms in the device in each point of the device operating bias space, ii) apply this methodology to calculate the operating lifetime in the entire bias space and iii) build a self-heating-aware and thus geometry-independent time-to-failure map.

11:55 AM
2A.4 **Cap Layer and Multi-Work-Function Tuning Impact on TDDB / BTI in SOI FinFET Devices**
W. Liu, A. Kerber, F. Guarin and C. Ortolland, GLOBALFOUNDRIES

In this work, we report comprehensive characterization and modeling of time-dependent dielectric breakdown (TDDB) and bias temperature instability (BTI) with multi-work function tuning and a cap layer above high-k in a leading edge SOI FINFET technology.

Session 2B - SiC Reliability and Devices

Session Chairs: *Aivars Lelis, US Army Research Labs, Matteo Meneghini, University of Padova*
Tuesday, March 13

10:35 AM - Session Introduction

10:40 AM
2B.1 **The Effects of Radiation on the Terrestrial Operation of SiC MOSFETs**
B. Akturk, CoolCad

11:05 AM
2B.2 **Reliability Studies of SiC Vertical Power MOSFETs (Invited)**
D. J. Lichtenwalner, Wolfspeed

11:30 AM
2B.3 **SiC Power MOSFET Gate Oxide Breakdown Reliability - Current Status (Invited)**
C. Cheung, NIST

11:55 AM
2B.4 **Defects Affecting SiC Power Device Reliability (Invited)**
R. Stahlbush, NRL

Session 2C - ESD/Latchup

Session Chairs: *Michael Khazhinsky, SI Labs, Gianluca Boselli, Texas Instruments*
Tuesday, March 13

10:35 AM - Session Introduction

10:40 AM
2C.1 **System level ESD and its Implications on I/O Protection (Invited)**
David Pommerenke, Missouri University of Science and Technology

11:05 AM
2C.2 **Stochastic Modeling of Air Electrostatic Discharge Parameters**
Y. Xiu, S. Sagan, A. Battini, X. Ma and E. Rosenbaum, University of Illinois, *Now with IBM*

Stochastic modeling is applied to predict the probability distribution of waveform features during air discharges. The variation in these features, even with an unvarying test condition, contributes to the probabilistic nature of soft failures. An automated air discharge tester enables the collection of sufficient data for statistical modeling.

11:30 AM
2C.3 **An Integral Injector-Victim Current Transfer Model for Latchup Design Rule Optimization**
G.Quax, T. Smedes, NXP Semiconductors

In this work, we present two models which can be used to optimize latchup design rules. The first model describes the injector-victim current transfer during negative current stresses. It includes all relevant geometrical parameters of the injector, victim, and guardring. The second model describes the trigger current of a parasitic pnp bipolar during external latchup. Both models are combined to determine accurate measures for the required well-tap distance in n-wells near injectors.

11:55 AM
2C.4 **Latchup Challenges in FinFET Technologies (Invited)**
Krzysztof Domanski, Intel

Session 3A - FEOL / MOL / BEOL Breakdown

Session Chairs: *Nagarajan Raghavan, Singapore University of Technology and Design, Andrew Kim, IBM*
Tuesday, March 13

10:35 AM - Session Introduction

1:40 PM
3A.1 **Insights into Metal Drift Induced Failure in MOL and BEOL**
C. Wu, O. Varela Pedreira, A. Leśniewska, Y. Li, I. Ciofi, Zs. Tőkei, and K. Croes, imec

Co and Cu drift induced degradation were investigated in SiO2. The failure mechanism of building-up metal in dielectrics is attributed to local metal filament nucleation and growth. Metal filament growth limits the failure times at high fields, while metal filament nucleation is more dominant at low fields. The competition between these two mechanisms and intrinsic dielectric degradation makes the collection of TTF in a wide field and temperature test window inevitable for reliable lifetime predictions.

2:05 PM
3A.2 **Time-Dependent Dielectric Breakdown Statistics in SiO_2 and HfO_2 Dielectrics: Insights from a Multi-scale Modeling Approach**
A. Padovani and L. Larcher, Università di Modena e Reggio Emilia

We use physics-based breakdown simulations to investigate the time dependent dielectric breakdown (TDDB) distributions of SiO2 and HfO2 stacks. We show that the low and thickness independent TDDB Weibull slope measured in HfO2 is originated by their intrinsic defect density and the spatially correlated defect generation process. We also demonstrate that the double slope observed in TDDB distributions of IL-HfO2 dielectric stacks is related to the stochastic nature of the bond-breakage process.

2:30 PM
3A.3 **Elapsed-Time Statistics of Successive Breakdown in the Presence of Variability for Dielectric Breakdown and RRAM applications**
E.Y. Wu, A. Kim, B. Li, and J. H. Stathis, IBM Co.

Due to the competition of multiple spots (filaments) culminating in final hard breakdown in very long wires, it is imperative to develop a comprehensive methodology to correctly incorporate this post-BD margin in technology qualification. In filamentary RRAM operation, elapsed-time statistics affects multi-level switching with multiple filaments and the endurance-related lifetime. In this work, we develop a comprehensive methodology for elapsed time statistics of successive breakdown for dielectric breakdown and RRAM applications.

2:55 PM
3A.4 **Study on Mechanism of Thermal Curing in Ultra-thin Gate Dielectrics**
Y. Mitani, Y. Higashi and Y. Nakasaki, Toshiba Corporation

In order to realize the sustainable devices, thermal curing by self-heating are attracting attention recently. In order to understand the progression of the recovery by heating, in this paper, the thermal curing of the deteriorations at both SiO2 interfaces was investigated in PFETs and NFETs. As results, the damage in PFETs can be recovered even by low temperature curing, but in the case of NFETs, the damage at SiO2/Si interface is hard to be recovered.

3:20 PM
3A.5 **New Methodology for Modelling MOL TDDB**
P. Roussel, A. Chasin, S. Demuynck, N. Horiguchi, D. Linten and A. Mocuta, imec

We report a novel time-dependent dielectric breakdown (TDDB) lifetime model which accounts for the impact of different sources of variability. We prove that the Weibull and Log¬Normal distributions normally used for FEOL and BEOL TDDB lifetime predictions respectively are not adequate for MOL TDDB analysis. Due to the many sources of variability, only a convolution of Weibull and LogNormal distributions can reconcile the intrinsic break¬down mechanism with the extra variability.

Session 3B – FOCUS SESSION: WBG Reliability Synergies and Standardization

Session Chairs: *Sandeep Bahl, Texas Instruments, Matteo Meneghini, University of Padova*
Tuesday, March 13

10:35 AM - Session Introduction

1:40 PM
3B.1 **Brief History of JEDEC Qualification Standards for Silicon Technology and Their Applicability to WBG Semiconductors (Invited)**
J. McPherson, Consultant

2:05 PM
3B.2 **Physical Failure Analysis Methods for Wide Band Gap Semiconductor Devices (Invited)**
A. Graff, Fraunhofer

2:30 PM
3B.3 **Challenges to Realize Highly Reliable SiC Power Device - From the Current Status and Issues of SiC Wafer (Invited)**
J. Senzaki, AIST

2:55 PM
3B.4 **Evaluation Methodology for Current Collapse Phenomena of GaN HEMTs (Invited)**
T. Sugiyama,Toshiba Corp.

3:20 PM
3B.5 **Understanding and Modeling Transient Threshold Instabilities in SiC MOSFETs (Invited)**
H. Reisinger, Infineon

Session 3C - System Reliability

Session Chairs: *Guneet Sethi, Amazon Lab 135, Rob Kwasnick, Intel*
Tuesday, March 13

1:35 PM - Session Introduction

1:40 PM
3C.1 **Managing Electrical Reliability in Consumer Systems for Improved Energy Efficiency**
V. Huard, S. Mhira, A. Barclais, X. Lecocq, F. Raugi, M. Cantournet, and A. Bravaix* STMicroelectronics, *ISEN-REER*

The paper for first time explains how to run realistic electrical reliability qualification trials at system level. Experimental dataset is fully explained by new hierarchical modeling flow. This combined approach enables further tuning of the aging margin to adapt to system usage in the field. This work paves the way to Static Adaptive Voltage Scaling qualification at system level as well as dynamic modulation of aging margin in the field so to improve energy efficiency.

2:05 PM
3C.2 **COTS Electronics Reliability for Space Applications (Invited)**
Jonny Pellish, NASA

2:30 PM
3C.3 **Machine Learning Based Dynamic Cause Maps for Condition Monitoring and Life Estimation**
A. Kale, A. Marathe, A. Kamath, N. Dhar, S. Sellers, Google

Estimating failure modes and life of electronic sub-component in field environment is challenging because of factors such as dynamic field environment, component interactions and errors and variability in operating characteristics. This paper addresses these challenge by developing dynamic cause maps using physics based models, field data and machine learning algorithms.

2:55 PM
3C.4 **Exascale Fault Tolerance Challenge and Approaches (Invited)**
Cameron McNairy, Intel

3:20 PM
3C.5 **Airplane Systems Design for Reliability & Quality (Invited)**
Anapathur Ramesh, Boeing

4:10 PM
3C.6 **Machine-Learned Assessment and Prediction of Robust Solid-State Storage System Reliability Physics**
J. Sarkar, C. Peterson, A. Sanayei, Western Digital Corporation

Reliability physics of complex fault-tolerant memory sub-system of solid-state storage is analyzed leveraging Machine Learning, enabling successful inferential and predictive SSD system reliability assessments in a pro-active manner. While being illustrative of applying Machine Learning to complex system reliability, this paper also discusses the first published method (known to the authors) for assessing individual SSD reliability under throughput acceleration.

4:35 AM

3C.7 **Statistical Modeling and Reliability Prediction for Transient Luminance Degradation of Flexible OLEDs**

H. Kim, H. Shin, J. Park, Y. Choi, J. Park, Technology Reliability, OLED Business Samsung Electronics

We, herein, propose a modified stretched exponential decay (MSED) model in the consideration of transient luminescence decay with respect to intrinsic emissive layer dependent initial luminescence and subsequent degradation over the constant current stress tests. By using the model well fitted to experimental data measured from accelerated stress tests extrapolated to user conditions, we successfully demonstrate that a MSED extracted from statistical modeling enables the precise lifetime prediction with respect to process variation and duty factor in real operation conditions.

5:00 PM

3C.8 **Reliability of MEMS Sensors Through SelfCcalibration (Invited)**

A. Lal, Cornell University

Session 3D - Product IC Reliability

Session Chairs: *Brian Pedersen, Intel, Pierre Chor-Fung Chia, Cisco*
Tuesday, March 13

4:05 PM - Session Introduction

4:10 PM

3D.1 **Resilient Automotive Products Through Process, Temperature, and Aging Compensation Schemes**

S. Mhira, V. Huard, D. Arora, P. Flatresse[*] and A. Bravaix[**], STMicroelectronics, STMicroelectronics, [*]SOITEC, [**]ISEN-REER, IM2NP,

A 32b SoC is designed in 28nm FDSOI to operate for safety-critical applications with joint Process, Temperature and Aging compensation schemes using body-bias. This work demonstrates that up to 74% energy efficiency can be gained by combining Body-Bias Process, Temperature and Aging compensation schemes altogether. This combination of compensation schemes offers the best energy efficiency gain as compared to recent results while guaranteeing high-level of robustness (<1 ppm) and safety for automotive products.

4:35 AM

3D.2 **Fast Chip Aging Prediction by Product-like V_{min} Drift Characterization on Test Structures**

S. E. Liu, G. Y. Chen[*], M. K. Chen[*], D. Yen, W. A. Kuo, C. S. Fu, Y. S. Tsai[*], M. Z. Lin, Y. H. Fang, M. J. Lin, MediaTek Inc., [*] Taiwan Semiconductor Manufacturing Company, Ltd.

We develop a novel product-like characterization methodology to predict chip aging rapidly. To assure reliability, an aging voltage guard band is usually collected by HTOL and implemented to a chip's voltage setting. We proposed a method to mimic product-like characterization on test structures to evaluate Vmin shift. Then, the correlation was established between test structure measurements and chip-level Vmin shift analysis. Therefore, product aging guard-band can be assessed rapidly with process and use condition changes.

5:00 PM
3D.3 **Reliability Characterization of Advanced CMOS Image Sensor (CIS) with 3D Stack and In-pixel DTI**
Y. Ji, J. Kim, J. Kim, M. Lee, J. Noh, T. Jeong, J. Shin, J. Kim,Y. Heo, U. Cho, H. Sagong, J. Park, Y. Choo, G. Do, H. Kang, E. Choi, D. Sun, C. Kang, S. Shin, and S. Pae, Samsung Electronics

Due to the advancement of CMOS image sensors, camera module on the mobile platform has paved way for very high quality photos and video shooting capability. In order to improve picture quality, the CIS technology has been also scaling aggressively to provide more Mega-Pixels but it also must be less susceptible and immune to noise sources, particle, and highly reliable. In this report, we'll discuss the reliability characterization done on the 3D stack sensor.

Session 3E - ESD/Latchup

Session Chairs: *Michael Khazhinsky, SI Labs, Gianluca Boselli, Texas Instruments*
Tuesday, March 13

4:05 PM - Session Introduction

4:10 PM
3E.1 **Defect-Assisted Safe Operating Area Limits and High Current Failure in Graphene FETs**
N. K. Kranthi, A. Mishra, A. Meersha, H. B. Variar and M. Shrivastava, Indian Institute of Science

In this work, a unique measurement setup, involving integration of transmission line pulse tester with Raman spectrometer, is used to investigate the pulsed safe operating area (SOA) boundary of graphene field effect transistors (GFETs). Physical insight into various SOA boundaries is given. Unique defect-assisted degradation in channel and its correlation with the carrier transport and failure is revealed. The SOA and power to fail dependency on carrier concentration and nature of carrier transport is addressed.

4:35 PM
3E.2 **On the ESD Behavior of a-Si:H based Thin-Film Transistors: Physical Insights, Design and Technological Implications**
R. Sinha, P. Bhattacharya, S. Sambandan and M. Shrivastava, Indian Institute of Science

In this work, we present detailed physical and technological insights into the ESD behavior of a-Si:H TFTs. Pre-Breakdown degradation is investigated. Device failure and effect of various parameters on failure is investigated. Effect of Channel dimensions on failure mechanism is thoroughly explored. For the first time, ESD behavior of a-Si:H based Gated diodes and Resistors is reported. Detailed Investigation on Drain Underlap devices and their possible usage as I/O protection device is discussed.

5:00 PM
3E.3 **Contact and Junction Engineering in Bulk FinFET Technology for Improved ESD/Latch-up Performance with Design Trade-offs and Its Implications on Hot Carrier Reliability**
M. Paul, B. Sampath Kumar, H. Gossner and M. Shrivastava, Indian Institute of Science, *Intel Deutschland*

Role of contact and junction engineering to improve ESD and Latch-up robustness while addressing its's implications on hot carrier reliability is discussed. Contact and junction engineering boosts ESD and latch-up robustness, however can adversely affect the HCI reliability, which has been explored in this work

keeping all ESD/Latch-up design parameters in mind. This has allowed us to derive technology guidelines for maximizing overall reliability behavior. Based on these guidelines, a hybrid contact/junction technology is proposed.

Session 4A - FEOL / MOL / BEOL Breakdown

Session Chairs: *Nagarajan Raghavan, Singapore University of Technology and Design, Andrew Kim, IBM*
Wednesday, March 14

8:00 AM - Session Introduction

8:05 AM
4A.1 **Mechanism of Soft and Hard Breakdown in Hexagonal Boron Nitride 2D Dielectrics**
A. Ranjan, N. Raghavan, S.J. O'Shea, S. Mei, M. Bosman*, K. Shubhakar and K.L. Pey,*
*Singapore University of Technology and Design (SUTD), A*STAR*

In this study, we investigate the physical mechanism of soft and hard breakdown using conductive atomic force microscope (CAFM) as a nanoscale spectroscopy tool on blanket h-BN films with tox = 5 nm. The soft breakdown (SBD) regime involves percolation path formation with boron vacancies while the hard breakdown (HBD) regime shows nano-pitting that involves removal of h-BN layers and formation of a metallic contact due to CAFM tip adhesion with the Cu substrate.

8:30 AM
4A.2 **The Physical Mechanism Investigation of Off-State Drain Bias TDDB and its Implication in Advance HK/MG FinFETs**
I. K. Chen, S. C. Chen, S. Mukhopadhyay, D. S. Huang, J. H. Lee, Y. S. Tsai, R. Lu, J. He, Taiwan Semiconductor Manufacturing Company, Ltd.

This work presents a systematic study to understand the off-state drain bias TDDB mechanism, especially for the short channel devices in advanced FinEFT technologies. With additional process optimization such as source/drain proximity push, the sub-threshold leakage current increases, which dominates the off-state TDDB resulting in worse lifetime during practical circuit stress conditions. Impact of body bias on sub-threshold current is also studied with detailed mechanism.

8:55 AM
4A.3 **AC TDDB Extensive Study for an Enlargement of Its Impact and Benefit on Circuit Lifetime Assessment**
M. Rafik A.P. Nguyen, X. Garros*, M. Arabi, X. Federspiel, C. Diouf, ST Microelectronics, *CEA-Leti*

Abstract – With technology scaling and hardening of operating conditions requirements, Time Dependent Dielectric Breakdown (TDDB) remains a major reliability concern. In this paper we show that considering AC rather than DC TDDB would be a promising way to generate margin on lifetime assessment and also to lower the predicted impact of the breakdown on circuit functionality.

9:20 AM
4A.4 **A Systematic Study of Gate Dielectric TDDB in FinFET Technology**
H. Kim, M. Jin, H. Sagong, J. Kim, U. Jung, M. Choi, J. Park, S. Shin and S. Pae, Samsung Electronics

TDDB may have been qualified with only considering operating Ninv and Pinv, but it is necessary to consider all modes including the accumulation mode & off-state mode as well for correctly assessing product level gate oxide dppms and remove conservatism. This along with AC stresses further enables the reliability margin, otherwise, cannot be fully explained generally large gap observed between wafer-level DC based TDDB and product level HTOL, extending technology Vmax headroom without reliability tradeoffs.

9:45 AM
4A.5 **Successive Breakdown Mode of Time-Dependent Dielectric Breakdown for Cu Interconnect and Lifetime Enhancement under Dynamic Bias Stress**
S.K. Lee, K.T. Jang, S.M. Yi and Y.C. Joo, Seoul National University

In gate dielectrics, successive breakdown (BD) was caused by randomly generated bond breakages of the dielectrics. In inter-metal dielectrics, we confirmed that successive BD occurred by the formation of metallic filaments for the first time. The filaments of the successive BD are consisted of Cu atoms mediating bond breakages. Moreover, TDDB lifetime was improved under bipolar stress compared to DC and unipolar stresses due to Cu atom to ion conversion and formation of misaligned filaments.

Session 4B - GaN-based devices reliability

Session Chairs: *Sandeep Bahl, Texas Instruments, Matteo Meneghini, University of Padova*
Wednesday, March 14

8:00 AM - Session Introduction

8:05 AM
4B.1 **Degradation of Vertical GaN FETs Under Gate and Drain Stress**
M. Ruzzarin, M. Meneghini, C. De Santi, M. Sun, T. Palacios*, G. Meneghesso, and E. Zanoni, University of Padova, *Massachusetts Institute of Technology*

We report the analysis of degradation of GaN VFETs under gate and drain stress. High gate bias induces the injection of electrons from the channel towards the gate dielectric (positive Vth shift) and the de-trapping of electrons from the gate insulator to the gate metal (increase in SS). The results of drain step stress reveal that the devices are stable up to VD=280 V, with no significant change in device characteristics.

8:30 AM
4B.2 **A Novel Insight of pBTI Degradation in GaN-on-Si E-mode MOSc-HEMT**
W. Vandendaele, X. Garros, T. Lorin, E. Morvan, A. Torres, R. Escoffier, MA Jaud, M. Plissonnier, F. Gaillard, CEA-Leti

GaN-on-Si HEMT technology is now considered as a serious candidate for medium power applications (650V rated). Vth instabilities are a major concern to increase lifetime of these power transistors. Advanced E-mode MOSc-HEMT (MOS-channel-HEMT) configuration has been recently introduced and studied under harsh gate conditions. In this paper we present for the first time a comparison between AC and DC stress combined with ultra-fast pBTI measurements (< 10µs) on GaN-on-Si E-mode MOSc-HEMTs.

8:55 AM
4B.3 **Reliability Issues of GaN Commercialization (Invited)**
U. Mishra, University of California, Santa Barbara

9:20 AM
4B.4 **Comprehensive Study into Underlying Mechanisms of Anomalous Gate Leakage Degradation in GaN HEMTs**
K. Mukherjee, F. Darracq, A.Curutchet, N. Malbert and N. Labat, IMS Lab, University of Bordeaux

This work investigates fundamental mechanisms governing an atypical parasitic gate leakage characteristic observed in DC forward gate behavior of Schottky gate GAN HEMTs after aging tests. DC measurements are performed to ascertain its long term impact. Detailed TCAD simulation study, for the first time to ourknowledge, reproduces this anomaly through donor state induced surface leakage and trap assisted tunneling across the AlGaN barrier. A proposed hypothesis addresses the unpredictable evolution of this effect.

9:45 AM
4B.5 **On the Origin of the Leakage Current of p-Gate AlGaN/GaN HEMTs**
*A. Stockman, E. Canato[**], M. Meneghini[**], G. Meneghesso[**], E. Zanoni[**], P. Moens and B. Bakeroot**
*ON Semiconductor, *CMST imec / Ghent University, [**]University of Padova*

Temperature dependent DC and double pulse measurements are performed on p-GaN gated AlGaN/GaN enhancement mode power transistors. Devices with improved Schottky metal barrier and p-GaN sidewall passivation are studied. It is shown that both processes reduce the reverse and forward gate leakage current significantly. Under double pulsed testing, a positive threshold shift at high forward gate voltage is induced, which is explained by electron trapping in the barrier.

Session 4C - Soft Error

Session Chairs: *Marta Bagatin, University of Padova, Nihaar Mahatme, NXP Semiconductors*
Wednesday, March 14

8:00 AM - Session Introduction

8:05 AM
4C.1 **Scaling Trends and Bias Dependence of the Soft Error Rate of 16 nm and 7 nm FinFET SRAMs**
B. Narasimham, S. Gupta, D. Reed, J. K. Wang, N. Hendrickson and H. Taufique, Broadcom Ltd.

SRAM SER measurements across technology nodes indicate that while scaling from planar to the first FinFET process provided a large reduction in per-bit SER, the subsequent scaling within FinFET process nodes results in SER reduction comparable to per-bit cell area reduction. Extensive SER measurements over a range of voltages show a strong exponential increase in the SER of FinFET processes with reduction in bias, compared to a linear bias dependence for the planar process.

8:30 AM

4C.2 **Soft Errors in 7nm FinFET SRAMs with Integrated Fan-out Packaging**

Y. Pin Fang and A.S. Oates, Taiwan Semiconductor Manufacturing Company

The susceptibility of alpha induced soft error rate (SER) is dominated by extrinsic alpha sources in packaging such as lead-bearing solder, and bumping materials. Using wafer-level integrated fan-out (InFO) packaging technology, alpha particles emitted from extrinsic packaging materials can be blocked by redistribution layers (RDL) in InFO packaging, leaving the SER susceptibility due to intrinsic alpha sources in Si process. With technology scaling, voltage dependent SER due to intrinsic alpha particles as well as high-energy neutrons is significantly reduced in 7nm SRAM.

8:55 AM

4C.3 **Threshold Ion Parameters of Line-Type Soft-Errors in Biased Thin-BOX SOI SRAMs: Difference between Sensitivities to Terrestrial and Space Radiation**

C. Chung, D. Kobayashi, and K. Hirose, University of Tokyo and Institute of Space and Astronautical Science

Thin-BOX SOI technology is drawing attention for its low soft error sensitivity. Terrestrial radiation tests already demonstrated its further reduction under a back-bias condition. However, recent heavy ion tests with SRAMs exhibited the opposite result, a 100-fold increase accompanying 10-bits-long line-type multi-cell upsets, when they were biased. A metal bridge model suggests that this difference in response to the back-bias conditioning stems from the difference in ion parameters such as range and linear energy transfer.

9:20 AM

4C.4 **Impact of Supply Voltage and Particle LET on the Soft Error Rate of Logic Circuits**

H. Jiang, H. Zhang, R. C. Harrington, J. A. Maharrey, J. S. Kauppila, L. W. Massengill, and B. L. Bhuva, Vanderbilt University

Heavy-ion irradiations of 14/16-nm node bulk FinFET combinational logic circuits under different supply voltage and frequency are investigated. Results indicate that particle LET strongly affects logic soft-error rate (SER). Singe-event transient (SET) experimental data and models for logic SER are used to explain the differences in SER for low-LET particles and high-LET particles.

9:45 AM

4C.5 **Evaluation of the System-Level SER Performance of Gigabit Ethernet Transceiver Devices**

B. Narasimham, T. Wu, J. K. Wang, B. Conway, Broadcom Ltd.

System-level SER measurements were conducted on two Gigabit Ethernet transceiver devices designed in 28-nm CMOS process to evaluate the true impact of soft error upsets. Measurement results are compared with the system SER estimates based on test chip data for memory and flip-flop SER. Results indicate that most SEUs cause packet errors which are recoverable while the SER for more severe link-drop type events is significantly lower than estimates.

Session 4D - FOCUS SESSION: 3D/2.5D/Packaging/MEMS

Session Chairs: *Kothandaraman Chandrasekara, IBM, Sudarshan Rangaraj, Amazon Lab 126*
Wednesday, March 14

10:30 AM - Session Introduction

10:35 AM
4D.1 **High-Density Fan-Out Technology for Advanced SiP and Heterogeneous Integration (Invited)**
K. Lee, Amkor

11:00 AM
4D.2 **Intra- and Inter-Chip Electrical Interconnection Formation by DSA (Invited)**
M. Mariappan, Tohuku University

11:25 AM
4D.3 **Stress Mitigation of 3D-packaging Induced Stresses (Invited)**
C. Croes, imec

11:50 AM
4D.4 **Fine Pitch 3D Interconnections with Hybrid Bonding Technology: Process Robustness and Reliability Results (Invited)**
L. Arnaud, CEA /LETI

12:15 PM
4D.5 **Reliability Concerns for Advanced Packaging (Invited)**
S. Iyer, UCLA

Session 4E - GaN-based devices robustness

Session Chairs: *Sandeep Bahl, Texas Instruments, Matteo Meneghini, University of Padova*
Wednesday, March 14

10:30 AM - Session Introduction

10:35 AM
4E.1 **p-GaN gate reliability including short-circuit robustness (Invited)**
A. Castelazzi, University of Nottigham

11:00 AM
4E.2 **Lifetime evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under practical switching operations**
A. Ikoshi, M. Toki, H. Yamagiwa, D. Arisawa, M. Hikita, K. Suzuki, M. Yanagihara, Y. Uemoto, K. Tanaka and T. Ueda, Panasonic Corporation

The GaN transistors' reliability under continuous switching operation is a very important topic. We perform dynamic high-temperature operating lifetime (D-HTOL) test on Hybrid-Drain-embedded Gate Injection Transistors (HD-GITs) with varying input voltage, switching current and temperature to extract their acceleration factors on the switching lifetime of HD-GITs. The obtained factors are employed to estimate

the lifetime when they are used for a totem-pole power factor correction circuit to conclude that the estimated lifetime is sufficiently long.

11:25 AM
4E.3 **Safe Operating Area (SOA) Reliability of Polarization Super Junction (PSJ) GaN FETs**
B. Shankar, A. Soni, S.D. Gupta, S. Yagi, H. Kawai*, V. Unni**, A.Nakajima**, M. Shrivastava, and E. M. Sankara Narayanan**, Indian Institute of Science, *Powdec K.K., **University of Sheffield*

This work reports Safe Operating Area assessment and degradation physics in Polarization Super Junction (PSJ) based GaN FETs made in Silicon and Sapphire substrates under high voltage and high current injection conditions. Impact of device design parameters on SOA, associated trap assisted device degradation and thermal failure are studied. Correlation between polarization super junction length and failure threshold is discovered, beside power and field dependence of SOA boundary.

11:50 AM
4E.4 **On the Trap Assisted Stress Induced Safe Operating Area Limits of AlGaN/GaN HEMTs**
B. Shankar, A. Soni, S. Dutta Gupta, R. Sengupta, H. Khand, N. Mohan, S. Raghavan and M. Shrivastava, Indian Institute of Science

This experimental study reports a systematic investigation of Safe Operating Area limits in AlGaN/GaN HEMT using sub-us pulse characterization with on-the-fly Raman and CV characterization to probe defect and stress evolution across the device. Influence of a recess depth on SOA boundary is analyzed. Post failure analysis corroborates well with the failure physics unveiled in this work.

12:15 PM
4E.5 **Reliable and Damage-Resistant Optics and Detectors for X-Ray Free-electron Lasers (Invited)**
S. Hau-Riege, Lawrence Livermore National Labs

X-ray free-electron lasers (XFELs) are revolutionizing the physical and life sciences. The sweeping recent success of XFELs can be attributed to their extreme output characteristics: XFELs deliver x-ray photon pulses that are more than nine orders of magnitude brighter than any previous laboratory light source, like synchrotrons. Such extreme radiation poses a particular challenge for the short- and long-term reliability of x-ray optics and detectors which are required to steer, condition, and diagnose individual x-ray pulses. In this presentation, we will discuss how we overcame the challenges of designing damage-resistant optics and detectors without ever having had access to such radiation.

Session 4F - Metallization Reliability

Session Chairs: *Gavin Hall, ON Semi, Zsolt Tokei, IMEC*
Wednesday, March 14

10:30 AM - Session Introduction

10:35 AM
4F.1 **Next Generation Interconnect Reliability Metallization Integration (Invited)**
C-K Hu, IBM

11:00 AM

4F.2 **Electromigration-Induced Backflow Stresses in Cu(Mn) Interconnects Analyzed Based on High Statistical Sampling**

M. Kraatz, C. Sander, A. Clausner, M. Hauschildt, M. Gall, and E. Zschech*
*Fraunhofer Institute for Ceramic Technologies and Systems IKTS, *GLOBALFOUNDRIES LLC & Co. KG,*

Using an alternate Wheatstone bridge setup, sampling over a total of 800 Cu(Mn) interconnects resulted in very smooth resistance vs. time curves during the electromigration process. The test temperature was 350 °C and several current densities ranging from 13 to 17 mA/µm² were applied. Using the averaged resistance curves, linear drift portions were extracted and saturation resistances were extrapolated. The data was further analyzed to obtain a critical Blech product of (510 ± 110) mA/µm.

11:25 AM

4F.3 **Electromigration Characteristics of Power Grid Like Strcutures**

B. Li, A. Ki, P. McLaughlin, B. Linder and C. Christiansen, IBM Systems

Setting appropriate EM limit becomes more and more critical for the leading edge technologies, especially for on-chip power grid. This paper presents EM characteristics of power grid like structures. It demonstrates that the EM reliability is much enhanced from the power grid design environment comparing to the traditional single link EM structures. Discussions are made on the contributing factors to this EM reliability enhancement and how they should be utilized.

11:50 AM

4F.4 **Effect of Metal Line Width on Electromigration of BEOL Cu Interconnects**

S. Choi, C. Christiansen, L. Cao, J. Zhang, R. Filippi Jr., T. Shen, K. B. Yeap, S. Ogden, H. Zhang, B. Fu, P. Justison, GLOBALFOUNDRIES

Electromigration reliability of BEOL Cu interconnects with various metal line widths and via sizes has been studied. EM lifetime improves from minimum width to three times the minimum width, and then saturates. The proposed mechanism for EM lifetime improvement is larger grains in wider lines leading to a reduction in grain boundary diffusion. Cu grain size and Cu drift velocity were correlated to the EM lifetime behavior.

12:15 PM

4F.5 **Protective Nanometer Films for Reliable Cu-Cu Connections (Invited)**

T. Berthold, G. Benstetter, W. Frammelsberger, M. Bogner, R. Rodríguez, M. Nafría, Autonomous University of Barcelona, and Deggendorf Institute of Technology

Session 5A - Transistors: Models and Characterization

Session Chairs: *Steve Ramey, Intel, Tibor Grasser, TUWien*
Wednesday, March 14

2:15 PM - Session Introduction

2:20 PM

5A.1 **Hot Electron and Hot Hole Induced Degradation of SiGe p-FinFETs Studied by Degradation Maps in the Entire Bias Space**

J. Franco, B. Kaczer, A. Chasin, E. Bury, D. Linten, imec

We study hot carrier degradation in $Si_{0.75}Ge_{0.25}$ p-FinFETs by measuring degradation maps in the entire bias space, and compare with Si counterparts. Hot carrier effects are enhanced in SiGe due to larger hole mean free path, and enhanced generation of secondary electrons in the reduced bandgap semiconductor. Both hole and electron injections are observed, partially compensating at some stress biases. Even at logic operating voltages, off-state stress increases the channel leakage due to hot-electron-induced punch-through.

2:45 PM
5A.2 **Role of Electron and Hole Trapping in Degradation and Breakdown of Oxide Films (Invited)**
A. Shluger, University College, London

3:10 PM
5A.3 **Impact of Slow and Fast Oxide Traps on $In_{0.53}Ga_{0.47}$ As Device Operation Studied Using CET aps**
V. Putcha[1,2], J. Franco[2], A. Vais[2], B. Kaczer[2], S. Sioncke[2], D. Linten[2] and G. Groeseneken[1,2]
[1]ESAT department, KU Leuven, [2]IMEC

Kinetics of charge trapping in the InGaAs/Al2O3/HfO2 gate-stack is studied using CET maps. A first defect population with relatively higher capture and emission energy barriers is found to affect the long term reliability of the device, while a second population with relatively smaller capture and emission energy barriers affects the device stability under high frequency operation. We conclude, it is essential to study both defect populations for accurately estimating device lifetime under different operating applications.

3:55 PM
5A.4 **PBTI in InGaAs MOS Capacitors with Al_2O_3/HfO_2/TiN gate stacks: Interface-state Generation**
E. Cartier, M. M. Frank, T. Ando, J. Rozen and V. Narayanan, IBM Research Division, T.J. Watson Research Center

Using devices with well passivated interfaces and reduced electron trapping it is demonstrated that significant interface-state generation occurs during PBTI stress in InGaAs MOS capacitors with Al_2O_3/HfO_2/TiN gate stacks. These observations on capacitors imply that the impact of interface-state generation on mobility and subthreshold degradation need to be monitored in III-V nFET once the electron trapping is brought under control.

4:20 PM
5A.5 **Reliability of Next-Generation Field-Effect Transistors with Transition Metal Dichalcogenides**
Y.Y. Illarionov, A.J. Molina Mendoza, M. Waltl, T. Knobloch, M.M. Furchi, T. Mueller and T. Grasser, TU Wien, *also with Ioffe Physical-Technical Institute*

We perform a detailed reliability study of MoS_2, MoSe2, $MoTe_2$ and WS_2 FETs fabricated on the same SiO2/Si substrate and compare the hysteresis and BTI dynamics for these devices. Our results show that the observed differences can be partially explained by the alignment of the band edges of the 2D semiconductors with the defect bands in SiO2. As such, our study provides strong fundamental insights into the understanding of the reliability of these new technologies.

4:45 PM
5A.6 **Hot Carrier Degradation, TDDB, and 1/f Noise in Poly-Si Tri-gate Nanowire Transistor**
Y. Yoshimura, K. Ota and M. Saitoh, Toshiba Corporation

We study various reliabilities in poly-Si nanowire transistors. Unique hot carrier degradation characteristics are found at low stress gate voltage where degradation was reduced due to suppressed drain avalanche hot carrier by grain boundary. Time dependent dielectric breakdown shows enhanced breakdown probability at nanowire corner similar to SOI nanowire transistors, while breakdown-time distributions is related to randomly oriented grain surface. 1/f noise shows conventional size dependence, while noise amplitude is related to grain size.

Session 5B - 3D/2.5D/Packaging/MEMS

Session Chairs: *Kothandaraman Chandrasekara, IBM, Sudarshan Rangaraj, Amazon Lab 126*
Wednesday, March 14

2:15 PM - Session Introduction

2:20 PM
5B.1 **Analysis of 28 nm SRAM Cell Stability Under Mechanical Load Applied by Nanoindentation**

A. Clausner[1], G. Kurz, M. Otto*, J. Paul*, K.-U. Gierin**, J. Warmuth**, R. Jancke**, A. Aal#, M. Gal, and E. Zschech, Fraunhofer Institute for Ceramic Technologies and Systems IKTS, *GLOBALFOUNDRIES LLC & Co. KG, **Fraunhofer Institute for Integrated Circuits IIS, Engineering of Adaptive Systems EAS, #Volkswagen AG*

28 nm high-k metal gate CMOS SRAM circuits were subjected to controlled mechanical load by nanoindentation. This enables high stress fields in the vicinity of operational SRAM cells. It was found that the loading leads to an increase of the bit cell fail probability around the nanoindentation point. The results attained here provide a quantitative estimate about the influence of package-related stress on performance and reliability of microelectronic products, shedding light on CPI- and CBI-effects.

2:45 PM
5B.2 **Electromigration of multi-solder ball test structures**
C. Hau-Riege, H. Xu, Y.-W. Yau, M. Kakade, J. Li, X. Zhang, H. Farr, Qualcomm Technologies, Inc., *Qualitau,*

This study investigates the electromigration failure characteristics for wafer-level packaging multi-ball structures with different ball numbers, trace sizes, and current distributions. Unlike single-interconnect structures, the resistance and voltage measurements of multi-ball structures show distinct steps and inflections, corresponding to individual ball fails, which was confirmed through failure analysis. Electromigration performance is greatly enhanced by splitting current amongst balls and by increasing the trace size.

3:10 PM
5B.3 **Reliability Challenges in 2.5D Packaging and Embedded Silicon Bridge (Invited)**
E. Armagan, Intel

3:55 PM
5B.4 **Reliability Challenges on 2.5D/3D Chip Integration - an Overview (Invited)**
C. S. Premachandran, GLOBALFOUNDRIES

4:20 PM
5B.5 **TSV Process-Induced MOS Reliability Degradation**
Y. Li, M. Stucchi, S. Van Huylenbroeck, G. Van Der Plas, G. Beyer, E. Beyne, K. Croes, imec

Process-induced MOS capacitor reliability degradation is investigated for both "via-last" and "via-middle" TSV flows. It is shown that during via-last TSV processing, the MOS capacitor reliability is impacted by both the TSV liner open dry etch and the PVD metal barrier deposition. With a protection PN diode, the MOS reliability degradation can however be prevented. In comparison, the reliability degradation in a via-middle flow, caused by the backside TSV dry-etch reveal process, is negligible.

4:45 PM
5B.6 **Device Reliability for CMOS Image Sensors with Backside TSVs**
J.P. Gambino, H. Soleimani, I. Rahim, B. Riebeek, L. Sheng, H. Truong, G. Hall, R. Jerome, D. Price, ON Semiconductor

In this study, device reliability is characterized for two different 0.18 um BSI image sensor technologies. We show that for devices with an SiO2 liner over the gates and with SiN backside dielectrics, the backside processing can degrade device reliability (due to hydrogen depassivation) and that backside process optimization is required to achieve acceptable device reliability (to allow effective repassivation during the final hydrogen anneal).

Session 5C - Circuit Reliability/Aging

Session Chairs: *Chris Kim, University of Minnesota, Georgios Konstadinidis, Google*
Wednesday, March 14

2:15 PM - Session Introduction

2:20 PM
5C.1 **Recent Advances in In-situ and In-field Aging Monitoring and Compensation for Integrated Circuits Monitoring and Compensation for Integrated Circuits (Invited)**
M. Seok, Columbia University

2:45 PM
5C.2 **All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits**
*G. Park, *B. Kim, M. Kim, **V. Reddy, C. H. Kim, University of Minnesota, *Nanyang Technological University, **Texas Instruments*

Using simple on-chip monitoring circuits, we precisely characterized the impact of hot carrier injection and bias temperature instability aging on frequency and phase noise degradation of a 65nm all-digital PLL circuit. Experimental data shows that PLL phase noise degrades with aging even though the output frequency is maintained constant due to the PLL feedback operation. Results show that applying high temperature annealing can recover most of the phase noise degradation.

3:10 PM

5C.3 **Design of Aging Aware 5 Gbps LVDS Transmitter for Automotive Applications**

S. Jagannathan, K. Abhishek, T. Goyal, N. Mahatme, G. Easwaran, NXP Semiconductors

This work investigates the effect of circuit aging on 5 Gbps LVDS Transmitter (TX) used in automotive SoCs. A sensitivity analysis of sub-blocks is discussed. imulations suggest aging induced minor increase in Vth results in system failure. On-chip aging adaptive capability is achieved using jitter and duty-cycle correction circuity to recover critical TX performance within its specifications. Experiments confirms the efficacy of mitigation techniques, with TX restoring its performance to <5% from its pre-aging values.

3:55 PM

5C.4 **Reliability Perspective of Resistive Synaptic Devices on the Neuromorphic System Performance (Invited)**

S. Yu, Arizona State University

4:20 PM

5C.5 **Accelerated BTI Degradation under Stochastic TDDB Effect**

D. Patra, A. Kamal Reza,, M. Katoozi**, E. H. Cannon**, K. Roy*, Y. Cao, Arizona State University, *Purdue University, **Boeing Research & Technology*

The generation of new traps during TDDB may significantly accelerate BTI, since these traps are close to the dielectric-Si interface in scaled technology. This work confirms this correlation with 28nm measurement data. Based on stochastic trapping/detrapping mechanism, new compact BTI models are developed and verified with 14nm FinFET and 28nm data. Moreover, these models are implemented into circuit simulation, illustrating a significant increase in failure rate due to accelerated BTI.

4:45 PM

5C.6 **Investigation of Accuracy of Speed Sensors for Process and Aging Compensation**

R. Shah, F. Cacho, D. Arora, S. Mhira, V. Huard, L. Anghel, STMicroelectronics, *TIMA*

This paper presents experimental results of different speed sensors that can be used for process and aging compensa-tion. Replica of critical path in ring oscillator, and a dedicated design of a sub-set functional critical path are compared with regard to microprocessor speed for reference. Measurements are performed on large sample sets for varied range of temperatures. Accuracy of speed compared to reference circuit to be monitored is discussed.

Wednesday Evening – Posters
Wednesday, March 14
6:00 PM – 9:00 PM

3D/2.5D/Packaging/MEMS

P-3D.1 **Optimal Design of Dummy Ball Array in Wafer Level Package to Improve Board Level Thermal Cycle Reliability (BLR)**
S. Jeong, J. Kim, A. Kim, B. Kim, M. Lee, J. Chang, H. Kang, S. Shin, and S. Pae, Samsung Electronics*

This paper investigates the effect of dummy ball on the board level reliability by performing thermal cycling test for 5 wafer level package products. The single dummy ball array at the chip corner boosted the BLR TC performance by 30~40% and the double dummy ball array by 92%. To maximize the dummy ball effect, the dummy ball array in the chip corners should be symmetric and co-optimized with die and package size.

Circuit Reliability/Aging

P-CR.1 **Study of Impact of BTI's Local Layout Effect Including Recovery Effect on Various Standard-Cells in 10nm FinFET**
M. Igarashi, Y. Uchida, Y. Takazawa, Y. Tsukamoto, K. Shibutani and K. Nii, Renesas Electronics Corp.

This paper presents impact of Local Layout Effect (LLE) of BTI on logic circuit by measuring Ring-Oscillators (RO) consisted with many kinds of standard cells in 10nm FinFET process. The measured Tpd degradation of all ROs are well correlated with estimated one without considering LLE of BTI and its maximum error rates is -16% and +13%. The LLE on BTI recovery effect is also evaluated and there is no obvious standard cell type dependency.

P-CR.2 **A Multi-bits/cell PUF Using Analog Breakdown Positions in CMOS**
K. H. Chuang, E. Bury, R. Degraeve*, B. Kaczer*, T. Kallstenius*, G. Groeseneken, D. Linten*, and I. Verbauwhede, imec-COSIC/ESAT , KU Leuven,* imec*

The breakdown position in a MOSFET is uniformly distributed, which can be utilized to generate multi-bit entropy out of a single transistor. A dedicated test structure for this analog-BD PUF was designed and fabricated in a commercial 40nm CMOS technology.The experiment and statistical analysis has shown that the analog-BD PUF is capable for multi-bit entropy generation but it requires significant improvement to replace the binary BD-PUF demonstrated in our previous work.

P-CR.3 **New Insights into the HCI Degradation of Pass-gate Transistor in Advanced FinFET Technology**
P. Ren, C. Liu, S. Wan, J. Zhang, Z. Yu*, N. Liu, Y. Sun, R. Wang*, C. Zhan, Z. Gan, W. Wong, Y. Xia and R. Huang*, Hisilicon Technologies Co., LTD, * Peking University*

HCI degradation of pass-gate transistor with forward and reverse stress biases in advanced FinFET technology is investigated comprehensively. Due to the bidirectional stress, pass-gate HCI shows larger degradation than conventional HCI, which can induce up to 50% error in predicting pass-gate delay degradation. Based on the proposed underlying physics, compact model of pass-gate HCI is developed and verified. With further analysis on circuit level, new simulation methodology is demonstrated.

P-CR.4 **Device-level Variability Tolerance of a RRAM-based Self-Organizing Neuromorphic System**

M. Pedro, J. Martin-Martinez, E. Miranda, M.B. Gonzalez, R. Rodriguez, F. Campabadal*, M.Nafria, Autonomous University of Barcelona, *Institut de Microelectronica de Barcelona*

Device modelling and system-level simulations are needed to verify neuromorphic systems tolerance to variability. In the present work, RRAM devices have been characterized and modelled for the implementation of a self-organizing simulated crossbar array. An unsupervised learning algorithm has been applied to the system for a simple image processing application, in order to provide a proof-of-concept of the proposed bio-inspired system tolerance to device-level variability.

P-CR.5 **Reliability Assessment of 4GSP/S Interleaved SAR ADC Reliability**
R. Lajmi, F. Cacho, O. David, J-P. Blanc, E. Rouat, S. Haendler, P. Benech, E. Lauga Larroze*, S. Bourdel*, STMicroelectronics, *IMEP-LAHC–Univ.Grenoble Alpes*

Inter-leaved Successive-Approximation-Register (ISAR) Analog to Digital Converter (ADC) are widely used because they have good tradeoff between high performance sampling rate, effective resolution, power and small area in GHz range.After presenting the design content, experimental results of aging at 40°C and 125°C are shown. Then, the analysis of reliability for all the critical blocks of the ADC is discussed, i.e. switches in capacitor array, comparator and latch.

P-CR.6 **Weighted Time Lag Plot Defect Parameter Extraction and GPU-based BTI Modeling for BTI Variability**
V. M. van Santen, J. Diaz-Fortuny, H. Amrouch, J. Martin-Martinez*, R. Rodriguez*, R. Castro-Lopez**, E. Roca**, Francisco V. Fernandez**, J. Henkel and M. Nafria*, Karlsruhe Institute of Technology (KIT), * Universitat Autonoma de Barcelona (UAB), **IMSE-CNM, CSIC/Universidad de Sevilla*

We present a novel BTI variability defect parameter extraction, which filters noise and RTN with the weighted time lag plot method (previously only used to characterize RTN) to obtain a noise-free BTI waveform and then extracts BTI defect parameters. Additionally, our novel high-performance parallel graphic card (GPU) based implementation of defect-centric PDO model. Together they tackle the challenge of characterizing and modeling BTI variability to ultimately evaluate BTI variability in circuits.

ESD/Latchup

P-EL.1 **A Case Study of ESD Trigger Circuit: Time-out and Stability**
K.-H. Meng, M. Moosa, C. Torres and J. Miller, NXP Semiconductors

This paper demonstrates the use of ETT (ESD trigger circuit time-out) measurement technique and AC loop-gain analysis to investigate the root-cause of oscillation in ESD trigger circuit (TC) design in 16nm Fin-FET technology. Measurement and simulation results are presented to investigate stickiness (TC's inability to time-out) and instability of different ESD TC designs by combining the complimentary analysis tools of transient ETT simulation and AC loop-gain analysis.

Failure Analysis

P-FA.1 **A Research Study on Unsupervised Machine Learning Algorithms for Early Fault Detection in Predictive Maintenance**
N. Amruthnath, DENSO Manufacturing Michigan

Fault detection being one of the key components of predictive maintenance, it is very much needed for industries to detect faults early and accurately. In this paper, we have chosen a simple vibration data collected from an exhaust fan, and have tried to fit different unsupervised learning algorithms to test its accuracy, performance and robustness. In the end, we have proposed a methodology to benchmark different algorithms and choosing the final model

Dielectrics - Gate, MOL, BEOL

P-GD.1 **New Insight on TDDB Area Scaling Methodology of Non-Poisson Systems**
T. Shen, K. B. Yeap, S. Ogden, C. Christiansen and P. Justison, GLOBALFOUNDRIES

Because of the large spatial variations across the wafer, the Poisson area scaling law is generally inapplicable. In this work, we demonstrate that although the previous non-Poisson statistical models may match with experimental data well, they are too conservative when projecting to the actual product area. A revised area scaling approach is proposed for a more aggressive yet more accurate fail rate projection that is essential for modern technologies.

P-GD.10 **Method to Assess the Impact of LER and Spacing Variation on BEOL Dielectric Reliability using 2D-Field Simulations for <20nm Spacing**
D. Kocaay, P. Roussel, K. Croes, I. Ciofi, A. Lesniewska and I. De Wolf, imec and KU Leuven

We developed a new 2D-model to quantify the impact of LER and spacing variations. We see that existing 1D-models are a good approximation down to 20nm spacing, but at lower spacings, 2D-models will be needed. Down to the 10nm spacing, our 2D-model gives reliable predictions and allows to define specifications of LER and spacing variation for advanced BEOL-spacings. Below 10nm spacing, when local field enhancements become too high, new models will need to be developed.

P-GD.2 **Reliability Evaluation of Defect Accounted Time-Dependent Dielectric Breakdown with Competing-Mixture Distribution**
S. Yokogawa and K. Tate, The University of Electro-Communications

Defect impacts to the whole lifetime distribution of time-dependent dielectric breakdown (TDDB) are discussed statistically by using a combination model of the competing risk and the mixture. The competing-mixture distribution well explains observations of TDDB lifetime. The model is able to describe realistic bathtub behaviors of failure rate without physical inconsistencies. Understanding the behavior of the failure rate supports the estimation of reliability with high accuracy.

P-GD.3 **Impact of Forming Gas Annealing on the Degradation Dynamics of Ge-Based MOS Stacks**
F. L. Aguirre, S. M. Pazos, F. R. Palumbo, S. Fadida, R. Winter*, M. Eizenberg*, National Scientific and Technical Research Council (CONICET), UTN-CNEA* Technion-Israel Institute of Technology*

Influence of FGA on Ge based MOS is analyzed in terms of electrical stress. The FGA reduces the charge trapping for stress at negative bias, which is a common trend regardless of the HK stack. It indicates that a considerable part of the interface defects with energies close to the valence band existing in the oxide-semiconductor interface result passivated during the FGA. Ge- and InGaAs-based MOS stacks show opposite dependencies on the FGA process.

P-GD.4 **Reliability of MgO in Magnetic Tunnel Junction formed by Sputtered MgO and Oxidation of Mg**

A. Teramoto, J-I Tsuchimoto, M. Hayashi, H-W Park, K. Hashimoto, T. Suwa and S. Sugawa, Tohoku University

The film property and the breakdown characteristics of the MgO films formed by the RF sputtering of MgO and oxidation of Mg in CoFeB/MgO/CoFeB structure. The both RF-MgO and Mg oxidation film property improved by the annealing. The breakdown of the RF-MgO depends on the stress current during the constant current stress, however that of the Mg oxidation film occurs at the defect site.

P-GD.5 **Study of Dynamic TDDB in Scaled FinFET Technologies**
K. Joshi, S.W. Chang, D.S. Huang, P.J. Liao, Y.–H. Le, Taiwan Semiconductor Manufacturing Company

Impact of SHE has been studied on FinFET devices under dynamic stress. A large channel temperature increase is observed under On-State stress which leads to degradation of TDDB, however, less impact of Off-State stress. MC simulators are developed to predict Off-State, On-State and Dynamic TDDB stress. It is shown that SHE in FinFETs leads to TDDB degradation only at higher bias, however, at use conditions; SHE has little impact for both NMOS & PMOS devices.

P-GD.6 **Dielectric Breakdown in Hexagonal Boron Nitride Dielectric Stacks**
X. Liang, F. Palumbo, Y. Shi, F. Hui, B. Yuan, X. Jing and M. Lanza Martinez, Soochow University and *National Scientific and Technical Research Council (CONICET),*

Hexagonal Boron Nitride (h-BN) could be a competitive solution due to its intrinsic excellent insulating ability and good interaction with graphene and other two dimensional (2D) materials. The implementation of new materials in electronic devices requires deep analyses to predict long-term degradation. This paper presents the first device-level reliability study of h-BN dielectric stacks and the complete dielectric breakdown (BD) process.

P-GD.7 **Percolation Defect Nucleation and Growth as a Description of the Statistics of Electrical Breakdown for Gate, MEOL and BEOL Dielectrics**
Y.C. Ong, S.C. Lee and A.S. Oate, Taiwan Semiconductor Manufacturing Company

We show that gate, middle end of line (MEOL) and back end of line (BEOL) dielectrics used in advanced Si technologies exhibit a common mechanism of breakdown involving the formation (nucleation) and growth of localized percolation defects. Consequently, industry standard reliability evaluations likely significantly underestimate dielectric reliability in circuit applications.

P-GD.8 **Oxide Breakdown Path as a Nanoscale Electro-Optical Switch/Sensor**
Y. Zhou, D. S. Ang, P. S. Kalaga, and S. R. Gollu, Nanyang Technological University

Visible-light-controlled resistance switching of the oxide breakdown path is demonstrated. Two distinct digital switching behaviors pertaining to the soft and hard oxide breakdown are revealed for the first time. For soft breakdown, the leakage current is decreased when the light is turned on, and is increased when the light is turned off. For hard breakdown, it behaves oppositely. The results suggest that the breakdown path may function as a nanoscale electro-optical switch/sensor.

P-GD.9 **High Voltage Time-Dependent Dielectric Breakdown in Stacked Intermetal Dielectrics**
S. H. Shin, Y-. P. Chen, W. Ahn, H. Guo, B. Williams, J. West, T. Bonifield, D. Varghese, S. Krishnan and M. A. Alam, Purdue University

There are increasing demands on high power applications. A new multi-kV voltage transformer, which uses IC-backend intermetal dielectric as an ultra-compact capacitive voltage-divider to connect high and low

voltage ICs, is easily integrated with multi-chip IC platform. The fundamental understanding of DC, AC, and thickness-dependent dielectric breakdown of this CMP-polished, stacked PECVD dielectric, will frame its properties in the broader context of TDDB-theory of traditional dielectrics, and will encourage diversified use of the core technology.

Metallization Reliability

P-MR.1 **Electromigration Failure Rate of Redundant Via**
J.-G. Ahn, P.-C. Yeh and J. Chang, Xilinx, Inc.

We derived two methods to get Electromigration (EM) Failure Rate of redundant via (RV) by Monte Carlo (MC) simulation and analytic formulation and showed the results are identical. The two methods are applied to get a simple trend, which can be used to predict EM Failure Rate of general RV cases.

P-MR.2 **Transient Self-Heating Modeling and Simulations of Back-End-of-Line Interconnects**
A. Kim, B. Li and B. Linder, IBM Systems

We present an enhanced steady-state thermal conductance model improved from the previously reported model and compact transient models that accurately predict time-dependent thermal behavior of an isolated metal carrying transient electrical signal embedded in dielectric material. Results of analytical models developed and presented in this work are in excellent agreement with those obtained by fully transient two-dimensional finite element simulations. Use of analytical models is much more advantageous over time-consuming finite element simulations.

P-MR.3 **Modeling Self-Heating Effects in advanced CMOS Nodes**
M. Arabi, X. Federspiel, A. Cros, V. Huard and C. Ndiaye, STMicroelectronics

In this paper, we analyzed the impact of the self-heating, observed on Back End of Line (BEoL) structures and NMOS transistors, in technology 28nm FDSOI. The metal characterization is required to calculate the thermal resistance (Rth). A given model relate the calculated thermal resistance to thermal conductivity (k). Rth and k are the input data used for the BEoL self-heating simulation.

Memory Reliability

P-MY.1 **Correlation between SET-State Current Level and Read-Disturb Failure Time in a Resistive Switching Memory**
P. C. Su, C. W. Wang, and Tahui Wang, National Chiao-Tung University

The relationship between SET-state current level and read-disturb failure time in a tungsten oxide RRAM is characterized and modeled. We found that read-disturb failure time is greatly improved by several orders of magnitude as SET-state current level increases a few times. We develop an analytical model to correlate read-disturb failure with SET-state current level. Our model provides a physical insight into the geometric effect of a conductive filament on read-disturb failure time.

P-MY.2 **Sub-pJ Consumption and Short Latency Time in RRAM Arrays for High Endurance Applications**
G. Sassine, C. Nail, L. Tillie, D. Alfaro Robayo, A. Levisse, C. Cagli, K. El. Hajjam, J.F. Nodin, E. Vianello, M. Bernard, G. Molas, E. Nowak. CEA, LETI, MINATEC Campus

Program operations are optimized for low power and short latency time application in RRAM kb arrays. Origin of consumption in SET and RESET operations is quantified on RRAM technology. Specific patterns are evaluated to reduce latency and energy consumption. Innovative circuit with on the fly switching detection is proposed, allowing to reduce programming consumption down to single pJ in large memory arrays.

P-MY.3 **High-Temperature and High-Field Cycling Reliability of PZT Films Embedded within 130 nm CMOS**
G. Walters, P. Chojecki, A. Garraud, S. Summerfelt, J. A. Rodriguez*, A. G. Acosta* and T. Nishida, University of Florida, *Analog Technology Development, Texas Instruments*

We present a reliability study of PZT-polarization retention after exposure to high temperatures and high-field cycling. Extraction of Preisach distribution after thermal depolarization and imprint confirms these observations: positive coercive voltage changes up to 45% while negative coercive voltage hardly changes (8%). Under accelerated aging via high electric fields (2.4V), maximum wake-up at 10^6 cycles followed by fatigue >10^8 cycles are observed. Asymmetry in coercive voltage is minimized after wake-up and remanent polarization maximized.

P-MY.4 **Suppression of Endurance-stressed Data-retention Failures of 40nm TaOx-based ReRAM**
Shouhei Fukuyama, Kazuki Maeda, Ryutaro Yasuhara, Shinpei Matsuda and Ken Takeuchi, Chuo University, *Panasonic Semiconductor Solutions Co., Ltd.*

This work investigates data-retention characteristics after different set/reset endurance cycles in ReRAM. The reliability of ReRAM depends on data-retention time in LRS, while data-retention time of HRS improves by the proposed write method "Finalize". The current distribution of LRS shifts overall to HRS side. Thus, the data-retention characteristics in LRS are determined by typical cells of the major current distribution. The physical model which is consistent with both endurance stress and data-retention characteristics are proposed.

P-MY.5 **Relaxing the STT-MRAM Reliability Challenge by Scaling MgO Thickness**
BJ O'Sullivan, S Van Beek, Ph. J. Roussel, S. Rao, W. Kim, S. Couet, J. Swerts,F. Yasin, D. Crotti, D. Linten, G. Kar, imec *also at KU Leuven,*

In this work, we detail a novel methodology to extract the magnetisation switching and breakdown characteristics from a single d.c. ramped voltage stress (RVS) measurement of STT-MRAM devices. We demonstrate how the switching and breakdown parameters are strongly interdependent for ultra-thin MgO layers. We validate this methodology by successfully correlating our results with the more widely reported pulsed-breakdown results.

P-MY.6 **Chip-Level Characterization and RTN-Induced Error Mitigation Beyond 20nm Floating Gate Flash Memory**
T. W. Lin, S.H. Ku, C.H. Cheng, C.W. Lee, J.-H., W.-J. Tsai, T.C. Lu, W.P. Lu, K.C. Chen, T. Wang, and C.-Y. Lu, Macronix International Co.

Vt instability caused by giant RTN in floating-gate flash memories in 1xnm is studied. Experiments reveal that the RTN would cause a tail which re-distributes to a "Gaussian-shape" rapidly and was measured by the product tester. A Multi-Times Verify (MTV) method to mitigate the tail is also exhibited. Further, a probability model to portray the compact Vt distribution under MTV is proposed. The impact of MTV on the reduction of Error-correcting-code bit is also demonstrated.

P-MY.7 **Cross Error Elimination ECC by Horizontal Error Detection and Vertical-LDPC ECC to Increase Data-Retention Time by 230% and Acceptable Bit-Error Rate by 90% for 3D-NAND Flash SSDs**
S. Suzuki, Y. Deguchi, T. Nakamura, K. Mizoguchi and K. Takeuchi, Chuo University,

XEE ECC with HED and V-LDPC is proposed to extend the data-retention lifetime of 3D-TLC NAND flash. HED improves the error correction capability of LDPC by evaluating the error bits in the horizontal direction. Moreover, V-LDPC improves the worst reliability in each WL in the vertical direction. This paper investigates the reliability of 3D-TLC NAND flash by XEE ECC. As a result, the data-retention lifetime and acceptable BER are extended by 230% and 90%, respectively.

Process Integration

P-PI.1 **Investigation of Monolayer MX_2 as Sub-Nanometer Copper Diffusion Barriers**
Kirby Smithe, Zhongwei Zhu, Connor Bailey, Eric Pop* and Alex Yoon, Lam Research Corp., *Stanford University*

We investigate four monolayer materials – MoS_2, WS_2, $MoSe_2$, and WSe_2 – on Si as possible sub-nm Cu diffusion barriers. SEM and TEM images suggest that W-based TMDs act as barriers up to 360°C, while Mo-based TMDs fail as low as 300°C. SEM indicates failure occurs as pinholes, suggesting mechanical damage may be the origin of failure. Further analysis by XPS on as-grown TMDs indicates that directly-grown TMDs still have potential as sub-nm diffusion barriers.

Product Reliability

P-PR.1 **Evaluation on Flip-flop Physical Unclonable Functions in a 14/16-nm Bulk FinFET Technology**
H. Zhang, H. Jiang, M.R. Eaker, K.J. Lezon, B. Narasimham, N.N. Mahatme**, L.W. Massengill, B.L. Bhuva, Vanderbilt University, Nashville TN 37212, 2Broadcom Corporation*

Physical unclonable functions (PUF) has been used to securely authenticate devices in electronic systems. In this paper, different flip-flop (FF) designs at a 14/16-nm bulk FinFET technology node have been evaluated for suitability as PUF generator. Randomness, repeatability and uniqueness is considered to rank order different FF designs. FF-based PUFs using reduced supply voltage are seen to be more promising compared to those for nominal supply voltages.

Photovoltaics

P-PV.1 **Charge State Evaluation of Passivation Layers for Silicon Solar Cells by Scanning Nonlinear Dielectric Microscopy**
*K. Kakikawa, Y. Yamagishi, K. Tanahash*i, H. Takato* and Y. Cho, Tohoku University, *National Institute of Advanced Industrial Science and Technology*

Nano scale charge states in Al3O3 passivation layers of Si solar cells and at Al3O3/Si interface were evaluated by using scanning nonlinear dielectric microscopy. The inhomogeneous distribution of fixed charge Qox in Al3O3 thin film and interface density of sate Dit was observed. Variations of Qox and Dit caused by annealing were clearly detected. Moreover, increase of negative fixed charge density by annealing was quantitatively evaluated.

P-PV.2 **Performance Improvement of Tandem Amorphous / Microcrystalline Si Photovoltaic Modules under Changes in Illumination Conditions**

*F. Ricco Galluzzo, A. Scuto, C. Gerardi 3, A. Battaglia4, A. Canino***, F. Aleo 3 and S. Lombardo, CNR IMM, *Università degli Studi di Catania, **ENEL Green Power, ***3SUN S.r.l.*

The Staebler and Wronski light soaking effect in a-Si:H implies a solar cell performances worsening. Previous our stress tests indoor on a-Si:H and tandem solar cells have proved that under suitable conditions an improvement of the cell perfomances is possible. In this work, we report on stress tests outdoor on commercial tandem amorphous/microcrystalline Silicon devices, highlighting the improvements of their electrical performances in the afternoon. Possible causes of such effect are discussed.

Reliability Testing

P-RT.1 **Effect of HCI Degradation on the Variability of MOSFETS**
C. Zhou, K.A. Jenkins, P.I. Chuang and C. Vezyrtzis, IBM T.J. Watson Research Center

The effect of HCI (hot-carrier injection) degradation on the variability of FETs is studied with a novel test structure. Using a space- and time-efficient technique, a large number of degradation measurements can be taken in the time usually used for a single device. Studies with this circuit have shown that variability of 14nm finFETs is actually reduced by the degradation caused by HCI stress.

P-RT.2 **Temperature and Voltage Effects on HTRB and HTGB Stresses for AlGaN/GaN HEMTs**
O. Chihani, L. Theolier, A. Benssousan, J.-Y. Deletage, A. Durier* and E. Woirgard, Univ. Bordeaux, CNRS, *2 IRT Saint-Exupery*

We investigate the degradation of AlGaN/GaN HEMTs submitted to HTRB and HTGB step-stresses. Steps in terms of temperature and voltage were done in order to distinguish the effect of each stressor. The main aim is to establish a lifetime model taking account multiple degradation mechanisms for a large range of temperature and voltage. The experiments evidenced two failure rate mechanisms that are activated simultaneously within the range of temperature and voltages selected.

P-RT.3 **Interaction of Permeats During the Measurement of Permeation Coefficients of Dense Polymer Films Under Realistic Conditions**
A. Piekarczyk, X. Xu, M. Köhl, K.-A. Weiß, Fraunhofer Institute for Solar Energy Systems ISE

In this publication the simultaneous measurement of several permeates are analyzed showing the interdependence of permeation rates of three major permeates (water vapor, oxygen and nitrogen gas) depending on their concentration. Based on these results the measurements of the permeability for single permeates can only be seen as an approximation by ignoring competitive effects of different permeates as found for most application environments, like in photovoltatics.

P-RT.4 **Polysilicon Resistor Stability Under Voltage Stress for Safe-Operating Area Characterization**
C. Kendrick, M. Cook, J. Gambino, T. Myers, J. Slezak and Y. Watanabe, ON Semiconductor

High resistance polysilicon resistors have been characterized by DC and pulsed I-V measurements over temperature, and DC and pulsed voltage stress/measurement cycling. The combination of these measurements along with resistor linearity and electromigration are used to determine the maximum safe-operating area. It is shown that the resistance shifts at high current conditions cannot be explained by electromigration alone, and are instead attributed to changes in the g polysilicon resistor itself.

P-RT.5 **Reliability Characteriscs of MIM Capacitor Studied Using ΔC-F Characteristics**
S. C. Kang, S. K. Lee, S. Heo, S. M. Kim, S. K. Lim and B. H. Lee, Gwanju Institute of Science and Technology

We propose a simple monitoring method for the quality of MIM capacitor. The differences in the slope of C-F curve at low and high frequency are found to be a good indicator showing the difference in the reliability characteristics of MIM capacitor. Asymmetric interface trap generation near top or bottom electrode could be monitored and clear difference was observed at various dielectric thicknesses, measurement temperature and stack structures.

Soft Error

P-SE.1 **Investigation of Alpha-Induced Single Event Transient (SET) in 10 nm FinFET Logic Circuit**
T. Uemura, S. Lee, D. Min, I. Moon, J. Lim, S. Lee, and S. Pae, Samsung Electronics

This paper investigates alpha-induced single event transient (SET) in combinational-logic in 10 nm bulk FinFET technology. FinFET technology improves SET in combinational-logic as well as single event upset (SEU) in flip-flops. However, the improving ratio in SET is ten times smaller than that in SEU. As a result, SET ratio to SEU in 10 nm FinFET technology is higher than that in bulk planer technologies.

P-SE.2 **Study of TID Effects on One Row Hammering using Gamma in DDR4 SDRAMs**
D. Yun, M. Park, C. Lim and S. Baeg, University of Hanyang

The Total Ionizing Dose (TID) effects on DDR4 SDRAM were investigated using Co60 γ-rays. While degradation in retention time was observed, no retention error was observed at a retention time of 64-ms in 80 °C and 90 krad exposure. Unlike that in retention time degradation, significant degradation in one row hammering threshold was observed. The threshold was reduced by up to 153 k, which is a 218 % reduction when compared to pre-radiation values.

P-SE.3 **Sensitivity to Soft Errors of NMOS and PMOS Transistors Evaluated by Latches with Stacking Structures in a 65 nm FDSOI Process**
K. Yamada, H. Maruoka, J. Furuta and K. Kobayashi, Kyoto Institute of Technology

Three different latch structures are fabricated in a 65 nm FDSOI process.We evaluate soft-error tolerance of latches by device simulations and α particle, neutron irradiation tests in order to identify which transistor type is dominant to cause soft errors. The latch structure including an inverter with stacked NMOS and unstacked PMOS transistors has enough tolerance against soft errors. It suggests that soft errors are dominant on NMOS transistors in the terrestrial region.

P-SE.5 **Design Soft-Error-Aware Circuits with Power and Speed Optimization**
H. Jiang, H. Zhang, B. Narasimham, L. W. Massengill, and B. L. Bhuva, Vanderbilt University, *Broadcom Corp.*

Even though power consumption for ICs has emerged as the most constraining aspect, it is important to deliver circuit designs that also meet area, speed, and SER specifications. DFF designs with different threshold voltages are fabricated at the 14/16-nm bulk FinFET CMOS technology node and evaluated for speed and SER from a power perspective. The results are used to create a model that will allow designers to identify optimum design and operating parameters to meet multiple design constraints.

P-SE.6 **Single-Event Effects on Optical Transceiver**
K. J. Lezon, S.-J. Wen, Y.-F. Dan*, R. Wong*, B. L. Bhuva, Vanderbilt University, *Cisco Systems*

All communications systems use optical modules to achieve data transfer speeds in 10's of GHz range. With increasing reliance on communication systems, the impact of soft errors in optical transceiver modules

has become a primary concern for system performance. This paper examines neutron-induced soft-error rates and associated failure modes of optical transceivers.

System Reliability

P-SR.1 **Weibull Cumulative Distribution Function (CDF) Analysis with Life Expectancy Endurance Test Result of Power Window Switch**

M. Lee, J. Kim, D. Lim, and D. Cho, LS Automotive

The first goal of this task is to develop realistic worst case lifetime endurance test specification because existing large number of switch test standards cannot induce degradation mechanism which makes the switches less reliable. 2nd goal is to assess quantitative reliability status of PWS based on test specification newly developed thru this project and to develop how to improve product reliability based on PWS degradation mechanisms.

P-SR.2 **Development of a Flexible Wearable Biometric Band and Smartphone Application for Remote User-Monitoring**

A. Pradeep Lall, B. Hao Zhang, C. Rahul Lall, Auburn University, * Stanford University*

Reducing paramedic response times to five minutes could nearly double survival rates of patients experiencing life-threatening medical conditions. Maintenance of an independent lifestyle with a comparable level of monitoring requires the development of devices which can provide continuous monitoring and timely medical intervention when needed, without the tie-down constraints of a hospital setting. In this project, a novel rapid-response flexible wearable bioelectronics device has been developed.

Transistors/Beyond CMOS

P-TX.1 **Low Frequency Noise in MoS_2 Negative Capacitance Field-effect Transistor**

S. Alghamdi, M. Si, L. Yang and P.D. Ye, Purdue University

We report for the first time on low frequency noise studies in MoS2 NC-FETs. The low frequency noise is found to decrease with thicker ferroelectric HZO, in contrast to the conventional high-k MOSFETs, the negative capacitance concept of the ferroelectric HZO practically explains the noise measurement results.The key result is that the negative capacitance can not only improve the device on- and off-state performance, but can also suppress the noise.

P-TX.2 **Hot Carrier Effects on the RF performance Degradation of Nanoscale LNA SOI nFETs**

D.P. Ioannou, Y. Tan, R. Logan, K. Bandy, R. Achanta, P.C. Wang, D. Brochu and M. Jaffe GLOBALFOUNDRIES

We report on the hot carrier effects on the DC and small signal RF parameters of nanoscale SOI nMOSFETs developed for high performance low noise amplifier circuits. This is the first study done on SOI nFETs scaled down to 35 nm where stress experiments specifically designed to address the LNA operational bias conditions and RF figures-of-merits are carried out. The obtained results lay the foundation for a reliability-aware RF LNA design.

P-TX.3 **Hot Carrier Induced TDDB in HV MOS: Lifetime Model and Extrapolation to Use Conditions**

G. Sasse, NXP Semiconductors

In this paper we report on a lifetime extrapolation model for hot carrier induced time dependent dielectric breakdown in HV MOS devices. The proposed lifetime model is based on findings from literature, supplemented with new experimental data on several types of HV pMOS devices. Furthermore the methodology to make accurate lifetime extrapolations towards use conditions is discussed.

P-TX.4 **Key Parameters Driving Transistor Degradation in Advanced Strained SiGe Channels**
*V. Huard, C. Ndiaye, M. Arabi, N. Parihar** X. Federspiel, S. Mhira, S. Mahapatra** and A. Bravaix**
*STMicroelectronics, *ISEN-REER, IM2NP, ** IIT Bombay*

The paper proposes new physical explanations to explain the impact of compressive strain, germanium content and nitrogen content on NBTI and HCI degradation on pMOS transistors. Both compressive strain and Ge content impact on NBTI degradation is found to relate to modifications in band structure of channel. Excellent agreement between theory and experimental results shed new light on NBTI degradation mechanism and the physics lying behind. HCI degradation is well explained by recent energy-driven theory.

P-TX.5 **Prediction of NBTI Stress and Recovery Time Kinetics in Si Capped SiGe p-MOSFETs**
N. Parihar and S. Mahapatra, IIT Bombay

Measured NBTI stress and recovery temporal kinetics at different experimental conditions are predicted in Si and SiGe p-MOSFETs. Mutually uncorrelated contributions from interface and bulk trap generation and hole trapping in pre-existing bulk traps are used to predict the overall threshold voltage shift. Process variations such as Si cap and quantum well thickness and Ge% in QW and their impact on stress-recovery kinetics are modeled.

P-TX.6 **Investigation on the Amplitude Coupling Effect of Random Telegraph Noise (RTN) in Nanoscale FinFETs**
S. Guo, Z. Lin, R. Wang, Z. Zhang, Z. Zhang, Y. Wang and R. Huang, Peking University

Based on the complex RTN data in FinFETs, the impacts of the trap coupling effect are studied statistically. The coupling effect is found to be enhanced by the double-side coupling mechanism in FinFETs. The non-monotonic VG dependence of amplitude coupling strength is observed, which is contributed by the evolution of channel percolation paths. In addition, the impacts of stress on the coupling strength are studied. The impacts of amplitude coupling on circuits are also investigated.

P-TX.7 **PBTI Evaluation of $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ Nanowire FETs with Al_2O_3 and $LaAlO_3$ Gate Dielectrics**
Y. Li, K. L. Wang, S. Y. Di, P. Huang, G. Du and X. Y. Liu, Institute of Microelectronics, Peking University

This paper investigates the PBTI of InGaAs nanowire FETs with different channel and gate dielectrics by 3D-Kenetic Monte Carlo method. It is found that indium and gallium components of channel impact on PBTI, and there is worse PBTI with larger In component. Moreover, PBTI along nanowire thickness (TNW) and width (WNW) directions shows different due to non-uniform electrical field. With sandwich structure channel, the Vth shift difference of TNW/WNW can be enlarged in high temperature.

P-TX.8 **Interface Engineering of Ferroelectric Negative Capacitance FET for Hysteresis-Free Switch and Reliability Improvement**
*C-C Fan, C-H Cheng, C. Liu, C-Y Tu, G-L Liou and C-Y Chang, National Chiao-Tung University and *National Taiwan Normal University*

In this work, we successfully achieve a hysteresis-free NCFETs by exploiting a defect passivation scheme and simultaneously provide a new insight into the gate-oxide reliability of NCFET. The fluorine-passivated HfAlOx NCFET features a sub-30-mV/dec, a negligible hysteresis-free switch of ~10mV and >1E7 Ion/Ioff ratio. Most importantly, fluorine passivation effectively suppress the generation of shallow traps during stress to maintain NC operation and SILC immunity, which has been verified by transient pulse IV measurement.

Wide Band Gap/Compound/Optoelectronics

P-WB.1 **Threshold Voltage Shift and Interface/Border Trapping Mechanism in Al_2O_3/AlGaN/GaN MOS-HEMTs**

J. Zhu, B. Hou, L. Chen, Q. Zhu, L. Yang, M. Mi, X. Zhou, P. Zhang, X. Ma and Y. Hao, Xidian University

Trap states and the induced voltage shift in Al2O3/ AlGaN/GaN MOS-HEMTs were studied. Interface trapping is found dominant at low gate voltage, and then border trapping become remarkable with voltage above 5 V due to the extra trapping energy. At low field, border de-trapping has a very long emission time constant, resulting in the maintainable voltage shift; while Vth recovery can be achieved after "breakdown" due to the tunneling de-trapping mechanism at high field.

P-WB.2 **Investigation of the Pulsed-IV Degradation Mechanism of GaN-HEMT under High Temperature Storage Tests**

Y. Kurachi, Y. Tateno, T. Yonemura, M. Furukawa*, H. Yamamoto, Y. Nose and S. Shimizu, Sumitomo Electric Device Innovations, Inc., *Sumitomo Electric Industries, Ltd.*

The purpose of this study is to investigate the physical mechanism of pulsed-IV degradation under high temperature storage tests. Using the measurements of the pulsed S-parameters immediately after the voltage stress was applied, we carried out the delay analysis. As a result, we found that the so-called "virtual gate" region extended toward the drain electrode due to high temperature storage, and we concluded that the electron tunnel injection probability increased and degraded the pulsed-IV characteristics.

P-WB.3 **Failure Mode Analysis of GaN-HEMT Under High Temperature Operation**

Y. Tateno, Y. Kurachi, H. Yamamoto* and T. Nakabayashi, Sumitomo Electric Industries, Ltd., *Sumitomo Electric Device Innovations, Inc.*

The purpose of this study is to investigate the physical mechanism of the threshold voltage shift of GaN-HEMT in high temperature storage tests. Using microscopic Raman spectrometry, we found the crystal extends vertically. From this observation, we concluded that one possible reason for the threshold voltage shift in high temperature storage tests is the change of the piezopolarization density dependent on the change of the crystal distortion under the gate metal.

P-WB.4 **A Novel GaN HEMT Degradation Mechanism Observed During HTST Test**

F. Iucolano, A. Parisi, S. Reina, and A. Chini, STMicroelectronics, *University of Modena and Reggio Emilia*

The Imax current reduction after high temperature short term tests in RF-GaN HEMT was investigated. A "critical-voltage" like degradation was observed with voltage levels correlated with the pinch-off voltage of the MIS structure. The recoverable nature of the phenomena and the positive temperature dependence of both the IMAX reduction and leakage currents within the passivation layer allowed us to propose a novel interpretation based on a charge-injection process from the FP into SiN/AlGaN.

P-WB.5 **Investigation of Degradation Phenomena in GaN-on-Si Power MIS-HEMTs under Source Current and Drain Bias Stresses**
C .Y. Yang, T. L. Wu, T. E. Hsieh and E. Y. Chang, National Chiao-Tung University

We investigate the degradation phenomena in GaN-on-Si MIS-HEMTs in the cascode topography for E-mode power switching applications. Different stress conditions are used to investigate the IS and VD dependent degradation. There are two results from findings. One is the phenomena under a low VD stress, the other is a different degradation phenomena under high VD stress. We also show the difference from different IS induced. The conclusion is instability degradation is mainly triggered by VD.

Session 6A - FOCUS SESSION: To Space and Beyond: Methods and Themes to Develop Reliable Systems!

Session Chairs: *Guneet Sethi, Amazon Lab 126, Rob Kwasnick, Intel*
Thursday, March 15

8:00 AM - Session Introduction

8:05 AM
6A.1 **Automotive Functional Safety (Invited)**
R. Mariani, Intel

8:30 AM
6A.2 **Making the Connection Between Physics of Failure and System-level Reliability for Medical Devices (Invited)**
A. Fenner, Medtronic

8:55 AM
6A.3 **Key Attributes to Achieving 99.999+ Satellite Availability (Invited)**
B. Kosinski, Space Systems/Loral, LLC

9:20 AM
6A.4 **Comprehensive Process of Quality and Reliability for Organic Light Emitting Diode Applied Flexible Mobile Display (Invited)**
J. Park, Samsung

9:45 AM
6A.5 **Prognostics and Health Monitoring of Electronic Systems: A Reliability-Physics Approach (Invited)**

P. Lall, Auburn University

Session 6B - Failure Analysis

Session Chairs: *Kevin Johnson, Intel, Baohua Niu, TSMC*
Thursday, March 15

8:00 AM - Session Introduction

8:05 AM
6B.1 **Solving Critical Issues in 10nm Technology using Innovative Laser-based Fault Isolation and DFT Diagnosis Techniques**
L. Zaren Endrinal, R. Kinger, L. Ranganathan and A. Sheth, Qualcomm Technologies, Inc.

This paper will present an innovative technique in performing fault isolation in our latest 10nm product to resolve 35% yield loss issue due to stuck-at-fault (SAF) logic failures during first silicon bring up. The main issue was the lack of viable diagnostic results, which made this problem almost impossible to solve. With the use of special DFT and new fault isolation techniques, we were able to crack the case and find the root cause.

8:30 AM
6B.2 **Cathodoluminescence Spectroscopy for Failure Analysis and Process Development of GaN-Based Microelectronic Devices (Invited)**
C. Monachon, Attolight

8:55 AM
6B.3 **Electrical Method to Localize the High-Resistance of Nanoscale CoSi2 Word-Line for OTP Memories**
M.-Yi Lee, T.-Y. Chang, W.-F. Hsueh, L.-K. Kuo, D.-J. Lin, Y.-H. Chao, U. J. Tzeng and C. Y. Lu, Macronix International Co.

The defective high-resistance in a nanoscale Cobalt silicide (CoSi2) word-line (WL) was observed for a high density of non-volatile memory. An electrical method through analyzing the variation of threshold voltage of memory cells with its physical position is proposed to help the localization of defective position, identify the root cause of CoSi2 agglomeration, and also provide a method to detect this kind of defective WL.

9:20 AM
6B.4 **Estimating Transistor Channel Temperature using Time-Resolved and Time-integrated NIR Photoemission (Invited)**
F. Stellari, IBM

9:45 AM
6B.5 **BEOL TDDB Reliability Modeling and Lifetime Prediction Using Critical Energy to Breakdown**
*P. S.Chen, S.C. Lee[*], A. S. Oates[*], and C. W. Liu[**], National Taiwan University, *Taiwan Semiconductor Manufacturing Company, **National Nano Device Laboratories*

By combining modeling of the leakage current of BEOL capacitors with TDDB data, we show that the hard breakdown of capacitors during electrical stress is related to the leakage current flowing through the dielectric. Moreover, we find the breakdown occurs after a critical energy density has been dissipated in the dielectric. We find that the tunneling currents do not contribute to the breakdown due to the absence of anode hole injection for the metal-insulator-metal structure.

Session 6C - Photovoltaics Reliability

Session Chairs: *Michael Daenen, Hasselt University, Karl-Anders Weiss, Fraunhofer - ISE*
Thursday, March 15

8:00 AM - Session Introduction

8:05 AM
6C.1 **Permanent shunting from passing shadows: Reverse-bias damage in thin-film photovoltaic modules (Invited)**
T. Silverman, NREL

8:30 AM
6C.2 **Modified Transformerless Dual Buck Inverter with Improved Lifetime for PV Applications**
A. Khan, L. Ben-Brahim, A. Gastli, Department of Electrical Engineering, Qatar University

Single-Phase grid-tied Photovoltaic (PV) inverter's reliability is severely deteriorated by the double grid frequency power pulsation, since this pulsation requires large unreliable DC-Link capacitors installation. Therefore, a modified Dual-Buck-Inverter (DBI) topology and control is proposed. The proposed modification allows utilizing the Common-Mode (CM) operation of the inverter to perform Active-Power-Decoupling (APD). Finally, the analyses were validated on a 3kW prototype and showed that a 30uF capacitor is adequate to achieve a ripple free DC-Bus voltage.

8:55 AM
6C.3 **Evaluation of the Silicon, Organic, and Perovskite Solar Cell Reliability with Low-frequency Noise Spectroscopy**
G. Landi, C. Barone, C. Mauro, S. Pagano and H. C. Neitzert, Università di Salerno

Low-frequency noise spectroscopy has been used to monitor electronic properties of solar cells under temperature or radiation stress. For all the investigated cells, the low-frequency noise analysis evidences a clear correlation of the recombination and the transport processes with the device performances.

9:20 AM
6C.4 **Mechanical and chemical adhesion at the encapsulant interfaces during the lamination of photovoltaic modules**
P. Nivelle, T.Borgers, E. Voroshazi*, J. Poortmans*, J. D'Haen, W. De Ceuninck, and M. Daenen,*
*Hasselt University, *imec,*

This work investigates the influence of the flux use on the adhesion strengthof encapsulants to the metallization/interconnection of a photovoltaic module as it can have a major effect on the long term reliability. In short, the influence of flux is predominantly determined by the encapsulant type. The differences measured in adhesion strength could be correlated to a difference in macro-scale roughness at the interface and in the quantity of solder particles present.

9:45 AM
6C.5 **A New Mechanism of Signal Path Charging Damage Across Separated Power Domain Deep N-Well Interface (Late News)**
Y.-L. Chu, TSMC

A new damage mechanism of cross domain interface from the non-DNW to DNW region is observed, which can be observed inside DNW. In addition, both NMOS and PMOS transistors are damaged instead of NMOS only. This new damage mechanism model is characterized and verified using test patterns in a 40nm logic process together with SPICE simulation results. Several prevention solutions to eliminate the charging damage are proposed and verified.

Session 6D - Memory Reliability

Session Chairs: *Alessandro Spinelli, Politecnico di Milano, Andrea Chimenton, Intel*
Thursday, March 15

10:30 AM - Session Introduction

10:35 AM
6D.1 **Investigation of Data Pattern Effects on Nitride Charge Lateral Migration in a Charge Trap Flash Memory by Using a Random Telegraph Signal Method**
Y. H. Liu, H. Y. Lin, Tahui Wang, W. J. Tsai, T. C. Lu*, K. C. Chen*, and Chih-Yuan Lu*, Dept. of Electronics Engineering, National Chiao-Tung University, *Macronix International Company Ltd.,*

Data charge pattern effects on nitride charge lateral migration and Vt retention loss in a charge trap flash memory is investigated by using an random telegraph signal method. We find that trapped hole lateral movement is dependent on the program Vt level of a neighboring bit through the modification of a built-in electric field. At a similar nitride electric field, trapped holes are found to be more mobile than trapped electrons in lateral migration.

11:00 AM
6D.2 **Impact of Specific Failure Mechanisms on Endurance Improvement for HfO2-based Ferroelectric Tunnel Junction Memory**
M. Yamaguchi, S. Fujii, Y. Kamimuta, S. Kabuyanagi, T. Ino, Y. Nakasaki, R. Takaishi, R. Ichihara, M. Saitoh, Toshiba Corporation

We conducted a detailed investigation on failure mechanisms for the HfO2 FTJ during set/reset cycling endurance by combining methodology of the well-known reliability evaluation (TDDB) and the memory-specific evaluation. As a consequence, we clarify the failure mechanism and successfully demonstrate a way to improve cycling endurance. Based on these findings, a potential cycling endurance over 10^6 cycles is shown to be expected, implying the HfO2 FTJ has a high potential for future non-volatile memory applications.

11:25 AM
6D.3 **Investigation of the Endurance of FE-HfO2 Devices by Means of TDDB Studies**
K. Florent, A. Subirats, S. Lavizzari*, R. Degraeve*, U. Celano*, B. Kaczer*, L. Di Piazza*, M. Popovici*, G. Groeseneken and J. Van Houdt, KU Leuven, *imec*

Ferroelectric HfO2 devices are potential candidates for non-volatile memory applications. However they often exhibit a pinched hysteresis, which requires the application of cycles to “wake-up” the device. In this paper, endurance of FE-Al:HfO2 MIM is investigated using TDDB measurements. An improvement in TDDB lifetime is observed with cycling. A hypothesis involving rearrangement of defects is proposed to explain this behavior.

1:10 PM
6D.4 **Carbon Electrode in Ge-Se-Sb Based OTS Selector for Ultra Low Leakage Current and Outstanding Endurance**
A. Verdy, G. Navarro, M. Bernard, S. Chevalliez, N. Castellani, E. Nolot, J. Garrione, P. Noé, G. Bourgeois, V. Sousa, M.-C. Cyrille and E. Nowak, CEA, LETI, MINATEC Campus

In this paper we study the reliability of a Ge-Se-Sb based OTS Selector. We highlighted that the Ti diffusion from the electrode appears to be the main mechanism responsible for the degradation of the device performances. We engineered a thin carbon layer as electrode, achieving an ultra-low leakage current lower than 10 pA and an endurance of 1G cycles. These results are among the best reported so far for an OTS selector technology.

1:35 PM
6D.5 **Reliability Benefits of a Metallic Liner in Confined PCM**
*W. Kim, Y. Xie**, Y. Kim**, T. Masuda*, S. Kim, R. Bruce, F. Carta, G. Fraczak, A. Ray, K. Suu*, C. Lam, M. BrightSky, J. J. Cha**, and Y. Zhu, IBM T. J. Watson Research Center, *ULVAC, Inc., **Yale University*

We demonstrate outstanding drift mitigation and void elimination as reliability benefits of a thin metallic liner. By tuning the resistivity of the liner, the confined PCM with a metallic liner yields an extremely low R-drift coefficient. We also show for the first time that confined PCM could have a self-recovering property by incorporating a metallic liner. The in-situ TEM results exhibit the robustness of the confined PCM that can recover by itself by void elimination.

2:00 PM
6D.6 **Area and Pulse Width Dependence of Bipolar TDDB in MgO STTRAM**
J. H. Lim, N. Raghavan, S.Mei, V.Naik,J.H. Kwon*, K.H. Lee*, K.L. Pey Singapore University of Technology and Design (SUTD), *GLOBALFOUNDRIES*

Results from the bipolar pulsed endurance test reveal that the breakdown voltage is dependent on the pulse width for a given applied voltage and area of MgO. Devices with lower pulse widths for the same overall stress duration have longer lifetime due to the self-heating effects that take a few microseconds to reach the saturation temperature. We prove that self-heating effects play a more dominant role than extrinsic etch damage effects in our samples.

2:25 PM
6D.7 **The First Observation of p-type Electromigration Failure in Full Ruthenium Interconnects (Late News)**
S. Beyne, S. Dutta, O. Varela Pedreira, N. Bosman*, C. Adelmann*, I. De Wolf, Z. Tokei* and K. Croes*, KU Leuven, *imec*

We show the first electromigration (EM) failures of full ruthenium interconnects with a cross sectional area of 60nm2. The void is observed at the anode, which demonstrates that in p-type metals, such as Ru, the electromigration force acts in the direction of the electric field. The conventional representation of electromigration as electrons transferring their momentum onto the metal ions, thus has to be adapted for such metals.

Session 6E - Reliability Testing

Session Chairs: *Kevin Manning, Analog Devices, Derek Slottke, Intel*
Thursday, March 15

10:30 AM - Session Introduction

10:35 AM
6E.1 **Lateral Profiling of HCI Induced Damage in Ultra-Scaled FinFET Devices with Id-Vd Characteristics**

M. Wang, R. G. Southwick, J. H Stathis and K. Cheng, IBM Research Division, T.J. Watson Research Center

In this work, we present an experimental method to obtain the location of the pinch-off point in a MOSFET biased in saturation. The proposed methodology enables lateral profiling of hot carrier induced defects directly from measured data without the need of extensive simulation or complicated analytical modeling.

11:00 AM
6E.2 **Ambient temperature and layout impact on self-heating characterization in FinFET devices**
P. Paliwoda, Z. Chbili, A. Kerber, D. Singh, D. Misra, GLOBALFOUNDRIES Inc., *New Jersey Institute of Technology*

Self-Heating effects are going to be increasingly significant in future nodes. Understanding self-heating measurement results is of vital importance. In this paper we show for the first time through measurement that the ambient temperature can affect self-heating measurement by up to 69%. Through a series of measurements at different temperatures and dissipated power, we show that the Si fin has a more dominant effect in heat transport and its varying thermal conductivity should be accounted.

11:25 AM
6E.3 **A New Method For Quickly Evaluating Reversible and Permanent Components of the BTI Degradation**
X. Garros, A. Subirats, C. Diouf, X. Federspiel*, V. Huard*, M. Rafik*, G. Reimbold, B. Gaillard, CEA-Leti, *ST Microelectronics*

A new method denoted SRP is proposed for a quick evaluation of the reversible and permanent NBTI components responsible for NBTI degradation. The technique which can be seen as a mathematical trick is useful for a fast comparison of process leverages impacting BTI. It can also provide a simple analytical compact model suitable for SPICE-like simulator.

1:10 PM
6E.4 **Threshold Voltage Bitmap Analysis Methodology: Application to a 512kB 40nm Flash Memory Testchip**
T. Kempf, V. Della Marca, L. Baron, F. Maugain, F. La Rosa, S.Niel, A. Regnier, J.-M. Portal*, P. Masson**, STMicroelectronics, *IM2NP, **EpOC / Nice Sophia-Antipolis University*

To answer demanding reliability requirements, the Flash memory technology development needs test chips to allow large statistical studies and a product-like approach. The use of such test chips must be carefully studied to separate peripheral effect on memory reliability, and to extract electrical parameters such as threshold voltage. In this abstract, we present a methodology of bitmap analysis to extract intrinsic and extrinsic parameters during reliability test of a 512kB Flash memory test chip.

1:35 PM
6E.5 **BVDSS (drain to source breakdown voltage) instability in shield gate trench power MOSFETs**
J. Hao, A. Ghosh, M. Rinehimer, J. Yedinak, M. A. Alam, ON Semiconductor, *Purdue University,*

We develop a constant current avalanche injection stress to test BVDSS instability in charge balance power MOSFETs. Our data shows this test is very sensitive to the BVDSS instability but HTRB (high temperature reverse bias) is not. We explain why this test is more sensitive than HTRB for BVDSS instability in charge balance MOSFETs. Furthermore, we show that during constant current stress, holes are injected into the shield oxide which results in the BVDSS instability.

2:00 PM

6E.6 **Effect of Measurement Speed (μs-800 ps) on The Characterization of Reliability Behaviors for FDSOI nMOSFETs**

*Y. Qu, R. Cheng, W. Liu, J. Li, B.Y. Nguyen**, O. Faynot***, N. Xu*, B. Chen, Y. Zhao, Zhejiang University, *University of California, **Soitec, Austin, ***CEA-Leti Minatec*

We experimentally investigate the impact of measurement speed (μs-800 ps) on the characterization of reliability behaviors, HCI and PBTI, for FDSOI nMOSFETs. The results show that, due to the severe self-heating effect (SHE) in the transistors, the I-V measurement speed could significantly affect the characterization of threshold voltage (VTH) shift and drain current (IDSAT) degradation after HCI and PBTI stress. Due to the inevitable SHE in the transistor channel caused by the long measurement time.

2:25 PM

6E.7 **Non-Poissonian Behavior of Hot Carrier Degradation Induced Variability in MOSFETs (Late News)**

R. Bottini, A. Ghetti, S. Vigano, M. G. Valentini, P. Murali, C. Mouli, Micron Technology Inc.

Previously, it was reported that Hot Carrier induced MOSFET Vth shift follows a Poissonian behavior. Here, we show new data deviating from this behavior. First, in the initial stage of the HC stress, Vth shift may exhibit a super-poissonian behavior. Second, for very high stress levels, HC Vth shift standard deviation tends to saturate to a maximum value. A new physical model able to explain these phenomena is proposed and validated with numerical simulations.

Session 6F - CMOS Process Integration session

Session Chairs: *Xavier Garros, CEA, Barry Linder, IBM*
Thursday, March 15

10:30 AM - Session Introduction

10:35 AM

6F.2 **Understanding Gate Metal Work Function (mWF) impact on Device Reliability - A Holistic Approach**

P. Srinivasan, R. Ranjan, S. Cimino, A. Zainuddin, B. Kannan, L. Pantisano, I. Mahmud, G. Dilliway, T. Nigam, GLOBALFOUNDRIES Inc.

The effect on device reliability due to gate metal work function (mWF) in thin and thick gate oxide FinFETs. Lower BTI is noticed for increasing WFM1 thickness for thin oxide nFETs. Higher degradation is seen for thin and thick oxide pFETs. A dual behavior is noticed for pFETs. For TDDB, t63% increases with increasing VT caused by modulation in WFM1 thickness. A physical model ispro posed which explains the observed reliability behavior.

11:00 AM

6F.3 **Performance & Reliability of 3D Architectures (Pifet, Finfet, Omegafet)**

A. Laurent X. Garros, S. Barraud, J. Pelloux-Prayer, M. Cassé, X. Federspiel, D. Roy*, E. Vincent*, G. Ghibaudo**, F. Gaillard, CEA-LETI, *STMicroelectronics, **IMEP-LAHC, Minatec/INPG*

The impact of 3D architectures and boosters on the trade-off performance/reliability is deeply investigated in this paper. "Finfet" transistor presents a slight superior trade-off than square shaped "Πfet" device because of little improved performance and similar BTI&HC reliability. "Ωfet" also offers a better compromise than Πfet due to improved BTI reliability. Finally strained SOI & SiGeOI devices are highly suitable since they allow boosting the transistor performance without any reliability penalty.

11:25 AM

6F.4 **Reliability Studies of a 10nm High-performance and Low-power CMOS Technology Featuring 3rd Generation FinFET and 5th Generation HK/MG**

A. Rahman, J. Dacuna, P. Nayak, G. Leatherman, S. Ramey, Intel Corporation

Development of an industry leading 10nm CMOS process technology with the highest reported drive currents and cell densities involved numerous enabling innovations, judicious choice of design rules, novel features, and most importantly a relentless pursuit of process-reliability co-optimization. This paper elaborates the process challenges to transistor scaling that once addressed, enabled meeting Intel's aggressive 10nm technology reliability targets.

1:10 PM

6F.5 **Effects of Far-BEOL Anneal on the WLR and Product Reliability Characterization of FinFET Process Technology**

H. Sagong, H. Kim, S. Choo, S. Yoon, H. Shim, S. Ha, T. Jeong, M. Choe, J. Park, S. Shin, and S. Pae, Samsung Foundry Business, Samsung Electronics,

Far-BEOL forming gas anneal has been used to passivate dangling bonds and to improve integrity of gate dielectric. The reliability study was conducted on 14nm FinFETs to study the effects of anneals using various gases (including high/normal pressure D2, H2, and N2). Despite that high pressure D2 anneal gave best I/O NFET HCI reliability, most of the other anneals also provided reasonable and comparable reliability results that can provide as more cost-effective alternate process approach.

1:35 PM

6F.6 **Bottom-up Methodology for Predictive Simulations of Self-heating in Aggressively Scaled Process Technologies**

D. Singh, O. Restrepo, P. P. Manik, N. Rao Mavilla, S. Pinkett, H. Zhang, E. Cruz Silva, J. B. Johnson, M. Bajaj, S. Furkay, P. Paliwoda, Z. Chbili, C. Christiansen, A. Kerber, S. Narasimha, E. Maciejewski, C.-H. Lin, GLOBALFOUNDRIES

A hierarchical methodology using combination of ab-initio phonon scattering, electron transmission & multi-scale FEM simulations is developed to accurately model material and device level self-heating in FinFET technologies. The framework is applied to capture heat dissipation paths and thermal resistance of FinFETs, interconnects and precision resistors. Excellent agreement against measurements and dependence on process technology is demonstrated across many device types without any fitting. The proposed methodology enables rapid evaluation and process mitigation of self-heating.

2:00 PM

6F.7 **Reliability of Dual-Damascene Local Interconnects Featuring Cobalt on 10nm Logic Technology (Late News)**

F. Griggio, J. Palmer, F. Pan, N. Toledo, A. Schmitz, I. Tsameret, R. Kasim, G. Leatherman, J. Hicks, A. Madhavan, J. Shin, J. Steigerwald, A. Yeoh, C. Auth, Intel

This paper discusses the reliability of a new metallization scheme for 10nm back end of line (BEOL) local interconnect. Electromigration (EM) and time dependent dielectric breakdown (TDDB) on Co fill

interconnects are investigated. Significant innovation in process manufacturing are delivered to meet the reliability challenges of technology scaling. Electromigration time to failure is observed to be at least four orders of magnitude higher for Co fill interconnects compared to Cu alloy metallurgy. Intrinsic TDDB reliability for Co/low-k ILD meets the expectations and surpasses the capability of Cu/low-k ILD systems with E-field acceleration factor of ~5 cm/MV using E-model fit. Wafer level stress induced voiding reliability on Co shows superior intrinsic properties with respect to Cu.

2:25 PM

6F.8 **Transistor Reliability Characterization and Modeling of the 22FFL FinFET Technology (Late News)**

C.-Y. Su, M. Armstrong, L. Jiang, S. A. Kumar, C. D. Landon, S. Liu, I. Meric, K. W. Park, L. Paulson, K. Phoa, B. Sell, J. Standfest, K. B. Sutaria, J. Wan, D. Young and S. Ramey, Intel Corp.

This paper describes the transistor reliability of Intel's 22FFL FinFET technology, which includes an extensive variety of device offerings to enable high performance and low power design options. Detailed evaluations of BTI, TDDB, self-heating, and HCI are included to demonstrate the impact from the various device's pitch, channel length, and threshold voltage. Process integration details are included to highlight the interaction with reliability. In addition, modeling results are shown to be well matched to silicon.

2A.1 **The Physics of NBTI: What Do We Really Know?,** Jim Stathis, IBM (invited)

Forty years after initially being identified, Negative Bias Temperature Instability in PMOS transistors remains a hotly debated topic, with an ever increasing number of publications treating the topic. Several competing theories have emerged, with varying degrees of success predicting actual behavior. This invited paper will help summarize the key features of each leading theory to help the community integrate the conclusions from the vast number of publications on the topic.

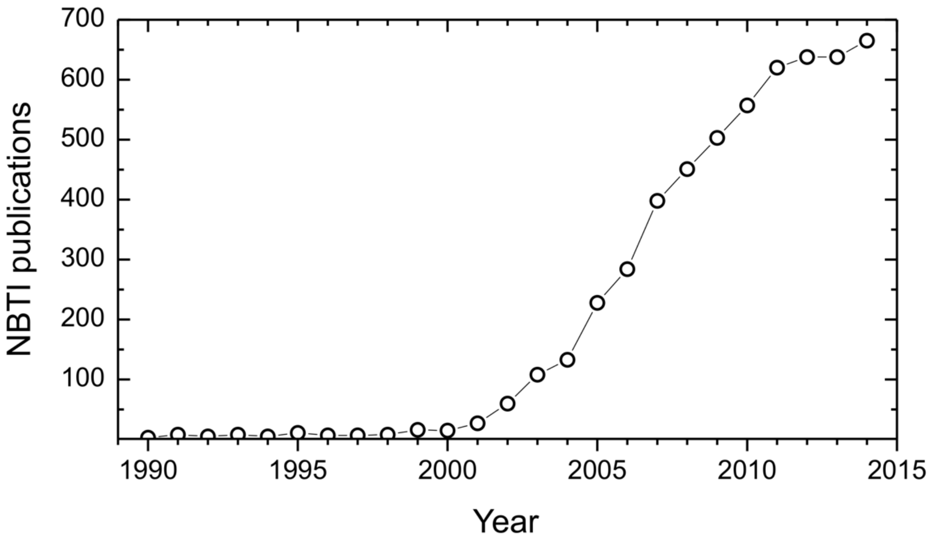
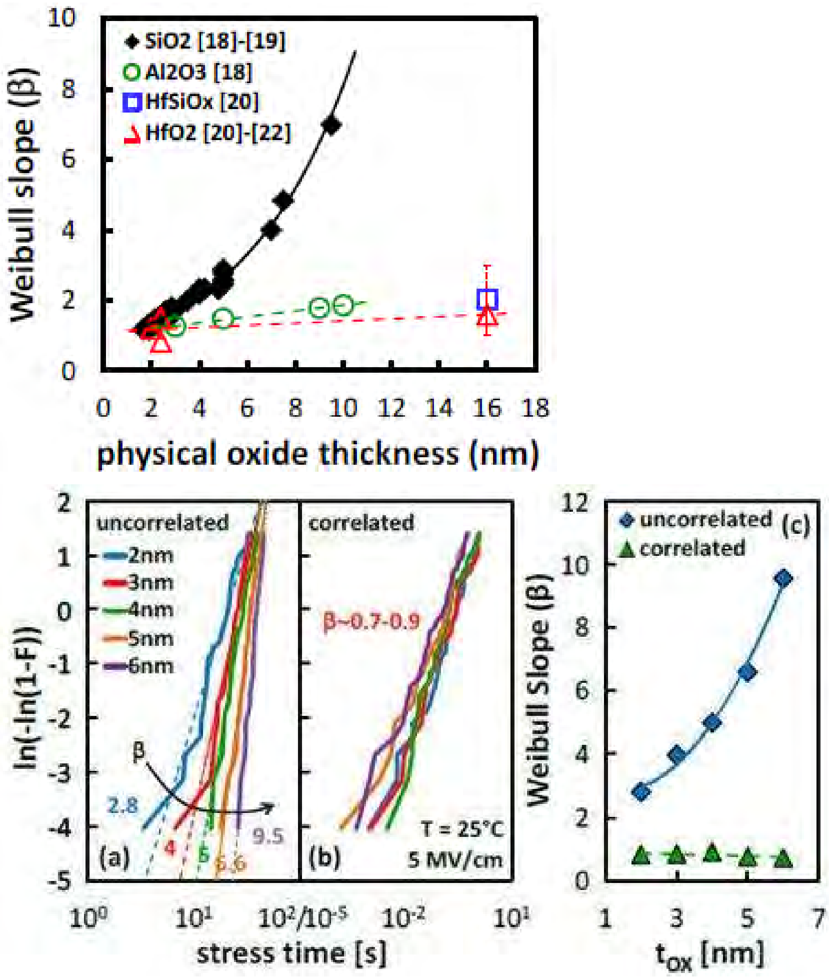


Figure 1. Number of publications annually on NBTI. From Google Scholar (https://scholar.google.com) searches on the phrase “negative bias temperature instability”.

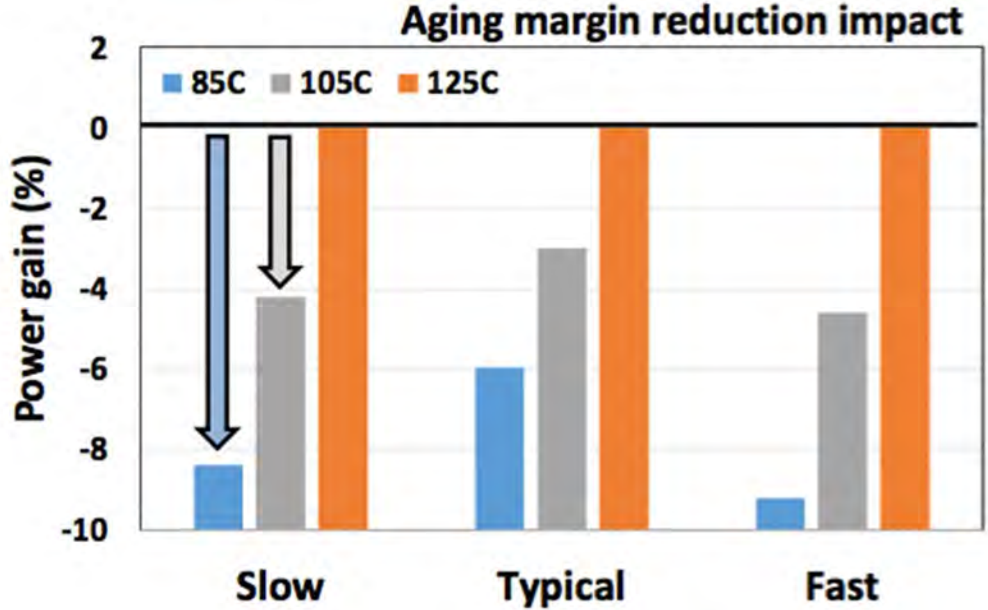
3A.2 **Time-Dependent Dielectric Breakdown Statistics in SiO_2 and HfO_2 Dielectrics: Insights from a Multi-scale Modeling Approach by** A Padovana and L. Larcher, MDLSoft Inc.

The authors attempt to look at the differences in the statistical distribution of TDDB for SiO2 and HfO2 dielectrics under the percolation framework, making use of a multi-scale multiphysics defect simulation platform called GINESTRA®. They highlight the possibility of "defect clustering" around existing oxygen vacancy defects in HfO2, which are not observed in SiO2 and "quantify" the impact of this clustering trend on the TDDB distribution and Weibull Slope scaling relationship with oxide thickness. Their results provide support for the "insensitivity" of Weibull Slope to oxide thickness scaling in high-K dielectrics, as shown by the figure below. These results, if proven experimentally, may fundamentally force us to relook at the percolation model and consider using non-Weibull distributions for lifetime estimation of ultra-thin dielectrics in the future.



3C.1 **Managing Electrical Reliability in Consumer Systems for Improved Energy Efficiency** by Vincent Huard, S. Mhira, A. Barclais, X. Lecocq, F. Raugi, M. Cantournet, and A. Bravaix, STMicroelectronics and ISEN-REER

In many systems there is always a driving force to improve energy efficiency. This paper describes a new method using Static Adaptive Voltage Scaling (S-AVS) at component level to develop electrically robust system while improving energy efficiency. This work paves the way to S-AVS qualification at system level as well as the dynamic modulation of aging margin in the field so to improve even more the energy efficiency. The figure shows the power efficiency improvement observed on the different SoC corners using the combined approach from the paper.



3C.6 Machine-Learned Assessment and Prediction of Robust Solid-State Storage System Reliability Physics by Jay Sarkar, Cory Peterson, Amir Sanayei, Western Digital Corporation

Application of machine learning (ML) to in-field failure prediction, aka prognostics, is developing. This paper from Western Digital (Sarkar et al.) used ML methods to predict near term failure of solid state drives (SSDs). They found that SSDs have signals which enable plausible prognostics. The figure shows they found they could predict with good accuracy impending failure out to around 75 days in the future.

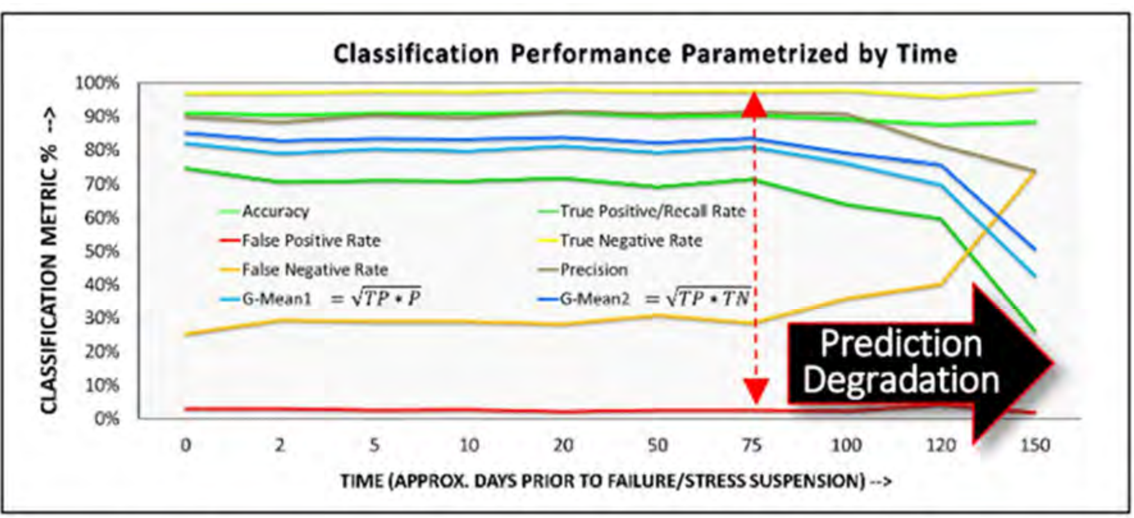
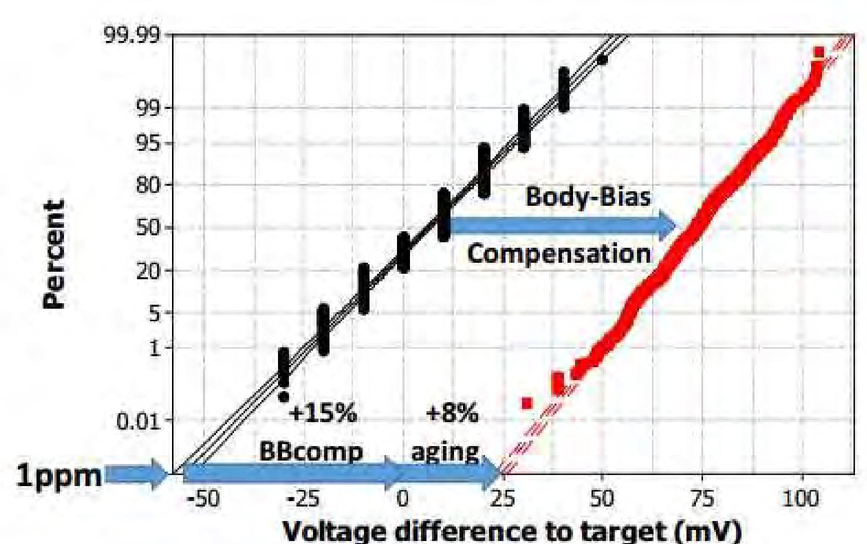


Fig. 5. Predictive efficacy of classification metrics shown as a function of time/state prior to actual failure or stress suspension for survivors.

3D.1 **RESILIENT AUTOMOTIVE PRODUCTS THROUGH PROCESS, TEMPERATURE AND AGING COMPENSATION SCHEMES** by S. Mhira, V. Huard, D. Arora, P. Flatresse and A. Bravaix

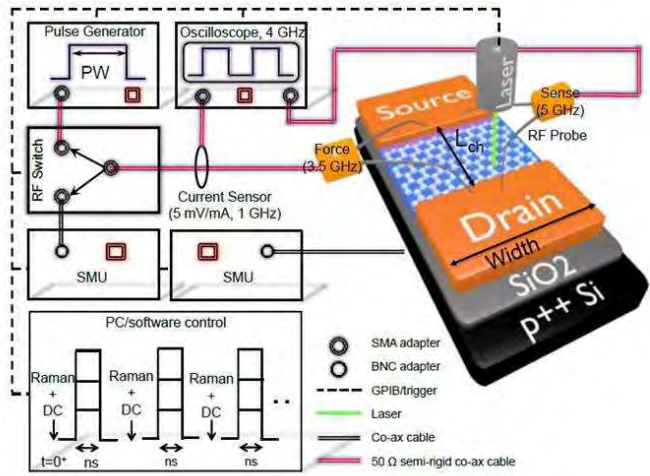
STMicroelectronics, SOITEC, and ISEN-REER, IM2NP

This paper introduces a novel concept through design and product engineering solutions to maximize performance, all while meeting the high reliability standards of the automotive market. The figure below shows results of 23% speed gain while maintaining 1ppm Automotive failure rate.



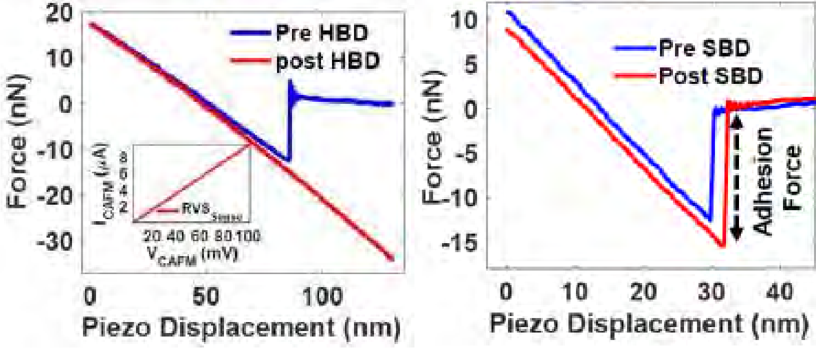
3E.1 Defect-Assisted Safe Operating Area Limits and High Current Failure in Graphene FETs" by Nagothu Karmel Kranthi, Abhishek Mishra, Adil Meersha, Harsha Variar and Mayank Shrivastava, Indian Institute of Science

In this work, a unique measurement setup, involving integration of transmission line pulse tester with Raman spectrometer (see Figure), is used to investigate the pulsed safe operating area (SOA) boundary of graphene field effect transistors (GFETs). Physical insight into various SOA boundaries, i.e., near-electrical, electro-thermal and thermal, is given. Unique defect-assisted degradation in channel and its correlation with the carrier transport as well as failure is revealed, with the help of electrical as well as Raman spectroscopy based investigations during well controlled pulse-stressing of GFETs. The SOA and power to fail dependency on carrier concentration and nature of carrier transport is addressed.



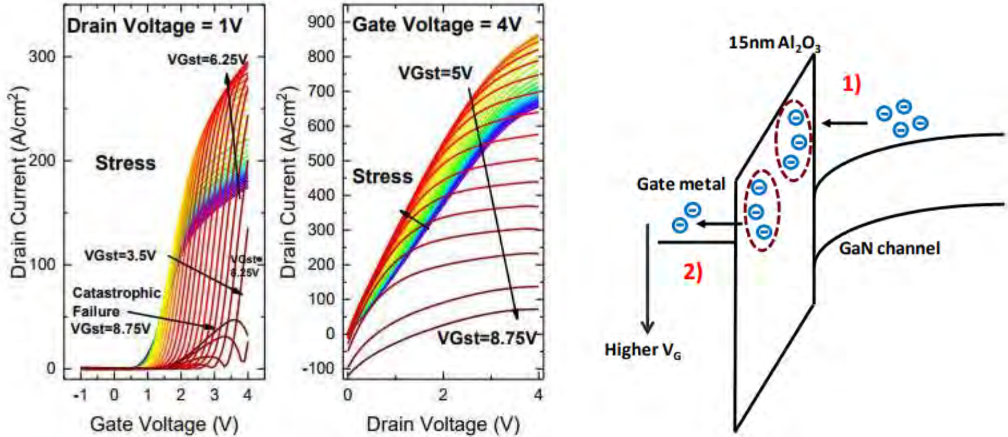
4A.1_ Mechanism of Soft and Hard Breakdown in Hexagonal Boron Nitride 2D Dielectrics by A. Ranjan, N. Raghavan, S.J. O'Shea, S. Mei, M. Bosman, K. Shubhakar, and K. L. Pey, Singapore University of Technology and Design and A*STAR

In this work, authors investigate the physical mechanism of soft and hard breakdown using conductive atomic force microscope (CAFM) as a nanoscale spectroscopy tool on blanket hexagonal boron nitride (h-BN) films. The soft breakdown regime involves percolation path formation with boron vacancies while the hard breakdown regime shows *nano-pitting* that involves removal of h-BN layers and formation of a metallic contact (filament) due to CAFM tip adhesion with the Cu substrate. The physical mechanisms of breakdown in h-BN have not been studied in-depth in the past and this study presents several evidences to understand these phenomena better. The results would also help in probing the similarities and differences in the dielectric breakdown trend for 2D and 3D (bulk) dielectric films such as HfO2 and SiO2. Authors used the adhesion measurement traces after soft and hard breakdown to prove that the mechanisms involved are very different in these two regimes, as shown in the figure below.



4B.1 Degradation of Vertical GaN FETs Under Gate and Drain Stress by M. Ruzzarin, M. Meneghini, C. De Santi, M. Sun, T. Palacios, G. Meneghesso, and E. Zanoni, University of Padova, and MIT

GaN-on-GaN vertical devices have a great potential, for application in the power conversion field. So far, no extensive reliability data has been presented on these devices. This paper reports the first experimental analysis of the degradation of GaN-based VFETs submitted to gate- and drain step-stress. The results allow to identify the main failure mechanisms under gate and drain-step stress.



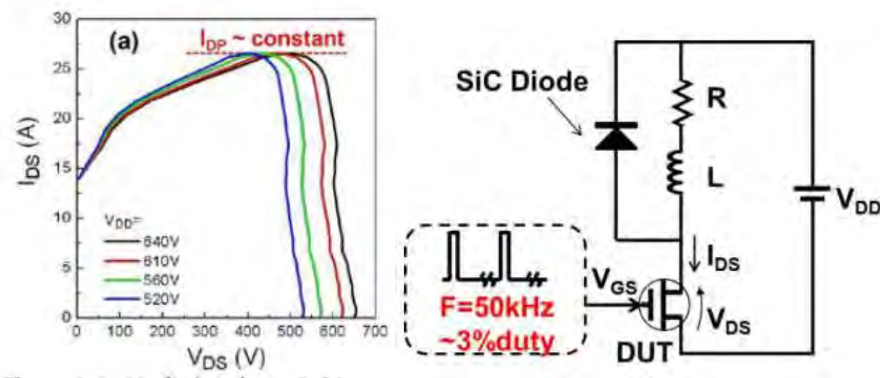
Impact of step-stress on the transfer and output characteristics of vertical GaN MOSFETs, and related (Schematic) model

4C.1 **Scaling Trends and Bias Dependence of the Soft Error Rate of 16 nm and 7 nm FinFET SRAMs** by Balaji Narasimham, Saket Gupta, Dan Reed, J. K. Wang, Nick Hendrickson, Hasan Taufique, Broadcom

This work presents the scaling trends in the alpha and neutron SRAM SER from planar to two FinFET process nodes. While the first process scaling from planar to FinFET resulted in large SER reduction, the subsequent scaling from 16 nm to 7 nm FinFET is shown to follow the bit-cell area reduction. Extensive data collected across a range of supply voltages in planar and FinFET processes show strong exponential bias dependence of SRAM SER for FinFET processes, while for the planar process it follows a linear trend. The results presented in the paper highlight the importance of understanding the SER scaling trends and bias dependence for FinFET-based circuits as well as developing mitigation schemes based on the intended application and operating voltage range.

4.E.2 Lifetime evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under practical switching operations by Ayanori Ikoshi, Masahiro Toki, Hiroto Yamagiwa, Daijiro Arisawa, Masahiro Hikita, Kazuki Suzuki, Manabu Yanagihara, Yasuhiro Uemoto, Kenichiro Tanaka, and Tetsuzo Ueda, Automotive and Industrial Systems Company, Panasonic Corporation

HD-GITs are high-performance normally-off transistors based on gallium nitride. This paper from Panasonic reports one of the first studies on the reliability of HD-GITs in actual practical conditions. The authors performed dynamic high-temperature operating lifetime tests on HD-GITs with varying input voltages, switching current and temperatures. Based on the acceleration factors obtained within this analysis, they evaluated the lifetime of HD-GITs operated in a 3 kW power factor correction (PFC) circuit (24 years).

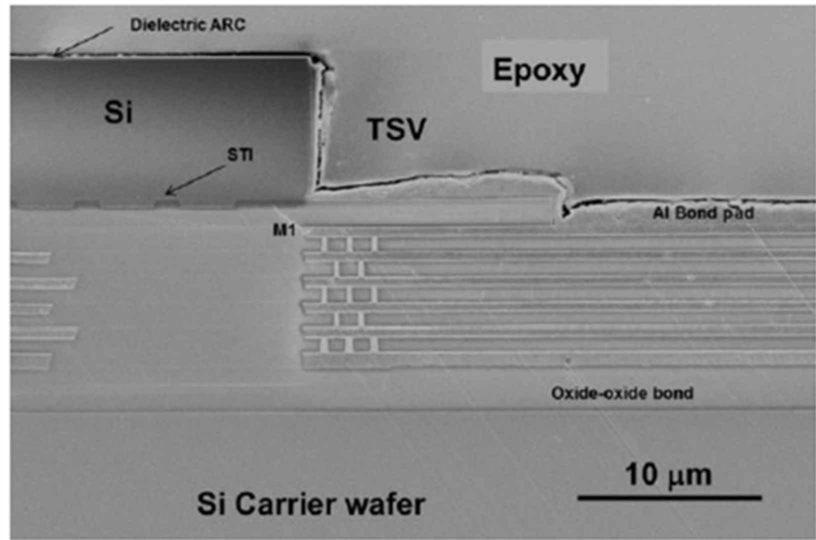


Hard switching ID-VD locus measured on GaN power transistors and related circuit

5.B.6 **Device Reliability for CMOS Image Sensors with Backside TSVs**

by J.P. Gambino, H. Soleimani, I. Rahim, B. Riebeek, L. Sheng,H. Truong, G. Hall, R. Jerome, D. Price,
ON Semiconductor

CMOS sensors with TSV is a fast growing application of 3D integration. This technology enables the fabrication of powerful image sensors that are assembled into the cameras of most portable electronic devices. Owing to their complex integration, potential interactions between the TSV processes and the CMOS image sensor play a key role in the reliability of such devices. This work studies the mechanisms of such interactions and highlights the potential challenges involved in bringing this complex technology to market.



This figure highlights the complex integrational challenges involved in fabricating an advanced imaging sensor with back-side TSV to enable fast connection to a processing chips. The TSV, while enabling the powerful image processing capabilities of the chip, also causes unwanted interaction to the devices. Understanding these perturbations enables more powerful imaging systems that will not fail in the field.

5.C.2 **All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits** by Gyusung Park, Bongjin Kim, Minsu Kim, [*]Vijay Reddy and Chris H. Kim , University of Minnesota, [*]Texas Instruments

The purpose of this work is to understand the impact of device aging on frequency and phase noise degradation of an All-Digital Phase Locked Loop (ADPLL) circuit. An on chip phase noise and Digitally Controlled Oscillator (DCO) monitor provides a fast and accurate in situ measurement and communication to the external world through a cheap and simple serial interface. This eliminates the need of expensive and complex external test setup like high frequency sampling scope or a spectrum analyzer, that would be prohibitive for some low cost test applications or environmental conditions (eg. Space applications)

Despite the fact that the on-chip monitor is based on standard digital circuits such as counters, flip-flops, and a variable delay line, it achieves a frequency degradation measurement accuracy of 0.01% within a few microseconds.

Such measurements provide the magnitude of required up-front design margin for proper end of life operation without over-designing. They also show that the natural recovery mechanism is not adequate to resolve this degradation issue and additional anneal will be needed for full recovery.

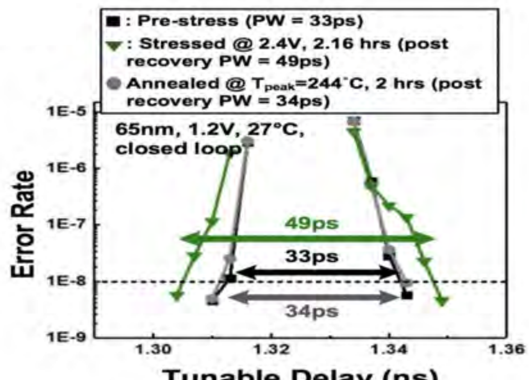


Fig. 11. Measured closed-loop phase window curves for pre-stress, stressed, and annealed DCOs.

5.C.3 **Design of Aging Aware 5 Gbps LVDS Transmitter for Automotive Applications** by Srikanth jagannathan, Kumar Abhishek, Tarun Goyal, Nihaar Mahatme, Gayathri Bhagavatheeswaran and Ender Yilmaz, NXP Semiconductors

This work describes the effect of circuit aging on 5 Gbps Low Voltage Differential Signaling (LVDS) Transmitter (TX) used in automotive high speed communication. Aging simulations are used to investigate the sensitivities of various sub-blocks of the TX designed in 16nm FinFet technology. Mitigation techniques using on-chip dynamic aging adaptive capability with jitter and duty-cycle correction circuity is developed to recover critical TX performance within its specification limits. Measured Si results confirms the efficacy of the mitigation techniques, with TX capable of restoring its aging induced degradation in performance to <5% from its pre-aging values.

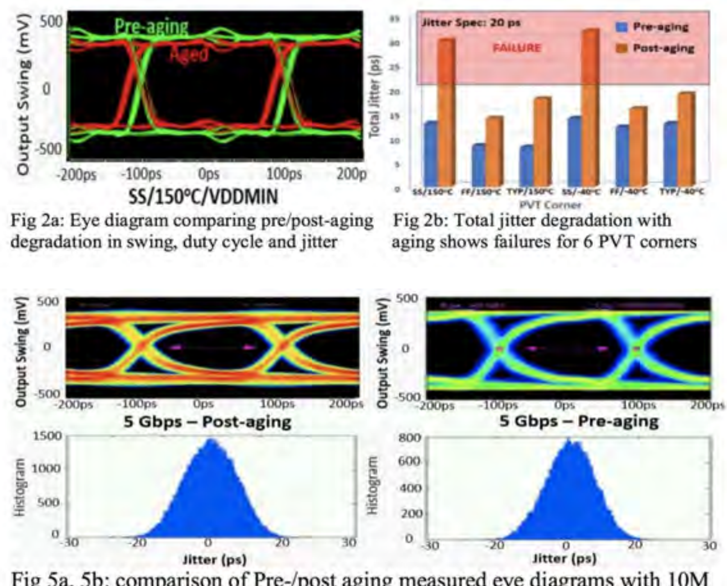


Fig 2a: Eye diagram comparing pre/post-aging degradation in swing, duty cycle and jitter

Fig 2b: Total jitter degradation with aging shows failures for 6 PVT corners

Fig 5a, 5b: comparison of Pre-/post aging measured eye diagrams with 10M samples of 5Gbps random data and total jitter at SS/VDDMIN/150 °C.

6B.1 **Solving Critical Issues in 10nm Technology using Innovative Laser-based Fault Isolation and DFT Diagnosis Techniques** by Lesly Endrinal , Rakesh Kinger, Lavakumar Ranganathan, Amit Sheth, Qualcomm Technologies, Inc.

The challenges of completing failure analysis on first silicon for the 10nm technology node are described in this paper by Qualcomm (Endrinal et al.) along with a solution for a particularly difficult, high impact, case. As dimensions shrink the ability of optical probe imaging has become severely resolution limited. Electrical fault isolation becomes more dependent upon DFT (Design For Testability) diagnosis, which also has practical limitations. Here the authors have written new test patterns, overcoming the limitations in imaging resolution and diagnosis, to provide clear fault isolation. Their innovative problem solving ultimately led to an image of the defect and clear direction for process improvement.

6.C.4 **Mechanical and chemical adhesion at the encapsulant interfaces during the lamination of photovoltaic modules** by Philippe Nivelle, Tom Borgers, Eszter Vöröshazi, Jef Poortmans, Jan D'Haen, Ward De Ceuninck and Michaël Daenen, University Hasselt

This paper investigates the influence of the flux use in the soldering on the adhesion strength of the encapsulation polymer to the metallization/interconnection of a photovoltaic module as it can have a major effect on the long term reliability. It shows that the influence of flux is predominantly determined by the encapsulant type. The differences measured in adhesion strength could be correlated to a difference in macro-scale roughness at the interface and in the quantity of solder particles present.

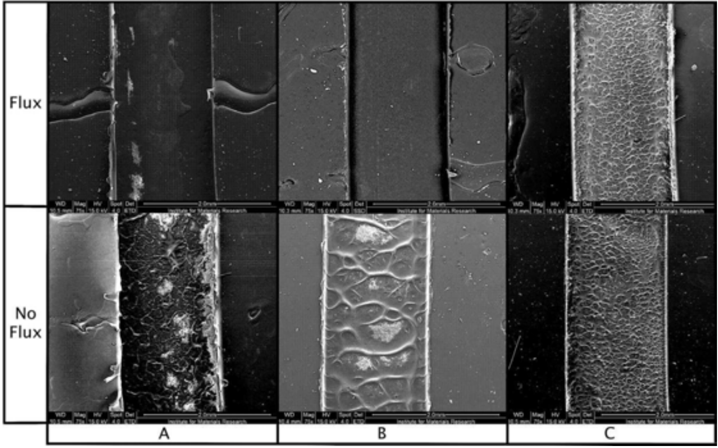


Figure 3: SEM-ETD images from the adhesion interface on the encapsulant providing a visual indication on the quantity of metallic solder particles (white) on the polymer surface.

6D.5 **Reliability Benefits of a Metallic Liner in Confined PCM** by

W. Kim, Y. Xie, Y. Kim, T. Masuda, S. Kim, R. Bruce, F. Carta, G. Fraczak, A. Ray, K. Suu, C. Lam, M. BrightSky, J. J. Cha and Y. Zhu
IBM, ULVAC Inc., and Yale University

Resistance drift is one major problem in PCM technology, leading to retention errors. The paper studies the relation between resistance drift and resistivity of the metallic liner in confined PCM cells, resulting in a choice of the liner which allows to achieve outstanding resistance drift. This is ascribed to the elimination of the generated voids during programming (see Figure), and results in a confined PCM cell with a high potential to be used as a high-density multi-level cell.

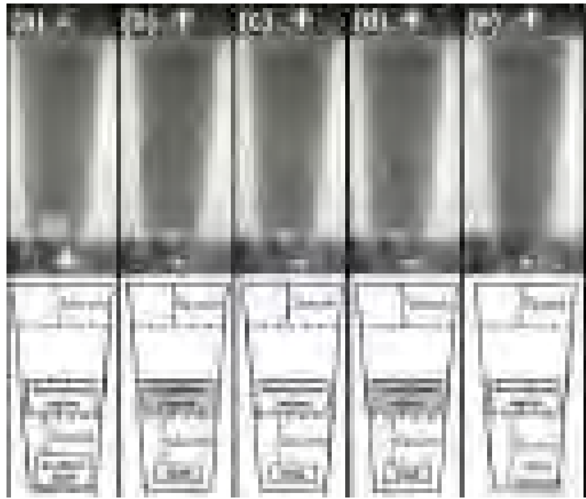
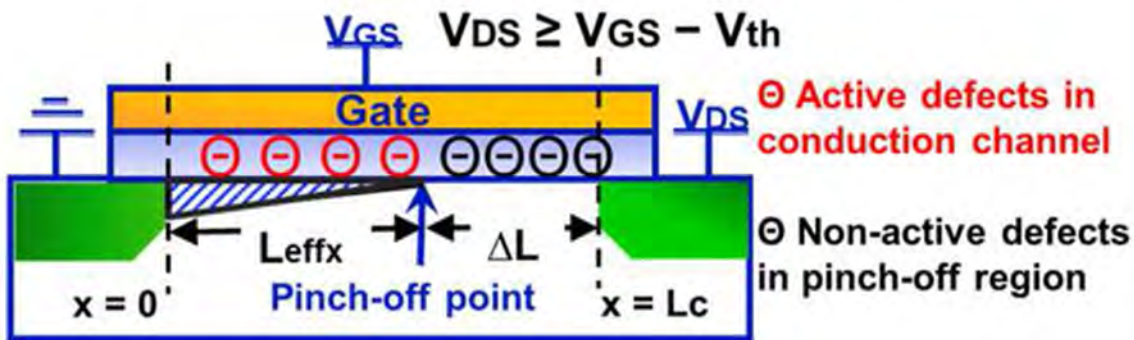


Fig.9: (a) Schematic figures of the confined PCM cells with liner A describe the switching region and elemental segregation in the PCM cell during the consecutive programming. (a) A void near BE was created by reverse-bias pulse. (b) and (d) indicate that switching occurs near center of the pore. The generated void was completely healed in (e).

6E.1 ***Lateral Profiling of HCI Induced Damage in Ultra-Scaled FinFET Devices with Id-Vd Characteristics****, Miaomiao Wang, Richard Southwick, James Stathis and Kangguo Cheng, IBM*

This work presents a novel technique for characterizing the lateral trap distribution along the MOSFET channel of hot-carrier created defects. In the past, this kind of characterization entailed extensive computer simulation or complicated analytical modeling that often had limited accuracy. This method utilizes a modified Id-Vd based lateral profiling technique which is capable of extracting the lateral distribution of hot-carrier created defects in ultra-scaled FinFET devices with improved accuracy.



6.F.4 **Reliability Studies of a 10nm High-performance and Low power CMOS Technology Featuring 3rd Generation FinFET and 5th Generation HK/MG**, Anisur Rahman, Javier Dacuna Santos, Pinakpani Nayak, Gerald S Leatherman and Stephen M Ramey, Intel Corporation

Reliability of a state-of the art 10nm FinFET technology. This paper from Intel (Rahman et al.) presents the new architectural features introduced to maximize the density scaling at 10nm (see Fig. 2) and investigates their effect on device reliability. The paper highlights the performance-reliability co-optimization required to develop a successful technology that considers the complex process reliability interactions observed in these ultra-scaled devices. One example is showns in Figure 9 with illustrates an improvement in the 10nm FinFET TDDB breakdown reliability as compared to 14nm generation arising from this performance-reliability co-optimization.

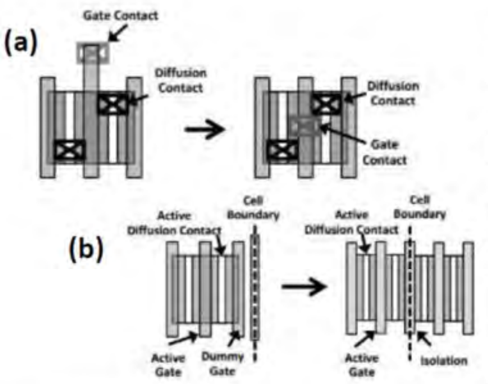


Figure 2 Two new architectural features helped to maximize density scaling at 10nm. (a) Gate contact over active area—eliminating need to extend it over isolation. (b) Minimum isolation at cell boundary, eliminating need for dummy gate.

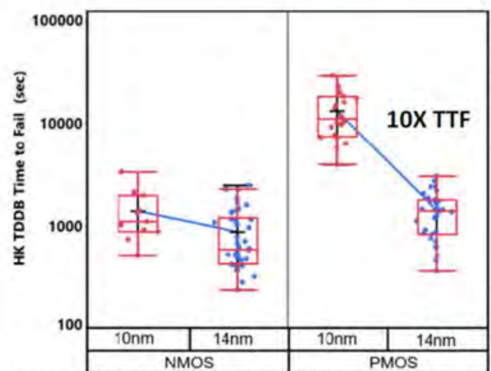


Figure 9 TDDB time-to-fail (TTF) compared between 14nm (4th Gen) and 10nm (5th Gen) HK at matched stress condition and test-structure area. 5th Gen PMOS HK shows substantial intrinsic GOX reliability improvements. NMOS TDDB is matched or better.

TM1.1

Chetan Prasad, Intel Corp.

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TM1.2
Tibor Grasser, TU Wien

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TM1.3

Mario Lanza, Soochow University

Conductive Atomic Force Microscopy and its Use in Nanoelectronic Device Reliability

http://lanzalab.com/profile/
https://www.linkedin.com/in/mariolan/

Mario Lanza is Full Professor at Soochow University. Dr. Lanza got his PhD in Electronics in 2010 at Universitat Autonoma de Barcelona, and two postdocs, one at Peking University (2010-2011) and another one at Stanford University (2012-2013). He has published over 80 research papers (including Science), edited the first book on CAFM for Wiley-VCH, and registered four patents (one granted with 1M$). He has received several prestigious awards, including the Young 1000 Talent Award of China, the Elsevier Young Investigator Award, and the Marie Curie postdoctoral fellowship. He is member of the advisory board of the journals Advanced Electronic Materials, Nature Scientific Reports and Nanotechnology, as well as member of the technical committee of several IEEE conferences. His research interests focus on the improvement of electronic devices using two dimensional materials, with special emphasis on layered dielectrics for memory devices.

Conductive atomic force microscopy (CAFM) has become one of the most useful techniques to analyze the electronic properties of many electronic materials and devices. This tutorial will show the capabilities of the CAFM to study many crucial nanoscale phenomena of thin dielectrics, such as the effect of thermal annealing, polycrystallization, thickness fluctuations, local defects, charge trapping and de-trapping, stress-induced leakage current, negative bias temperature instability, dielectric breakdown and resistive switching. The tutorial will also describe how to apply combined electronic and mechanical stresses, which may be crucial for the study of future flexible devices. Data from HfO_2, Al_2O_3, and SiO_2 based devices will be mostly presented, although information about novel two dimensional dielectrics (i.e. hexagonal boron nitride) will be also disclosed. Modifications of standard CAFM setups to achieve higher performances will be also discussed. In the final part, indications about how to perform reliable experiments and how to avoid wrong CAFM data interpretations will be presented.

TM2.1
Yiming Huai, Avalanche Technology

STT-MRAM: Past History, Current Status and Future Perspectives

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Dr. Yiming Huai serves as VP of Technology and Foundry Partnership at Avalanche Technology, a front runner to commercialize STT MRAM technology. He leads Avalanche STT MRAM product development and manufacturing in collaboration with top-tier foundries and also plays a key role in business development.

Dr. Huai is a pioneer on STT MRAM and was the first to demonstrate spin transfer switching in magnetic tunnel junctions. Dr. Huai received his BS degree in theoretical physics from Shanghai University of Science and Technology and his M.S. and Ph.D. in Physics from the University of Montreal. He worked as a Staff Scientist at the Lawrence Livermore National Laboratory and as a Post-Doctoral Fellow at the National Research Council in Ottawa, Canada. From 1996 to 2001, Dr. Huai served as Sr. Director of Thin Film Manufacturing at Read-Rite Corporation (now Western Digital), where he led the development and volume production of industry leading GMR heads for hard disk drives. In 2002, Dr. Huai cofounded Grandis, Inc., a pioneer in STT MRAM technology and served as CTO, VP of Engineering and board member. While at Grandis, Dr. Huai successfully raised more than $25M in private and government (DARPA STT MRAM and NIST) funding and led STT MRAM joint development with leading semiconductor companies (Renesas and Hynix). Grandis was acquired by Samsung in 2011. He has published more than 150 papers in scientific journals, and holds more than 160 U.S. patents. He has given more than 60 invited talks on STT-MRAM technology and has served as Conference Chairman and Organizer for major international magnetic and semiconductor conferences and workshops. Dr. Huai was an Editorial Board member of Spin Journal. In 1996, Dr. Huai received the prestigious R&D 100 Award for his innovative work on Ultra-High Density Magnetic Sensors.

Spin transfer torque magnetic RAM (STT-MRAM) is the most promising new nonvolatile memory technology owing to its superior performance of unlimited endurance (>1016) and fast switching speed (<10 ns). While Standalone STT-MRAM products are rapidly entering market with increasing varieties of applications, embedded STT MRAM products are on the cusp of mass production with larger market impact. This tutorial will provide an introduction to STT-MRAM from past STT-MRAM development history, including spin transfer torque switching and magnetic tunnel junction basics, to current STT-MRAM product development status with recent landscape in semiconductor industry, to STT-MRAM applications, markets and future perspectives.

TM2.2

Makoto Fujiwara, Toshiba Corp.

3D Flash Memories: Overview of Cell Structures, Operations and Reliability

Makoto Fujiwara received the B.S. degree in electrical engineering from North Carolina State University, Raleigh, NC in 1992 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA in 1994. He was a research and teaching assistant at Stanford University in 1995. He joined Toshiba Corporation in 1996 where he was responsible for device design and process integration of both bulk and SOI MOSFETs, device/process modeling for TCAD and development of advanced gate stack. From 2005 to 2006, he was a visiting researcher at Stanford University where he worked on physics and modeling of high mobility channel devices. From 2008 to 2011, he was with IBM-Toshiba System LSI Development Alliance in Albany, NY where he conducted development and evaluation of low power CMOS technologies. Currently, he is leading cell device design and characterization for 3D flash memories.

A growth of the memory storage capacity without increasing the area occupation is constantly demanded by the market. The transition from two-dimensional (2D) to three-dimensional (3D) architectures has been the most viable solution to overcome performance and reliability issues from capacity limitations.

In this tutorial, the main reliability mechanisms affecting 3D flash memories will be addressed, providing a comprehensive overview of 3D charge-trap cells and the underlying physics of operation and reliability. Starting from an analysis of basic cell structures and operations, physical mechanisms impacting the reliability of 3D flash memories are reported.

TM2.3

Daeyong Shim, SKHynix

HBM Design, Test & Reliability Challenges for AI Applications

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Daeyong Shim, VP of SKHynix, received his B.S. degree in Electronic Materials Engineering from KAIST (Korea Advanced Institute of Science and Technology) in 1993, the M.S. degree in Inorganic Materials Engineering from Seoul National University, Seoul, Korea in 1995, and the Ph.D. degree in Electrical Engineering from Seoul National University, Seoul, Korea in 2013. He joined Hyundai Electronics Co. Ltd. (now SK Hynix Semiconductor), Icheon, Korea, as a Research Engineer where he has been working more than 20 years experiences as a DRAM design, test and device engineer worked on processes from 0.32 um to 1y nm. From2016 he is now in charge of HBM product development. His research interests include design of high-bandwidth low-power memory and system applications. He was also a panel speaker in ASSCC 2017.

This tutorial covers recent technology trends of High Bandwidth Memory (HBM)design, test & reliability issues. Current HBM has been developed by dynamic random access memory (DRAM) technology that uses through-silicon vias (TSVs) to interconnect stacked DRAM Core(Cell) die and base die(Logic). After the first successful launching of HBM1 based AMD's Fiji processor which comprises a graphics processor unit (GPU) and four HBM cubes using 2.5D fine-pitch silicon interposer technology, HBM is being used widespreadly in high-performance computing (HPC), data center and network applications.

This presentation introduces the challenges for system integrators to adopt HBM as a high-bandwidth low-power memory solution with small form-factor. Main topics include the reliability issues in HBM 2.5D solution related with TSVs, micro-bumps, fine-pitch silicon interposer and post package DRAM cell repair scheme between HBM and SOC. The thermal &power distribution network (PDN) related HBM design issues and key approaches will be also discussed. Finally, the next generation HBM3 solution will be also briefly introduced.

TM3.1

Sameer Pendharkar, Texas Instruments

Ultra High Voltage LDMOS Device and Technology

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Sameer Pendharkar is a TI Fellow and Manager of the High Voltage silicon and wide bandgap technology development group at Texas Instruments. He is the author or co-author of more than 75 research papers and has more than 120 issued patents in the area of power and high voltage semiconductors. He has given invited talks and short courses on high voltage, ESD, reliability and power device technology at numerous conferences like IEDM, ISPSD,BCTM, ISPS and IRPS and has served on power and WBG technical sub-committees of several conferences.

The increased focus on green energy applications drives the need for ultra high voltage Bipolar-CMOS-DMOS technology (at least 700V) targeting applications like AC-DC adaptors and LED lighting. While the low and mid-voltage components in such a technology allow for logic and analog functional integration the high voltage LDMOS is typically the workhorse device that interfaces with the outside world. Depending on the targeted application, the HV LDMOS needs to either block the voltage with fast switching capability or need to have low resistance to minimize losses. This tutorial will provide an introduction to UHV BCD technologies with particular emphasis on LDMOS device design evolution and reliability and robustness characterization.

TM3.2

Alberto Castellazzi, University of Nottingham

SiC Power MOSFETs: Application Benefits and Technology Validations Needs

Alberto Castellazzi is an Associate Professor of Power Electronics at the University of Nottingham, UK. He has been active in power electronics R&D for over 15 years, collaborating with some of the main industrial and academic institutes worldwide. His research interests are power devices and the enabling technologies of power electronics. He has published over 170 papers in peer reviewed journals and conference proceedings and is a member of the Technical Program Committee of the IRPS, ISPSD, ESREF, ESTC and IPEC conferences.

This talk will review the rapid development of SiC MOSFET technology over the past 5 to 10 years. It will discuss its application-related interest and its establishment as the preferred device type against alternative normally-off solutions. It will review qualification needs, including the development of bespoke validation methodologies, and offer insight into present technology maturity and ongoing progress.

The presentation will conclude by addressing concurrent technology development needs enabling full exploitation of the device characteristics.

TM3.3

Kenichiro Tanaka, Panasonic Corp.

Validating the Robustness of GaN Power Transistors

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Kenichiro Tanaka received the bachelor, the master and the doctor degree of Engineering from the University of Tokyo in 1997, 1999, and 2003, respectively. In his doctoral thesis, he had investigated the optical properties of lead-iodide-based inorganic-organic perovskite materials which have been gaining attention in recent years due to their outstanding properties as a solar cell. After he had investigated as a Special Postdoctoral Researcher in RIKEN institute, Japan, he joined Semiconductor Device Research Center, Matsushita Electronics Corporation (currently Panasonic), Kyoto, Japan in 2007. Since then, he has been engaging in the development of GaN power transistors applicable for high-frequency switching applications. He started his career with the development of crystal growth of GaN on Si substrate, and he has been involving the device design, manufacturing, reliability, and simulation study. He had involved in MHz high-frequency power converter design employing Panasonic's GaN transistors in CPES, Virginia Tech, in the USA from 2015 to 2017. He authored and coauthored 24 technical papers. He is a member of Japanese Journal of Applied Physics and also a sub-committee member of International Reliability Physics Symposium (IRPS) in 2017 and 2018.

In recent years, as GaN power transistors come into widespread use as the promising switches for power converter applications, it is all the more important and inevitable to guarantee their reliability. Firstly, in this tutorial, we will review how we strengthen the robustness of GaN power transistors. We have been incorporating a bunch of technologies to strengthen the robustness of GaN power transistors, which will be briefly discussed. In particular we will introduce a Hybrid-Drain-embedded Gate Injection Transistor, the structure of which is quite effective to ensure the GaN reliability to the commercially-applicable level.

Secondly, we will discuss how we evaluate the robustness of GaN power transistors. The robustness of GaN power transistors should be examined under switching operations as well as under the conventional DC tests standardized for Si power transistors, because severe switching event induces the so-called current collapse, which may end up in the device degradation. The magnitude of current collapse depends strongly on the trajectory of IDS-VDS during the switching event, so is the reliability. Therefore, the concept of Switching Safe Operating Area (SSOA) is proposed recently to define the IDS-VDS limit inside which the device can be switched with safety. In this tutorial, we exemplify the SSOA for our Hybrid-Drain-embedded Gate Injection Transistors (HD-GIT) under the switching for a short period of time. Furthermore, we extract the SSOA for HD-GIT under the switching for much longer period of time, based on the lifetime investigation under accelerated switching condition. We hope that the methodology presented here is utilized to guarantee the robustness of GaN power transistors and it further accelerate the more widespread use of GaN power transistors.

TS1.1
Chris Henderson, Semitracks Inc.

Semiconductor Reliability and Product Qualification

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Christopher Henderson received his B.S. in Physics from the New Mexico Institute of Mining and Technology and his M.S.E.E. from the University of New Mexico. Chris is the President and one of the founders of Semitracks Inc., a United States-based company that provides education and semiconductor training to the electronics industry. From 1988 to 2004, Chris worked at Sandia National Laboratories, where he was a Principal Member of Technical Staff in the Failure Analysis Department and Microsystems Partnerships Department. His job responsibilities have included failure and yield analysis of components fabricated at Sandia's Microelectronics Development Laboratory, research into the electrical behavior of defects, and consulting on microelectronics issues for the DoD. He has published over 25 papers at various conferences in semiconductor processing, reliability, failure analysis, and test. He has received two R&D 100 awards and two best paper awards. Prior to working at Sandia, Chris worked for Honeywell, BF Goodrich Aerospace, and Intel. Chris is a Senior Member of IEEE and EDFAS (the Electron Device Failure Analysis Society). He was the General Chair of the International Symposium for Testing and Failure Analysis (ISTFA) in 2007 and the General Chair of the IEEE Reliability Physics Symposium in 2016. At Semitracks, Chris teaches courses on failure and yield analysis, semiconductor reliability, and other aspects of semiconductor technology.

Reliability Engineering is an increasingly important discipline within the semiconductor industry. Today, we implement electronics in more applications that demand high levels of reliability, such as automotive, defense, and industrial. In the future, even our smart phones will require higher levels of reliability, as they become part of the electronics used for medical purposes. Reliability engineering encompasses a number of activities, including experimental testing to model existing failure mechanisms and uncover new ones, mathematical calculations to assess the reliability of our semiconductor devices in various use conditions and applications, product qualification to assess the fitness of our devices for a customer's use, and consultation on design issues, to make our devices more reliable. We will provide an overview of the various activities and introduce important topics and concepts for the new reliability, quality, or product engineer to understand.

TS1.2
Barry Linder, IBM

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This tutorial will introduce a variety of topics related to the Front End of the Line (FEOL) reliability. The entire landscape of FEOL reliability will be covered including the origins of Bias Temperature Instability (xBTI), Time Dependent Dielectric Breakdown (TDDB), and Hot Carrier Instability (HCI). The tutorial will also touch on testing approaches for reliability qualification, process solutions to FEOL reliability, and the effect of future scaling on FEOL reliability.

Barry P. Linder received his B.S. from Pennsylvania State University in 1993, and an M.S and Ph.D. in Electrical Engineering from the University of California at Berkeley in 1999. His doctoral thesis dealt with plasma processing, plasma implantation, and plasma charging damage. From 1999-2016, Dr. Linder was employed as a Research Staff Member at the IBM T. J. Watson Research Center, Yorktown Heights, NY. Initially his work centered on the breakdown of ultra-thin gate oxides, including the statistics of breakdown phenomenon, post-breakdown conduction mechanisms, and the interaction between oxide breakdown and circuit operation. This work formed the basis for the paper that received an "Outstanding Paper Award" at the 2003 International Reliability Physics Symposium.

After 2003, his focus switched to electrical characterization and integration of metal gates and high-k materials. He has studied the full array of advanced gate stack materials including their integration and their effect on effective work function, channel mobility, gate leakage, and inversion layer thickness scaling. He specialized on the interaction between cap layers, interface layers, and metal gate composition on the final electrical properties of the gate stack. As manufacturing of high-k/metal gate stacks approached, he concentrated on all reliability aspects with emphasis on dielectric breakdown and bias temperature instability. More recently, he focused on the effect of transistor degradation on circuit functionality and performance, optimizing the trade-off of system performance with system reliability.

Since 2016, Barry has managed the Technology Reliability and Quality group for the IBM Systems Group. In this role he is responsible for the end to end technology qualification for from technology specification definitions to accelerated life testing.

TS1.3
Baozhen Li, IBM Systems

Back-End of Line (BEOL) Reliability

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Baozhen Li has a Ph.D. degree in Materials Science and Engineering from the University of Notre Dame. He is currently a Senior Technical Staff Member at IBM Systems, focusing on reliability and product/technology interactions, working between foundry and chip design and product integration. Prior to IBM's divesture of its semiconductor manufacturing in 2015, he was a leading engineer for BEOL reliability to support technology development, manufacturing and chip design. He served as committee chairs of BEOL Reliability & Low K TDDB and gave two tutorials previously for IRPS.

BEOL reliability has been an important part of semiconductor technology development and qualification. It focuses on the integrity of the on-chip interconnect stacks. The wear-out failure mechanisms include electromigration (EM), stress migration/voiding (SM/SV), thermal mechanical stability, low K dielectric breakdown (TDDB) and chip/package interactions (CPI). Following the introduction of physical and statistical fundamentals of these mechanisms, this tutorial will provide examples of reliability analysis at chip and system level. Discussions will also be made on the challenges to the BEOL reliability with the new technology scaling, material set and integration schemes.

TS1.4

Scott Pozder, GLOBALFOUNDRIES

An Overview of Chip to Package Interaction and its Impact on Reliability

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Scott Pozder is a Member of Technical Staff at GLOBALFOUNDRIES. He received a B.S. in Physics from Montana State University and a M.S. in Material Science from Colorado School of Mines. Prior to joining GLOBALFOUNDRIES he was at Motorola which then became Freescale working on CPI, 3D wafer and die stacking in addition to MEMS process integration. After Freescale to development projects he participated in development projects for memristors and wafer bonded sensors for life sciences applications. At GLOBALFOUNDRIES his focus area is the CPI reliability of advanced node semiconductor technologies. He is an author or coauthor on over 14 publications in the areas of 3D IC, Advanced Packaging and Cu BEOL and is an inventor on 19 U.S. Patents.

In the early 2000's CPI became a major reliability topic because of the susceptibility for low-k and ultra-low-k dielectric BEOL materials to fail during chip attach to package. With over a decade of interconnect and package material improvements CPI remains a reliability challenge. This is due to factors beyond the continued use of low k films as interconnect dielectric material. These factors include: the increase in device density through scaling and from 2.5/3D integration, decreasing bump size or moving to Cu pillars to enable higher IO counts, increasing package to chip area ratios to accommodate the higher IO counts, the introduction of thinner coreless packages, thinner chips and the evolution package materials. These and other aspects of CPI and their impact on reliability will be covered in this tutorial.

TS2.1
Norbert Seifert, Intel Corporation

Soft Error Fundamentals

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Norbert Seifert is a Principle Engineer in the Technology and Manufacturing Group at Intel Corporation in Hillsboro, Oregon, where he currently manages the Soft Error Rate (SER) Team responsible for test chip design, planning and conducting radiation test campaigns, modeling of radiation effects, and interacting with internal and external customers on radiation effects topics.

Dr. Seifert holds a Ph.D. in Physics (Vienna University of Technology) and has over 20 years of experience in the semiconductor industry focusing on the interaction of radiation with matter at various levels throughout his career. He has authored or co-authored over 60 conference and journal publications, written one book on chip-level modeling strategies for soft errors and one book chapter on "Soft Error Resilient System Design through Error Correction". He has given several tutorials, invited talks, and keynotes on radiation effects at conferences and workshops in recent years. He holds five issued patents. In 2014 Dr. Seifert was awarded the Intel Achievement award (Intel's Highest Award) for his radiation effects work. Dr. Seifert actively participated in the creation of several international industry standards on soft errors, such as JEDEC JESD89A, and is currently a member of the JESD89 Task Group working on the JESD89A revision.

Despite significant progress made in recent years, in particular with the introduction of FinFET transistors into the high volume manufacturing market, radiation-induced soft error reliability remains one of the most important fundamental issues in silicon technology. This tutorial will provide an introduction into all key topics to get you prepared for embarking into soft errors and for quickly becoming a productive contributor. Covered topics include: SE mechanism overview, testing for SE, modeling, trends and mitigation.

TS2.2
Nathan D. Jack, Intel Corp.

Introduction to ESD and Latchup Design and Test Methods

Nathan Jack received a Ph.D. in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, in 2012. Since 2012 he has been with Intel Corp. in Oregon as an ESD/Latchup Reliability Engineer. Dr. Jack was the recipient of the Best Poster Award from IRPS, the Best Student Paper Award from the EOS/ESD Symposium and is a two-time recipient of the Outstanding Paper Award from the EOS/ESD Symposium. He has served for the past five years on the technical program and steering committees for the ESD Symposium, International ESD Workshop, and IRPS. He is also an active member of the ESDA/JEDEC CDM Joint Working Group.

The challenges (and opportunities!) facing the ESD and latchup engineer have never been greater. While technology scaling and increasing data rates shrink the ESD and latchup design space, many of the real-world causes of ESD and latchup do not scale. This tutorial is designed as an introduction for those new to or unfamiliar with ESD and latchup. An overview of the real-world events that can cause ESD and latchup damage to ICs as well as the standardized test methods for approximating these stresses (CDM, HBM, system-level ESD, and latchup testing) will be given. On-chip protection and design practices will be reviewed, and examples of failure mechanisms will be given. The tutorial will also touch briefly on the need for improved ESD test standards and factory control to meet the demands of future technology.

TS2.3

Davide Appello, STMicroelectronics
Oscar Ballan, Xilinx

Testing of Automotive IC's: Introduction and Advances

Davide Appello holds a degree in Electronics Engineering from the Universita' di Pavia. He is with STMicroelectronics since 1994 where he is concerned with testability and testing and is currently product engineering director for the automotive digital products. Davide authored and co-authored 60+ papers published at conferences and on journals. He is active within TTTC and TTEP groups of IEEE.

Oscar Ballan holds a degree in Electronics Engineering from the University of Padova and a Masters in Business Administration from Hult International Business School. With 20+ years of experience in the Semiconductor industry he has been working on Functional Safety for integrated circuits since 2008 leading various assessments for different silicon vendors. He is author and co-author of various publications related to fault grading of hardware and software safety mechanisms and fault injection on integrated circuits.

"Electronics content in the car is constantly growing. On top of traditional applications for engine control, transmission, braking/steering, passive safety, body and dashboard also multimedia, advanced driver assistance and car2Xsegments are rapidly growing. The stability and extended duration in manufacturing of these components makes them very attractive for the industry. Extreme product quality achieved with controlled cost is the key challenge. The proposed tutorial covers a broad range of topics which are defining the testability, testing and manufacturing requirements of automotive products, keeping in mind their possible utilization for extreme safety-sensible applications like autonomous driving. Advanced topics like testing of safety critical and secure devices are proposed beside more traditional topics like testability, test development, qualification, industrialization, burn-in and manufacturing. Relevant industrial cases will be proposed to participants."

TS2.4
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Amit Marathe earned his M.S. and Ph.D. in Materials Science and Engineering from the University of California, Berkeley in May 1991 and August 1996 respectively. Amit joined AMD in Sunnyvale CA soon after graduation and then GlobalFoundries in 2009. At AMD and GF, he was leading and managing the Technology & Reliability Development Organization. In 2011, Amit joined Microsoft and was managing the Silicon/Packaging Operations & Reliability Org for all of Microsoft Hardware. Amit joined Google in 2016 where he is heading the SOC/Module Technology and Reliability Engineering & supporting all programs within Consumer Hardware Org at Google.

Amit has co-authored over 40 technical research publications as well as a chapter in a book on Moore's Law Scaling Reliability Challenges. He has chaired sessions at IRPS Conf. and presented "Year in Review" on System Reliability. He has also given keynotes at other International Conferences. He is a co-inventor of over 15 patents granted and over 50 pending US patents in the area of technology & reliability development.

Amit Kale earned his M.S. and Ph.D. in Mechanical engineering from University of Florida, Gainesville in 2005. After completing his Ph.D., Amit joined General Electric Global Research Center in Niskayuna, NY and worked on research and development of jet engines and land based turbines. Amit joined Baker Hughes in 2012 and worked in oil and gas industry for development of predictive analytics and data science for drilling equipments reliability and efficiency. Amit is currently working as a Reliability Program Leader at Google on Moonshot products. Much of Amit's research and industry experience concerns machine learning, data science, reliability analysis and modeling, fracture and fatigue mechanics, and structural design optimization, among other topics. Amit has published over 25 publications in peer reviewed journals and conferences. He is an inventor in two patents and co-inventor in two pending US patents in area of data science and engineering.

Accurate estimation of system level reliability requires a thorough understanding of the failure modes of the various components and modules that make up the system and their interactions with each other. A clear definition of Mission profile is necessary to project the test data to use conditions. With the increasing use of smart devices, mobile technologies and ubiquitous computing, the usage scenarios are getting increasingly complex. As a result, JEDEC based standard Qualification methodologies for components cannot be relied upon to ensure reliability at system level during field usage. This tutorial will introduce the methodology of "Reliability Budgeting" and show how this can be applied at chip level and then at the system level using a tops-down and bottoms-up approach to realize an optimum trade-off between performance and reliability. We will outline the methodology for a rigorous DFMEA process (Design Failure Mode Effects Analysis) which is vital to implement a "Design for Reliability" (DFR approach). The tutorial will also discuss scenarios where system reliability may be improved and demonstration test duration may be reduced by adding redundancy. Using specific test cases, we will also demonstrate the process of optimizing tradeoff between cost of redundancy vs reducing maintenance cost of the system. Finally, a methodology to calibrate component level failure models and test plans is demonstrated from life data on fielded product.

3D Transistor reliability: BTI

Background BTI - Measurements, Modeling and Variability

1) Measurements - the one point drop down method is kind of widely used to sense Vt shift. However, what should be the measurement speed, stress bias range and stress time range (to minimize recovery and EOL extrapolation errors) for bench test? Is there any concern regarding corrections required for long measurement delay typically encountered for HTOL tests? Also, is Vt sense enough, or do we need to sense other parameters (like Idlin etc) as well?

2) Modeling - Modern transistors are 3D (with quantum effects in the channel), and actual operation involves mixing of HCI, BTI and self heating effects. Is there a need to invoke TCAD for accurate device level simulation (and isolation of different effects)? On the SPICE compact model side - is DC enough, or there is need for good AC (eg duty cycle) modeling? Are the existing CAD vendor frameworks good enough (is there any consistency between different foundry models), or there is need to develop an uniform, consistent compact model platform? Is there any benefit to include ageing/BTI in DTCO efforts? Finally, with new materials (SiGe channel, III-V channel, N, F, dipole, trace elements in the gate stack), is there a requirement to bring in ab-initio models for prediction?

3) Variability - What are the relative importance of time-zero (eg process related) and BTI variability? Are these fully uncorrelated or weakly correlated? What is the importance of RTN? Does RTN change after BTI stress?

Moderators

Souvik Mahapatra received his PhD from IIT Bombay in 1999. During 2000-01, he was at Bell Laboratories, Murray Hill, USA. Since 2002, he is at the Department of Electrical Engineering at IIT Bombay and presently a full professor. His current research interests are CMOS device scaling and reliability, memory device reliability, and device-circuit co-design for co-optimisation of power, performance and reliability. He has published more that 150 papers in peer reviewed journals and international conferences, delivered invited talks at major international conferences including IEEE IEDM and IRPS, and has been actively collaborating with several global semiconductor industries. He is a fellow of IEEE (for contributions to CMOS transistor gate stack reliability), fellow of Indian National Academy of Engineering (INAE) and fellow of Indian Academy of Sciences (IASc), distinguished lecturer of IEEE Electron Devices Society (EDS), and holds visiting faculty positions at Purdue University and University of Notre Dame.

Chadwin D. Young received his B.S. degree in Electrical Engineering from the Univ. of Texas at Austin in 1996 and his M.S. and Ph.D. in EE from the North Carolina State University in 1998 and 2004, respectively. In 2001, he joined SEMATECH where he completed his dissertation research on high-k gate stacks and continued this research at SEMATECH working up to Senior Member of the Technical Staff on electrical characterization and reliability methodologies for the evaluation of high-k gate stacks on current and future device architectures. He joined (09/12) the Materials Science and Engineering Department at the University of Texas at Dallas as an Assistant Professor where his research focus is on electrical characterization and reliability methodologies for the evaluation of future materials and devices. He has authored or co-authored 250+ journal and conference papers. He has served: on the management or technical program committees of IIRW, IRPS, SISC, IEDM, WoDiM; as Guest Editor for IEEE Transactions on Device and Materials Reliability; and as a peer reviewer for several journals. He is currently a Senior Member of IEEE.

3D Transistor Reliability: Hot Carrier (HC) Degradation

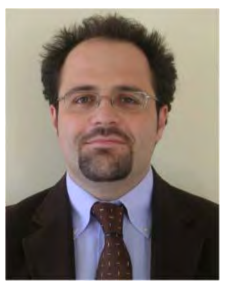
Background

In recent technology nodes, Hot Carrier-induced degradation is coming up arguably as the most concerning FEOL degradation mechanism. As a consequence of its inherent physical complexity, HC degradation requires careful experimental characterization and thorough modeling for relevant reliability projections. In this workshop, we will discuss recent trends in HC literature, focusing on a list of topics related to current characterization practice, modeling approaches, and device engineering for HC mitigation, with the goal of assessing the existence of a consensus view of the reliability community on each of these aspects.

Discussion topics:

- HCD is traditionally studied at worst-case bias (i.e., maximum impact ionization) or at $V_G=V_D$: is this still enough? Does the community see a need to move toward more comprehensive studies in the whole $\{V_G,V_D\}$ bias space? Is it acceptable to simply rescale the degradation measured in DC at worst-case bias to the actual AC workload?
- Does the bias history affect the device degradation (e.g., is BTI the same on a device which already suffered severe HC degradation)?
- How can one de-embed the SHE impact on the degradation consistently across the whole $\{V_G,V_D\}$ bias space?
- Is variability of the HC degradation relevant? If yes, what experimental approaches are effective to characterize it across the $\{V_G,V_D\}$ stress bias space?
- Is Off-state hot carrier stress also a relevant degradation mode for Si finFETs? If yes, which unified failure criterion can we use for any stress $\{V_G,V_D\}$ combination? (note: the typical shifts of I_{Dsat} and V_{th} are not enough for Off-state degradation as other device metrics as I_{off}, SS, GIDL, also degrade)
- HC mitigation at the device level: which device design strategies are effective without penalty on the device performance (typical trade-offs: abrupt junctions --> better short channel controls --> higher electric field peak --> worse HC!; high-mobility channels (SiGe) --> larger carrier mean free path --> worse HC!)
- Theoretical studies focus on individual physical degradation modes (e.g., Single-Vibrational Excitation vs. Multi-Vibrational Excitation for the Si-H bond breaking): how should one decouple these modes and what acceleration model should one adopt to project the degradation of devices during real use (i.e., bias spanning dynamically a given trajectory in the {Vg,Vd} space)?
- Are empirical models (based on physical understanding) sufficient for HC degradation or should we adopt complex full physics models (including, e.g., carrier distribution functions; electron-electron scattering impact on the energy tails, etc.)?
- What classes of circuitry is HCI a concern for (clock distribution, high-speed IO, SerDes, etc.) vs. not (data paths, sequentials, SRAM, etc.)?

Moderators



Jacopo Franco is a Principal Member of Technical Staff at imec, Belgium. He received the B.Sc. (2005) and M.Sc. (2008) in Electronic Engineering cum laude from the University of Calabria - Italy, and the Ph.D. degree in Engineering summa cum laude from KU Leuven - Belgium (2013). His research focuses on the reliability of high-mobility channel MOSFETs, on modeling of oxide traps in novel MOS gate stacks, and on time-dependent variability in nanoscale devices. He has (co-)authored 190+ publications in international journals and conference proceedings, including 20+ invited papers, 1 book, 3 book chapters, 2 international patent families. He received the Best Student Paper Award at IEEE SISC (2009), and the EDS Ph.D. Student Fellowship (2012). He is one of the recipients of the EDS Paul Rappaport Award (2011), and the Best (2012), Outstanding (2014), and Best Student (2016) Paper Awards at IRPS. He is serving as a Technical Program Committee member at IRPS, IIRW, ESREF, WoDiM conferences, and as an Editor of IEEE Transactions on Device and Materials Reliability.

Chetan Prasad is the Quality and Reliability R&D manager for the 7nm process generation at Intel Corporation. He received his B.E. (1997) in Electronics and Telecommunications Engineering from the University of Mumbai, India, and his M.S. (1999) and Ph.D. (2003) in Electrical Engineering from Arizona State University, USA. His work is focused on technology reliability research across Intel's 90nm to 14nm process generations. During his tenure at Intel, he has been the recipient of 3 Intel Achievement Awards (IAA) and 10+ Divisional Awards. He has authored/co-authored 60+ papers in international journal and conferences, including the delivery of several invited talks and tutorials, and has both awarded, as well as pending, patents. He has served on multiple Technical Program Committees at IRPS, IEDM and ESREF, has peer reviewed publications for IEEE Transactions on Electron Devices, and has contributed to multiple JEDEC standard definitions.

Advanced packaging reliability: 2.5D, 3D and fan-out packaging for system scale

Background:

Recently advanced packaging technologies of 2.5D, 3D and fan-out have attracted attention for realizing high performance and multi-functionality systems. But heterogeneous integration of various materials and devices for 2.5D, 3D, fan-out packaging has crucial reliability challenges. Moreover, a trend of 3D/2.5D packaging towards thinner chip, more layer stacking, and more joining density to maximize area efficiency. Fan-out packaging requires more fine width/space, and multi-layers of Cu RDL for multi-dies integration. These trends could induce severe potential reliability challenges. Therefore, advanced packaging reliability becomes a hot research topic for further system scale. The main objective of this workshop is to discuss the reliability challenges and possible solutions for mass volume manufacturing start. However, the discussion will be by no means limited to this topic and other subjects will also be covered such as characterization/simulation techniques, impact of materials choice.

Moderators:

Kang-Wook (Kriss) Lee is currently VP, R&D, Amkor Technology Korea. He received the Ph.D. degree in machine intelligence and systems engineering from Tohoku University, Sendai, Japan, in 2000. From 2000 to 2001, he was a Researcher with Japan Science and Technology Corporation, Sendai, Japan. From 2001 to 2002, he was a Postdoctoral Researcher with the Department of Electrical, Computer, and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY, USA. From 2002 to 2008, he worked with Packaging Development Team, Memory Division, Samsung Electronics Ltd., Korea, as a Principal Engineer, where he led the research and development of TSV based 3D packaging technologies. From 2008 to 2016, he was a professor with Tohoku University, Sendai, Japan. He has led the development of 3D hetero-integration technology for multi-functional convergence systems, multi-chip self-assembly technology, exa-scale 2.5D/3D integration technology, and the reliability studies of 3D-IC. Especially, he worked pioneerly the studies about the impacts of 3D integration process such as Cu TSV formation, wafer thinning and micro-joining of thin chip on reliability of 3D stacked devices by leading the world.

He is a Senior Member of the IEEE.

Emre Armagan joined Intel Corporate Quality Network (CQN) organization as Assembly Test Technology Development Quality and Reliability (ATTD Q&R) engineer in 2011. He is currently ATTD Q&R Senior Engineering Manager responsible for assembly and substrate process technology development. He has worked on silicon far backend, FLI and package quality and reliability; and supported pathfinding and technology development for various multi-die products and 2.5D/3D package integration, including Intel's Embedded Multi-Die Interconnect Bridge (EMIB) solution. He has authored/co-authored multiple papers as invited, journal and conference publications and has

awarded and pending US patents. His industry engagements include contributions to IRPS and InterPACK technical committees and journal reviews.

Automotive: what are the challenges for new technologies?

The requirements flow chain for microelectronics as well as for intelligent power electronics that is intended to be used for future e-mobility, infotainment and autonomous driving applications is changing in the same way as the whole automotive industry is in a transformation process. From a business perspective, the car becomes a product that integrates all possible variants of complex semiconductor based functions with makes it an attractive object for seed funding of even wider targets (e.g. AI) within various other industry sectors.

From a functional perspective, many hardware (incl. architecture) related requirements will need to follow new SW based requirements. From a HW/SW maintenance, security, reliability and cost perspective the automotive industry now requires high performance, low power and resilience capable (fail operational) robust technologies. Of course, this relates to chip, but as well also to corresponding construction and connections technologies (assembly) that interfere with automotive load scenarios. An obvious challenge for automotive is the semiconductor/assembly technology focused mass volume target product specification and its deviation from corresponding automotive specs. However, transparency about these deviations already opens cost effective compensation and technology enhancement opportunities.

This discussion group will strike a dialogue to focus on leading-edge technologies verification, validation and qualification approaches in order to also conclude on necessary change and extension scenarios (technology readiness process) to adapt those approaches to new technology generations as well as to corresponding application fields. General and application specific technology capability enhancement options will be discussed. For those that are interested to actively participate in the discussion group it should be noted that although 'automotive requirements' are behind this discussion, the 'solutions space' and methodology options is assumed to be of general nature and are in principle applicable to various high demanding industries as the automation industry, aviation and military.

Moderators:

Khai Nguyen received his Bachelor (confered with great distinction) and Ph.D. degrees in Electrical Engineering from Concordia University, Montreal, Quebec, Canada in 1994 and in 1999, respectively. He was a recipient of NSERC (Natural Sciences and Enegineering Research Council of Canada) awards twice. He was awarded Phoivos Ziogas Medal in 1994, and received Canadian Advanced Technology Award in 1997 for academic achievements.

In the last 10 years, he has been with NVIDIA. His reponsibilities include product-level reliability characterization and qualification, customer engagement. He is a voting member in JEDEC 14.1, 14.2, 14.3.

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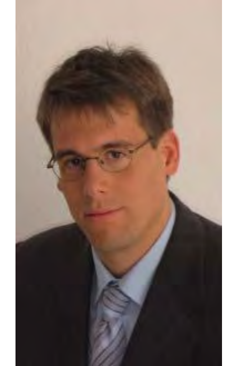
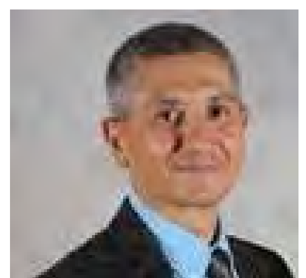


Andreas Aal leads the semiconductor strategy and reliability assurance activities within the electric-/electronic development department at Volkswagen, Germany, which he joined in 2011. His activities concentrate on technology capability enhancement of nodes down to 12 nm as well as optimization of power electronics for automotive applications. He leads two semiconductor related European projects and is a strong representative of the through-the-supply-chain-joint-development approach. Mr. Aal has been working within the semiconductor industry since 1998 holding different positions from engineering to management working on production monitoring, process and technology development, qualification, and failure analysis. He was involved in device optimization, the development of test structure design as well as new combined stress/measurement and data analysis methodologies for qualification and fWLR monitoring. Andreas (certified reliability professional) published and co-authored various papers, has given invited talks, served as reviewer for different Journals and has served in the technical and management committee for IEEE IIRW. He is a member of the IEEE Electron Devices, CPMT, Nuclear and Plasma Sciences, Reliability and Solid-State Circuits Societies and also a frequent participant / contributor of the JEDEC subcommittee 14.2. Since 2007 he is chair of the German ITG group 8.5.6 (VDE) on (f) WLR, reliability simulations and qualification.



Dr. Shalabh Tandon is the Director of Internet of Things (IOT) Product Q&R group that is responsible for qualifying products for this emerging market. The IOT division at Intel services the embedded, retail, industrial markets as well as the expanding automotive (ADAS or fully autonomous) markets where computational needs and workload complexities are increasing at a rapid pace.

Shalabh joined Intel in 1997 in the packaging quality and reliability group. Over his ~20 years at Intel, Shalabh has worked in the Corporate Quality Network (CQN) serving various functions. His tenure has included responsibilities in understanding thermomechanical

behavior of polymers in semiconductors, especially from a reliability perspective; product testing for performance and quality using various functional sockets; qualification strategies for various semiconductor usage approaches. His current focus is both understanding the usage of semiconductors in the IOT space, especially automotive industry, and ensuring the products needed for these evolving markets are capable of meeting customer's computational and quality and reliability needs.

Shalabh holds a MSc in Chemistry from University of Pittsburgh & a Ph.D in Polymer Science & Engineer from University of Massachusetts, Amherst. He has published several technical articles in peer reviewed journals and holds a few patents.

2018 IRPS Workshop: Challenges and Advances in Advance Node Interconnect Reliability

Background

Several new areas of challenge exist for interconnect reliability stemming from the ever present drive for dimensional scaling and RC delay reduction. The challenge associated with dimensional scaling and variability is a consistent theme for advance nodes and is further exacerbated by minimal to no scaling in operating voltages. New materials for inter-layer dielectrics, dielectric spacers, etch stop layers, Cu/ILD barriers are introducing new challenges for interconnect reliability in the Back-End-of-Line (BEoL) and in the Middle-of-Line (MoL). New integration and patterning schemes like Air Gaps, self-aligned vias and contacts, and EUV patterning might offer a balance of reliability enhancing and detracting aspects. Beyond the direct assessment of intrinsic reliability in interconnects there is an additional set of challenges to assess, predict, and control end product reliability which incorporates other aspects like latent defectivity, package stress, and the challenge of assessing metallization reliability in product like configurations. In this workshop we will focus the discussion on the key areas of interconnect challenge in the present and near term, and discuss the prospects for advancement in reliability methodology that might be used to mitigate these challenges for end product reliability spanning across various market segments.

Workshop Co-Moderators:

Patrick Justison (Patrick.justison@globalfoundries.com)

Dr. Patrick Justison received his Ph.D. and M.S.E. in materials science from the University of Texas and his B.S. in materials science from Lehigh University. He has been with GLOBALFOUNDRIES since its inception in 2009, after joining AMD in 2008. He currently the leads the BEoL reliability team in Malta, NY. He and his team are responsible for all aspects of interconnect reliability, including development, qualification, PDK support, and development of novel methodologies for advanced technology nodes. Previously, he was with Freescale in Austin, TX where he also focused on BEoL reliability topics.

Dr. Rahim Kasim (Rahim.kasim@intel.com) is a Reliability Manager in Intel's Logic Technology Development Group working primarily on MOL/BEOL reliability across 14nm/10nm and 7nm Technology nodes. He joined Intel in 2005 after receiving Ph.D. and M.S degrees in Electrical Engineering from Arizona State University. His interests includes BEOL/MOL dielectric Reliability and Interconnect Reliability

Circuit Reliability
Advanced nodes concerns and CAD tool flows

Moderators:

Matthew Hogan, Mentor, A Siemens Business
Wonjae Kang, Intel
Hiu Yung Wong, Synopsys

Device physics, detailed simulations and angst over the next generation of interconnect electromigration and other reliability rules drive much of the challenges many of us face on a daily basis. In isolated environments, testchips and accelerated testing form the basis for the recommendations that are made to drive reliability design rules. But what about the circuit designs, the layout engineers and our verification and CAD teams? How does the larger ecosystem supporting and executing robust IC design flows benefit from these findings and what form will they take so that next generation designs can be created while keeping up with the aggressive turn-around-times required for market introduction?

Please joins us in this workshop as we discuss best practices and concerns of advanced process nodes and their associated CAD flows. We will start with the challenges facing simulation and how reliability verification and advanced CAD flows, along with foundry supported rule decks can help establish a solid baseline to build upon, including:

- Pre-silicon characterization efforts for reliability, design for reliability(including correct-by-design), and the impact on design rules and reliability verification.
- The wide range of challenges with simulation infrastructures, custom circuits, and modeling of reliability effects including circuit interaction.
- Balancing productivity efficiency with circuit complexity and increasing transistor count with the desire to incorporate 2nd order issues.
- The role of DFT to identify and isolate damage in manufacturing failures and field returns, before the descriptive process of analysis begins.
- Understanding best practices being used by different groups within the industry and the trade-offs on what to simulate, and when.

Share your experience and learn from others as we discuss the challenges we face as we transition to not only the “next” node, but also consider the implications of continuing to use or migrating bulk substrate designs, FD-SOI, finFETs or planar transistors and the legacy IP that has been proven. What are the applications that are driving these decisions and the design choices that are creating an environment for change?

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Matthew Hogan is a Product Marketing Manager for Calibre Design Solutions at Mentor, a Siemens Business, with over 18 years of design, field and product development experience. He is actively working with customers who have an interest in Calibre® PERC™ or reliability verification. Matthew is an active member of the International Integrated Reliability Workshop (IIRW), is on the Board of Directors for the ESD Association (ESDA), contributes to multiple working groups for the ESDA and is a past general chair of the International Electrostatic Discharge Workshop (IEW). Matthew is also a Senior Member of IEEE, and a member of ACM. He holds a B. Eng. from the Royal Melbourne Institute of Technology, and an MBA from Marylhurst University. Matthew can be reached at matthew_hogan@mentor.com

Wonjae L Kang, Intel
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Wonjae L. Kang leads design reliability capability and methodology development efforts at Intel Corporation. Meeting technical challenges with complexity increase reliability mechanism in high-performance and complex designs in IP and SOC designs has been the passion for Wonjae over two decades. Wonjae has technical and engineering management experiences in process, design/CAD enablement and product qualification/ramp. His focus area of expertise is enabling design CAD/Methodology solutions ranging from correct-by-construction to verification for critical reliability mechanisms and design quality interaction issues. Previously he also led an industry-wide initiatives in enabling CAD and design methodology efforts to tackle complexity increase with design automation efforts for Designing-In-Reliability. He received MS and BS in Electrical Engineering from Arizona State University.

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Hiu Yung Wong received his Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley in 2006. Between 2006 and 2009, he worked as a Technology Integration Engineer on 45/32nm NOR flash memory in Spansion Inc., Sunnyvale. Since 2009, he has been with Synopsys Inc., Mountain View, where he is currently a Senior Staff AE in TCAD simulation. His research interests include NBTI and hot carrier degradation simulation in FinFET/nanowire/nanosheet, wide band gap materials (such as GaN, Ga_2O_3 and Diamond) device and reliability/defect simulations, novel semiconductor device design and Design Technology Co-Optimization (DTCO). Part of the activities are reflected in the near 50 publications and patents applied. He is a senior member of IEEE.

Circuit Reliability: In-field healing and repair – serious need or science fiction?

With continued Moore's Law scaling to 7nm node and beyond, CMOS technologies face variability and reliability challenges that impact performance, power, and yield. While static variations can be handled by more robust post-silicon test and binning procedures, dynamic variations are impacted by environmental conditions, activity, and workload. These variations coupled with ever-increasing chip complexity present large challenges for guaranteeing reliability at an acceptable cost. These challenges are becoming especially critical in markets such as automotive and avionics with stringent reliability requirements. While in-field dynamic adaptation to temperature and voltage fluctuations has become standard for many semiconductor devices, techniques for detecting and compensating reliability degradation are still in their infancy [1-3]. Thus the question arises: is in-field healing and repair a serious technology need, or science fiction?

At the device level, various solutions have been examined for reducing impact of wearout issues such as hot-carrier degradation and bias temperature instability: annealing defects at very high temperature in silicon bulk MOSFETS [4,5], using short self-healing in flash memory [6] and in gate-all-around MOSFETs [7], by oxide charge neutralization with opposite-carrier injection [8], and by using forward current in the drain-bulk junction [9]. While promising at the device level, most of these solutions are not feasible to implement in operating circuits. This can be overcome using real-time carrier injections (however the gain in device lifetime is limited [8]) or through the use of forward body bias in FDSOI technology [10], but a high-level methodology is needed from circuit to system level, that is based on a hierarchical framework [3] for the trade-off between performance, activity, and power consumption.

At the circuit level, techniques have been demonstrated for detecting and responding to dynamic fluctuations in temperature, voltage, and workload demand. It is now feasible to extend these techniques to monitor and maintain reliability in the field. For example, an in-situ mission profile recorder [11] used with thermal sensors can dynamically adapt the frequency or supply voltage in response to changes in activity, variability, or aging that are detected by in-situ slack monitors [3,12,13]. These adaptive techniques will become more important as reliability requirements become more stringent, and as process scaling becomes more difficult. However, advancements are required not just on the detection circuits and adaptation techniques, but also on dedicated analog and digital design flows to enable reliability-aware design platforms and a full self-adaptive design methodology from devices to software [14].

Improving in-field reliability further will require advancements in the entire design hierarchy from devices to software. Early-life failures due to latent defects or electromigration cannot easily be detected with monitor circuits, and adaptive voltage and frequency techniques cannot repair permanent failures. Instead, techniques for core/circuit self-test and repair [15-16] are needed, as well as methods to maintain system performance as self-test is performed, and the necessary level of redundancy to repair failures in a way that is invisible to the application (and the customer). These techniques have been explored for high-reliability server processors but are difficult and expensive to adopt. Is this level of reliability monitoring and repair necessary in other applications? At what point does the reliability benefit of these techniques justify the investment in cost and complexity? How can the dramatic increase in device count that comes with every process generation be used to not only add features and improve performance, but also improve reliability and yield? When will our semiconductor devices "heal themselves“?

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Moderators:

Alain BRAVAIX graduated from the University of Sciences of Paris (PhD-1991). Since 1994 he is professor for Engineering and Master Degree at the Institut Supérieur d'Electronique et du Numérique (ISEN-Toulon) developing research activities on the reliability and optimization of ultra-short CMOS nodes. Since 2000, he is a member of the Institut Matériaux Microélectronique Nanosciences de Provence (IM2NP) UMR 7334 and has supervised 15 PhD students since 2005. He is now (2014)

member of the "Radiation Effects and Electrical Reliability (REER) joint Laboratory" with ST Microelectronics Crolles and Aix Marseille University. His research interests cover semi-conductor physics, device to circuit reliability, electrical characterization techniques for nanoscale CMOS nodes. He developed research activities on Electro Static Discharge (ESD) for automotive applications with INFINEON (Munich), nitridation processing with CNET (Grenoble) and for circuit reliability devoted to avionics and space applications (EADS). His research interests cover device to circuit reliability, process optimizations, electrical and fast characterization techniques in ultra-thin gate-oxides (SiON, High-K), for novel and ultra-small CMOS FDSOI technology. He is a member of the IEEE Electron Devices and Reliability Society and become an IEEE Senior member in 2012. He is the author or co-author of 165 technical papers (53 journals) in these fields with 14 invited papers or tutorials (9 Best paper awards for his PhD students). He is a member of technical committee of ESREF and IEDM (2014-15), reviewer for scientific journals as Transaction on Electron Devices, Transaction Device and Material Reliability, Solid State Electronics and Microelectronics Reliability.

Jim Tschanz is a circuits researcher at Intel Corporation in Hillsboro, Oregon and the Director of the Intel Circuit Research Lab. He received his B.S. degree in computer engineering and M.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign, and since 1999 has been involved in low-power circuits research at Intel. He also taught VLSI design for 7 years as an adjunct faculty member at the Oregon Graduate Institute in Beaverton, OR. He has published over 100 conference and journal papers, has authored 3 book chapters, and has 75 issued patents.

Emerging memory reliability challenges and opportunities in MRAM, RRAM, PCM, 3DXP

Background

Several non-charge-based nonvolatile memories are categorized as “emerging” memories, not suffering from charge-specific issues like scaling limited by statistical fluctuations from small numbers of stored charges or charge leakage. The workshop will consider each emerging memory technology, including MRAM, PCM, RRAM, and 3D X-point, to discuss their reliability physics and reliability issues. These emerging memories typically employ a two-terminal resistive device combined with a selector, thus the adoption of selection devices will be considered in the form of 1T-1C, 1T-1R, or 1D-1R, the diode selector being the key to practical 3D cross-point memory. However, the discussion will be by no means limited to this topic and other subjects will also be covered such as memory device characteristics, characterization techniques, impacts of variability, and materials choice.

Questions:

1. What are the top two reliability concerns for each of the emerging memories?
2. Do devices that employ atomic (or ionic) motion to change states have inherent reliability limitations due to the reversibility of the resistance change process? If so, are there failure acceleration methods and models to experimentally predict the limits?
3. Is there a clear separation of intrinsic and extrinsic failures in each of these device types?
4. Is a tradeoff between endurance and data retention time inherent to all of these devices? Same question for endurance – speed and endurance – write energy.

Moderators:

Jon Slaughter is a Principal Research Staff Member and Cognitive Nonvolatile Memory Technologist at IBM Research in Albany New York. Dr. Slaughter has over 20 years of experience in MRAM and related technologies with emphasis on developing new materials and devices for reliable products, including the world's first commercial MRAM products. He worked previously at Motorola, Freescale Semiconductor and Everspin Technologies, Inc. He received his bachelor’s degree in physics and mathematics from the University of Wisconsin, River Falls, and doctorate in physics from Michigan State University.

Dr. Chung-Wei(Jerry) Hsu is a Principal Engineer at TSMC. He received Ph.D in Electronics Engineering, National Chiao Tung University (NCTU), Taiwan, in 2016. He was a visiting scholar in Electrical Engineering and Stanford SystemX Alliance, Stanford University. His research interests include the development of terabit nonvolatile RRAM, reliability Physics and memory device characterization. He joined TSMC in 2016 with Path-Finding team for N5/N3 technology FEOL transistor integration development as well as FEOL module development.

GaN reliability for power and RF devices- what are the key issues and how to resolve?

Brief summary: GaN has recently emerged as an excellent material for the fabrication of both RF and power transistors. RF transistors are already in widespread use in satellite, radar and communication fields. Power transistors are now rapidly finding application in the next-generation power conversion systems with 600-650V transistors already commercially available.

The present success of GaN is a testament to the good intrinsic reliability of the technology. This has been achieved by an understanding of key failure modes and mechanisms. A market transformation is now underway, and the next step is one of high-volume reliability. The aim of this workshop is to understand which are the still-open issues: is charge trapping still impacting operation? What are the main reliability concerns? What are the acceleration laws? How are the different operating regimes (of-state, on-state, semi-on) impacting reliability? What are the pathways for industrial-level reliability? Which testing procedures must be used for reliability estimation/assessment? Are there any learnings from the (longstanding) RF GaN experience that can be applied to power GaN?

This workshop will address these questions, by stimulating the discussion on the key issues that presently limit the reliability and the performance of GaN-based HEMTs. It will be a natural lead-in for the subsequent workshop on WBG reliability synergies and standardization.

Moderators

Sandeep Bahl is a distinguished member of technical staff in the High Voltage Power Business Unit of Texas Instruments. He has extensive experience with semiconductor technology development, and has worked on both silicon and compound semiconductor technologies. His present focus is to bring reliable GaN products to market, and to develop the methodology to know that they will be reliable under actual-use conditions. Sandeep helped kickoff the standardization effort of the GaN industry and is presently participating on the JC70 reliability committee as a task-group co-chair. He has served as chair of the Power and Compound Semiconductor subcommittee of the International Electron Devices meeting (IEDM) and of his local San Francisco/Santa Clara valley IEEE chapter. He is presently serving as chair of the IRPS Wide Bandgap Committee. Sandeep graduated with a PhD in Electrical Engineering from the Massachusetts Institute of Technology.

Matteo Meneghini received his PhD in Electronic and Telecommunication Engineering (University of Padova), working on the optimization of GaN-based LED and laser structures.

He is now assistant professor at the Department of Information Engineering at the University of Padova. His main interest is the characterization, reliability and simulation of compound semiconductor devices (LEDs, Laser diodes, HEMTs).

Within these activities, he has published more than 200 journal and conference proceedings papers.

During his activity, he has cooperated and/or co-published with a number of semiconductor companies and research centers including:

-OSRAM-OptoSemiconductor (Germany)
-Panasonic Corporation (Japan)
-Universal Display Corporation (USA).
-NXP (The Netherlands)
-ON Semiconductors (Belgium/USA)
-Sensor Electronic Technologies (USA)
-IMEC (Belgium)
-Infineon (Austria)
-Fraunhofer IAF (Germany)
-University of Cambridge (UK)
-Universiy of California at Santa Barbara (USA)
-University of Wien (Austria)

Meneghini is a Senior Member of IEEE and a member of the SPIE. He – together with his colleagues - won several best paper awards at international conferences (including ESREF 2009, IWN 2012, ESREF 2012, ESSDERC 2013). He is/has been involved in the technical program committee of several conferences including IEEE-IEDM, IEEE-IRPS, ESSDERC, ESREF.

IRPS Workshop: Providing Enterprise Level System Reliability in the Sub-10nm Technology ERA

1. Background.

The leading-edge technology nodes required for SOC (System on a Chip) have become increasingly complex, requiring device, wiring, and packaging level innovations to sustain the demand for increased processor efficiency, density and performance. These innovations include finFETs, Nanosheet FET, Vertical FETs, Ultra Low K Dielectrics, 2.5D and 3D chip package integrations. With the rapid pace of these innovations (including higher SOC core & socket content), it has become increasingly more difficult for the technology and product reliability teams to effectively reduce the reliability failure rates that meet the enterprise system reliability requirements. From a system level perspective, there are additional reliability challenges with increase in non-volatile memory technology, higher speed I/O interfaces, and off chip accelerators.

The challenges are clear:

1) Identify any new 'systematic' defects that are a direct or indirect result of the new innovative technology and implement process integration modifications to reduce or eliminate these 'systematic' defects.
2) Enable sufficient 'random' level reliability defect learning given the image size reduction and increased circuit density.
3) Maximize System Reliability, Availability, & Serviceability (RAS) product and system design features to address the failure rate mechanisms that have the largest potential impact to system reliability.
4) Ensure sufficient technology reliability lifetime, including BTI, Hot e-, EM, TDDB, and SER that supports enterprise level system lifetime requirements.

The key question is, how do we accelerate our technology and product reliability learning to keep pace with the level of innovation and scaling facing the SOC development and manufacturing teams? In the keynote address at IRPS 2017, four major initiatives to address the above challenges were suggested:

- Evaluate Technology Qualification Data Early & Often w/ Emphasis on Functional Stress
- Ensure Intrinsic System Lifetime → Based on Kinetics + Application
- Mitigate Impact of Variability with Process Controls, Chip Design for Manufacturability, & System Design Techniques.
- Build End to End Capability to Screen / Eliminate Subtle Functional Defects (including excursions that may be the result of unique user experience / software)

This list is only a starting point of high level ideas to achieve the learning required in the 10nm / 7nm technology nodes. We would like to explore these in more detail by asking the following questions:

1. Do you think we are experiencing a higher level of new reliability failure mechanisms in the 14nm / 10nm / 7nm technology nodes?
2. How can we more effectively identify new, systematic reliability defects encountered during the early technology development cycles (L1 & L2)?
3. How can we improve our ability to 'screen' reliability defects without impacting system EOL integrity? Including Wafer Level, Module, and System Screens?
4. How can we effectively 'design-in' better chip and system level RAS to mitigate the increases in reliability failure rate?
5. What is the single biggest challenges facing our reliability teams in sub 10nm generation technology

Moderators:

Mr. Ronald Newhart is currently a Distinguished Engineer with IBM working in the Systems & Technology Group, focusing on product engineering and reliability. His first nineteen years with IBM entailed assignments in semiconductor parametric and functional characterization, memory design, yield modeling, and reliability engineering. For the past seventeen years, he has been the lead technology interface to the IBM POWER and Z Series circuit design teams. Ron's contributions have supported the development and manufacturing of more than nine generations of POWER and Z System microprocessors. Ron frequently consults on complex problems that span design, process, and technology for both IBM internal products and other IBM System supplier components. He has co-authored fourteen US Patents and has received several corporate awards.

Mr. Newhart has a Bachelor of Science degree in Electrical Engineering from Pennsylvania State University and a Master of Science degree in System Management from the University of Southern California.

Cameron McNairy is a system reliability, availability and serviceability (RAS) architect for Intel's high performance computing (HPC) efforts. Previously, he drove processor level fault-tolerant solutions as a processor architect for Intel Xeon and Xeon Phi specializing in RAS. Prior to his work in HPC, Cameron was an architect for the Intel Itanium line of processors supporting efforts in RAS, firmware, performance and design. Cameron has been awarded 10 patents, authored or co-authored 8 papers, and has spoken in many forums on a wide variety of topics relevant to the HPC and mission critical computing challenges. He received a BSEE and a MSEE from Brigham Young University and is a member of the IEEE.

Storage and Memory – SSD, SD, DIMM: Resiliency in design, system-level considerations and role of usage analytics

Background:

Modern leading-edge storage and memory technologies and products are often integrated systems comprising innovations drawn across leading-edge non-volatile and volatile memory, controller, DRAM and even firmware designs. In many cases, innovations of different measure and across various domains need cohesive integration for deriving practical benefits in a reliable manner. Towards that end, inherently designed resilience often becomes a critical enabler for robust storage and memory devices. Critical balance in stress-strength interaction, achieved with appropriately conservative trade-offs in design, are often necessary for appropriately accommodating usage models. In this workshop, one of the intents is to discuss the appropriate levels of resiliency in storage and memory design, towards enabling their robust operational physics.

Can data analytics aid in this endeavor? Wide variances in continuously evolving usage scenarios cover many different stress exposures. Analytics coupled with domain knowledge of system-physics can provide opportunities for understanding usage scenarios of interest, while leveraging machine-learning for system-level models relevant to stress-strength interaction relevant to reliability. Data availability on system-level operational physics can therefore become a key enabler in this quest.

Moderators

Jay Sarkar is a Technologist at Western Digital Corporation (HGST) focused on solid-state storage (SSD) analytics and robustness research and development at the system level. His professional experience of 10 years has included core physics and reliability research and development leading to the first Phase Change Memory technology implementation at Intel and Numonyx (Intel spin-off, now Micron) at 90 nm and 45 nm lithography nodes; and a novel reflective, power-efficient display technology development based on microelectromechanical systems (MEMS) at Qualcomm. He has authored/co-authored 16 peer-reviewed international conference and journal papers across diverse domains of system and device physics, analytics, reliability and process modeling of SSDs, Phase Change Memory, 3-D NAND Flash memory and lower-dimensional electron transport. He has issued or filed/pending patents on machine-learned solid-state storage analytics, Phase Change memory array programming for robustness and MEMS encapsulation design. He earned a PhD in Electrical and Computer Engineering from the University of Texas at Austin (awarded the Ben Streetman Prize for dissertation research), M.S. in Applied Physics from Rice University, Houston and B.S. in Physics from the Indian Institute of Technology, Kharagpur. He is a member of the IEEE and has served on the Technical Program Committee of the International Reliability Physics Symposium.

<u>Haitham Hamed</u> has more than 20 Years of experience working on various memory technologies (SRAM, DRAM and Flash) and their end systems. Recently concentrating on SSD system reliability and very low failure rate systems. Worked for a number of startups and large IDMS such as ST Micro, LSI and Avago technologies. Currently working for SK Hynix in their memory Solutions division in San Jose concentrating on SSD Controller Quality & Reliability and aiming to achieve ultra-low failure rate SSD controller. This should easily translate to high reliability SSD Drives for both client and enterprise applications.

Synergies between GaN and SiC Power Devices for reliability development and standardization

A worldwide effort is underway to develop standards for wide bandgap devices. Both JEITA and JEDEC have started efforts. JEDEC has formed a new committee, JC70, for GaN and SiC standardization. IRPS is the IEEE reliability conference where reliability physics started and resulted in the qualification procedures we use. Standards need a good technical foundation and an understanding of the applications, which is the focus of the 'WBG reliability synergies and standardization' workshop. By making researchers more aware, it will result in more synergies, better standards and common test equipment and procedures

Moderators

Dr. Sameh Khalil received his M.A.Sc and Ph.D. from the University of Toronto, Canada in Electrical and Computer Engineering in 1999 and 2003, respectively, where he experimentally introduced Lateral Super-Junction Power devices. He is currently a Lead Principal Engineer at Infineon Technologies, PMM Division, where he focuses on GaN Device Reliability assurance and Product Engineering Management and is the project manager of Infineon's Lead HV GaN product. He is currently active in industry-wide efforts for the standardization of GaN Device reliability as a co-chair of JEDEC's newly formed JC70.1.1 GaN Reliability Task Group (previously GaNSPEC Reliability DWG) and GaN Power Device roadmap as a co-chair of ITWR (the International Technology Roadmap of Wide Band-gap Power Semiconductors) GaN Device sub-committee. He was the technical program chair of the device track at WiPDA 2017.

Dr. Aivars Lelis, who received his Ph. D. in Reliability Engineering from the University of Maryland in 2011 and his M.S. degree in Electrical Engineering from the Johns Hopkins University in 2000, leads the Wide Bandgap Device Reliability Physics Team of the Power Conditioning Branch at the U.S. Army Research Laboratory in Adelphi, MD, with a focus on the device reliability physics of SiC and GaN MIS-based power devices, for high-temperature, high-efficiency power conversion and conditioning for advanced Army systems. He was a member of the steering committees for both the GaN Standards for Power Electronic Conversion (GaNSPEC) Devices Working Group (DWG) and SiCSPEC, and is presently the co-chair for the SiC reliability task group under JEDEC JC-70.2