2019 IRPS Conference Proceedings

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Intro

For 59 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world.

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Topics of Interest

SPECIAL FOCUS TOPICS

IRPS 2019 is Soliciting Increased Participation in Reliability for the Following Areas: Modeling of Circuit Reliability and Aging; Beyond CMOS – Reliability Issues in Neuromorphic Computing; Reliability Challenges in Automotive Electronics; and Advanced Packaging (2.5/3D)

Circuits, Products, and Systems

Circuit Reliability and Aging – Includes digital, mixed-signal, power and RF applications; design for reliability; variability-aware design, EDA tools and compact modeling

Product IC Reliability – Includes burn-in; defect detection; on-chip sensors; modeling

Consumer, System and Automotive Electronics Reliability – Includes smart phones; wearable devices; tablets; healthcare devices, automotive, space, communications, energy and computing/ networking; screening techniques; system monitoring; failure root cause determination; modeling methodologies; product qualification vs reliability

Soft Errors – Includes neutron and alpha particle SER; multi-bit SER/SEU; mitigation techniques; simulation

ESD and Latchup – Includes component and systemlevel ESD design; modeling and simulation

Packaging and 2.5D/3D Assembly – Includes chippackage interaction; fatigue; power dissipation issues; reliability of 2.5D and 3D IC packaging and TSV integration, interconnects, multichip modules

Reliability Testing – Includes reliability equipment, tools, and test methods

Neuromorphic Computing – Includes devices, circuits and systems for neuromorphic computing; degradation and instability of devices under neuromorphic design-imposed operation conditions

Materials, Processing, and Devices

Transistors – Includes hot carrier phenomena; BTI; RTN; advanced node scaling; variability; Ge and III-V channels

Gate and MOL Dielectrics – Includes TDDB modeling and reliability of novel gate and MOL dielectrics; modeling of progressive breakdown; gate dielectric reliability for III-V FETs

Beyond CMOS Devices – Includes reliability of tunnel FETs, transistors with 2D semiconductors (graphene, MoS2); ferroelectric and negative capacitance FETs; spintronics

Wide-Bandgap Semiconductors – Includes reliability of WBG-based power devices (GaN, SiC, Ga2O3)

Compound and Optoelectronic Devices – Includes reliability of III-V-based devices; optoelectronic devices; silicon photonics; far infrared detectors

Back-End Reliability – Includes electromigration; Joule heating; stress migration; low-k dielectric breakdown, ILD/IMD TDDB; MIM/MOM capacitors

Process Integration – Includes new process-related reliability issues; foundry reliability challenges

Failure Analysis – Includes evidence of new failure mechanisms; advances in failure analysis techniques

Memory Reliability – Includes DRAM and NVM; novel memory devices such as 3D Flash, STT MRAM and ReRAM

Photovoltaics – Includes reliability of solar cells in silicon, CdTe, CIGS, organics, multi-junctions, etc.

MEMS – Includes reliability of sensors and actuators; reliability testing; analysis & modeling; BioMEMS

Program

NOTE – For full Program, including Abstracts and Speaker information, view Appendix

VIDEOS – https://www.youtube.com/user/IEEEIRPS/videos

Keynote & Invited Speakers

IRPS Keynote 1: Abundant-Data Computing: The N3XT 1,000X

Professor Subhasish Mitra, Stanford University

Abstract:

Coming generations of information technology will process unprecedented amounts of loosely-structured data, including streaming video and audio, natural languages, real-time sensor readings, contextual environments, or even brain signals. The computation demands of these abundant-data applications, such as deep learning, far exceed the capabilities of today's electronics, and cannot be met by isolated improvements in transistor technologies, memories, or integrated circuit (IC) architectures alone. Transformative NanoSystems, which leverage salient features of emerging nanotechnologies to create new IC architectures, are required to deliver unprecedented performance and energy efficiency.

The N3XT (Nano-Engineered Computing Systems Technology) approach overcomes these challenges through recent advances across the computing stack: (a) new logic devices using nanomaterials such as one-dimensional carbon nanotubes (and two-dimensional semiconductors) for high performance and energy efficiency; (b) high-density non-volatile resistive memories; (c) ultra-dense (e.g., monolithic) three-dimensional integration of logic and memory with fine-grained connectivity; (d) new IC architectures for computation immersed in memory; and, (e) new materials technologies and their integration for efficient heat removal. In addition, special techniques to overcome imperfections, variations and reliability challenges in such logic and memory technologies are essential.

N3XT hardware prototypes represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual NanoSystems. Compared to conventional approaches, N3XT architectures promise to improve the system-level energy-delay-product of abundant-data applications significantly, in the range of three orders of magnitude. Such massive benefits enable new frontiers of applications for a wide range of computing systems, from embedded systems all the way to the cloud.

Biography:

Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University, where he directs the Stanford Robust Systems Group and co-leads the Computation focus area of the Stanford SystemX Alliance. He is also a faculty member of the Wu Tsai Neurosciences Institute at Stanford. Prof. Mitra holds the Carnot Chair of Excellence in Nanosystems at CEA-LETI in Grenoble, France. Before joining the Stanford faculty, he was a Principal Engineer at Intel Corporation.

Prof. Mitra's research interests range broadly across robust computing, nanosystems, VLSI design, validation, test and electronic design automation, and neurosciences. He, jointly with his students and collaborators, demonstrated the first carbon nanotube computer and the first three-dimensional nanosystem with computation immersed in data storage. These demonstrations received wide-spread recognitions (cover of NATURE, Research Highlight to the United States Congress by the National Science Foundation, highlight as "important, scientific breakthrough" by the BBC, Economist, EE Times, IEEE Spectrum, MIT Technology Review, National Public Radio, New York Times, Scientific American, Time, Wall Street Journal, Washington Post and numerous others worldwide). His earlier work on X-Compact test compression has been key to cost-effective manufacturing and high-quality testing of almost all electronic systems. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools.

Prof. Mitra's honors include the ACM SIGDA/IEEE CEDA A. Richard Newton Technical Impact Award in Electronic Design Automation (a test of time honor), the Semiconductor Research Corporation's Technical Excellence Award, the Intel Achievement Award (Intel's highest corporate honor), and the Presidential Early Career Award for Scientists and Engineers from the White House (the highest United States honor for early-career outstanding scientists and engineers). He and his students published several award-winning papers at major venues: ACM/IEEE Design Automation Conference, IEEE International Solid-State Circuits Conference, ACM/IEEE International Conference on Computer-Aided Design, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors "for being important to them during their time at Stanford."

IRPS Keynote 2: The Era of Hyperscaling in Electronics

Professor Suman Datta, University of Notre Dame

Abstract:

In the past five decades, the semiconductor industry has gone through two distinct eras of scaling: the geometric (or classical) scaling era and the equivalent (or effective) scaling era. As transistor and memory features approach 10 nanometer, it is apparent that room for further scaling in the horizontal direction is running out. In addition, the rise of data abundant computing is exacerbating the interconnect bottleneck that exists in conventional computing architecture between the compute cores and the memory blocks. In this talk, I will discuss how electronics is poised to enter a new, third, era of scaling – hyper-

scaling – in which resources are added in a flexible way when needed to meet the demands of data abundant workloads. This era will be driven by advances in extremely low power beyond-Boltzmann transistors, embedded non-volatile memories, hybrid devices with merged logic and memory functionalities, monolithic three-dimensional integration, and heterogeneous integration techniques.

Biography:

Suman Datta is the Frank M. Freimann Chair Professor of Engineering at the University of Notre Dame. Prior to that, he was a Professor of Electrical Engineering at The Pennsylvania State University, University Park, from 2007 to 2011. From 1999 till 2007, he was in the Advanced Transistor Group at Intel Corporation, Hillsboro, where he developed several generations of high-performance logic transistor technologies including high-k/metal gate, Tri-gate and non-silicon channel CMOS transistors. His research group focuses on emerging device concepts that support and enable new computational models. He is a recipient of the Intel Achievement Award (2003), the Intel Logic Technology Quality Award (2002), the Penn State Engineering Alumni Association (PSEAS) Outstanding Research Award (2012), the SEMI Award for North America (2012), IEEE Device Research Conference Best Paper Award (2010, 2011) and the PSEAS Premier Research Award (2015). He is a Fellow of IEEE and the National Academy of Inventors (NAI). He has published over 300 journal and refereed conference papers and holds 175 patents related to advanced semiconductors. He is the Director of a multi-university advanced microelectronics research center, called the ASCENT, funded by the Semiconductor Research Corporation (SRC) and the Defense Advanced Research Projects Agency (DARPA). He will serve as the Technical Program Chair of the 2019 IEEE International Electron Device Meeting (IEDM).

IEW Keynote: Radio-Frequency Interference in Wireless Devices

Professor Jun Fan, Missouri University of Science and Technology

Abstract:

A variety of wireless devices ranging from cell phones to smart hardware and IoT devices have emerged and will continue to develop rapidly, together with the emerging new technologies such as IoT and 5G wireless. While wireless communication enables convenient connections of the devices, it also makes them inherently vulnerable to electromagnetic interference. Any radio frequency (RF) antenna used as a radio receiver can easily pick up the unintended electromagnetic noise from digital circuits, resulting in RF interference. Unlike conventional EMI issues, RF interference usually deals with noise at a much lower level and does not have standards or regulations to follow. In this talk, fundamentals of RF interference issues in wireless devices will be introduced. Challenges and progress in noise source characterization, understanding of coupling mechanisms, and mitigation solutions will be discussed and illustrated using real-world examples. RF interference and ESD are two dominant design issues in wireless devices. It will be shown that ESD protection circuits could be a source for RF interference. Modulation and intermodulation generated in these circuits could result in the noise components falling into the receiver band and thus degrade the performance of the receiver. Effort in modeling and characterizing this problem will be proposed.

Biography:

Jun Fan received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently the Cynthia Tang Missouri Distinguished Professor in Computer Engineering and Director of the Missouri S&T EMC Laboratory. Dr. Fan also serves as the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. In the IEEE EMC Society, Dr. Fan served as the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, the Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He currently is an associate editor for the IEEE Transactions on Electromagnetic Compatibility and IEEE EMC Magazine. Dr. Fan received an IEEE EMC Society Technical Achievement Award in August 2009. He is an IEEE fellow.

IEW Invited Talk 1: System Level Testing of Components

Doctor Kathy Muhonen, Qorvo

Abstract:

This Invited Talk will explain in detail, recommendations for testing components to the IEC 61000-4-2 standard. While components are not completed systems, OEMs still ask their vendors to test components outside the system according to this standard. There is no real guidance for this in the IEC 61000-4-2 standard and results are not repeatable. This talk aims to give guidance to those who have to conduct the test regardless. The talk will also review the similarities and differences between testing to the IEC 61000-4-2 standard and the HMM standard practice. The hurdles and pitfalls to system level testing is shown and best

practices are outlined. This talk also reviews several controlled experiments to determine the amount of variability that is typical in this type of test. One of the experiments is a round robin study with 10 labs and four types of components. Its findings will be summarized. A second experiment was conducted with one part, one operator and different equipment. Finally, a third experiment looked at changing different parameters of the test set up too see if the results would be impacted.

Biography:

Doctor Kathleen Muhonen is currently an ESD Engineer at Qorvo in Greensboro, NC. She is involved in ESD on-chip protection for mobile and millimeter wave applications. She is also heavily involved with system level testing and helped standardize IEC testing of RF components. Kathleen is heavily involved in ESD instrumentation for better ESD characterization of clamps and materials. Previously she was responsible for RF characterization and model support for SOI and Gallium Arsenide technologies for power amplifiers, switches and antenna tuners. She has also done extensive work on developing state of the art harmonic characterization of semiconductors, improving de-embedding techniques of large scale switches and development of an Envelope Tracking Load-pull characterization bench. Kathleen's previous experience includes assistant professor at Penn State Erie, linearization design for base stations at Hewlett Packard, power amplifier design at Lockheed Martin and GE Aerospace. Kathleen has served as a member of the ESD Association and sat on all device testing standards committees, including serving as past TLP and HMM workgroup chairs. She has also served on the Board of Directors as curricular implementation chair. Her involvement in round robin testing for TLP, VF-TLP and IEC Component Testing has generated several papers presented at the EOS/ESD Symposium over the last decade. Kathleen received her BSEE degree from Michigan Technological University in 91, a MSEE from Syracuse University in 94 and a Ph.D.EE from Penn State University in 99.

IEW Invited Talk 2: Cost-Efficient Methods for Latch-up Prevention in CMOS Integrated Circuits

Professor Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University, Taiwan

Abstract:

In CMOS ICs, latchup is formed by the parasitic p-n-p-n structure between power lines of VDD and VSS. Such parasitic p-n-p-n structure is inherent in the bulk CMOS technology. The parasitic p-n-p-n structure could be accidentally triggered on by external glitches or transient noises to generate a low-impedance path between the power lines. When latchup was triggered on, CMOS ICs were often burned out seriously by the latchup-generated heat. Therefore, latchup presentation is one of major reliability topics in CMOS ICs, especially realized in bulk CMOS technology. In this talk, a brief background of latchup in CMOS ICs is given. The methodology to extract compact layout rules used to prevent latchup occurrence on the I/O cells is introduced. Even if the I/O cells of a CMOS IC are free from latchup, the core circuits in the CMOS ICs will be still sensitive to latchup issue. The reasons to cause latchup occurrence on the core circuits are explained, including the transient-induced latchup during system-level ESD or FET testing. To further improve latchup immunity of CMOS ICs but without enlarging the spacing/distance in the chip layout, a novel concept of "active guard ring" and its corresponding circuit implementation will be addressed. Additional latchup events on the circuits with different power domains, such as HV and LV blocks, I/O PMOS and core PMOS, PMOS and varactor, will be discussed. Finally, the low holding voltage of the on-chip ESD protection device used in the power-rail ESD clamp may also cause latchup-like failure. The solutions to overcome such latchup-like issue, especially in HV applications, will be mentioned. Latchup prevention in CMOS ICs is not only the process issue but also highly dependent to the layout and design issue, which has been an important topic that the IC designers need to know.

Biography:

Ming-Dou Ker received the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1993. He worked as the Department Manager with the VLSI Design Division, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. During 2012-2015, he was the Dean of the College of Photonics, National Chiao-Tung University (NCTU), Taiwan. Now, he has been the Distinguished Professor in the Institute of Electronics, National Chiao-Tung University, Taiwan. Currently, he is also serving as the Director of the Biomedical Electronics Translational Research Center (BETRC), NCTU, working on biomedical electronics translational projects.

In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 560 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents. He had been invited to teach and/or to consult the reliability and quality design by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include the circuits and systems for biomedical applications, as well as circuit-related reliability issue.

Professor Ker has served as member of the Technical Program Committee and the Session Chair of numerous international conferences for many years, including IEEE Symposium on VLSI Circuits and IEEE International Solid-State Circuits Conference. He ever served as the Associate Editor for the IEEE Transactions on VLSI Systems, 2006-2007. He served as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2018). He was

the Founding President of Taiwan ESD Association. Currently, he is serving as an Editor for the IEEE Transactions on Device and Materials Reliability, and an Associate Editor for the IEEE Transactions on Biomedical Circuits and Systems. Professor Ker has been a Fellow of the IEEE since 2008.

2019 IRPS Distinguished Lecturer

Life, turmoil, and abundance in Monterey Bay: how we study it and what sponges have to do with it

Dr. Amanda S. Kahn, Monterey Bay Aquarium Research Institute

Abstract:

Monterey Bay is a dynamic region known for its natural features, tide pools, beaches, and the abundant marine life it supports. This talk will begin by introducing the violent forces – earthquakes, landslides, volcanoes, and pounding surf – that have shaped the California coastline (and specifically Monterey Bay). It will then focus on how diverse ecosystems – on land and in the ocean – are supported by the turbulent ocean. The second half of the talk will focus on how animals make a living in one of the most extreme environments on the planet: the deep ocean. The deep seafloor makes up 80% of the planet's surface and is readily accessible in Monterey Bay due to the Monterey Submarine Canyon, although accessing it requires advanced technology and approaches. MBARI specializes in developing technology to study the deep ocean such as hydraulically powered remotely operated vehicles powered by kilometers-long fiber optic cables, autonomous underwater vehicles capable of surveying the seafloor for weeks on end, and sensors designed to withstand near freezing temperatures and the weight of over a thousand meters of water compressing them.

Seafloor communities in these deep habitats cannot rely on locally produced food as light cannot penetrate to fuel photosynthesis. Deep-sea communities thus rely mainly on imported nutrients, either as material sinking from the surface or arriving via lateral currents. The food that arrives is often limiting, yet in some locations, dense communities manage to persist and even flourish. Suspension feeders – animals that capture food particles suspended in the water column—are important vectors for transferring food energy from the water column into the benthic food web. Dr. Kahn's research focuses on one group of suspension feeders that is highly successful at surviving in the deep sea: the sponges (Phylum Porifera). Through their feeding activity, sponges act as oases of nutrients in the food-poor deep ocean.

Biography:

Dr. Kahn's research broadly focuses on the movement of food energy (carbon) within and between ecosystems, and on how animals facilitate this movement – especially in the food-starved deep sea. Her research has involved studies of deep-sea sponges from extinct underwater volcanoes off the coast of California, the unique glass sponge reefs of western Canada, and 'cheese-bottom' sponge grounds in the fjords of Norway. Dr. Kahn received her PhD in Ecology from the University of Alberta in Edmonton, Alberta, Canada. She completed postdoctoral fellowships studying sponges in the deep north Pacific and oceanography of the North Atlantic, and is now currently a postdoctoral fellow in the benthic ecology lab at the Monterey Bay Aquarium Research Institute. She is preparing to transition to Moss Landing Marine Laboratories to begin as an assistant professor in invertebrate ecology in August this year.

Tutorials

- FEOL Reliability-Transistor reliability in the FinFET era I Stephen M. Ramey (Intel)
- Compact, Efficient, and Precise Characterization of Circuit Aging Using Silicon Odometers I C. H. Kim (Seoul National University)
- Low-K dielectric Reliability Challenges with Technology Scaling I Rahim Kasim (Intel)
- SER-Radiation Hardening by Design of Digital Circuits I K. Kobayashi (Kyoto Institute of Technology)
- Practical Aspects of Latchup for Low Voltage CMOS: Design Rules, Layout Floor Planning, and Test I Scott Ruth (NXP)
- FDSOI Technology and Dynamic Body Bias Compensation to Enable Next Generation AI/IoT and Automotive Products - An industrial perspective & Dynamic aging compensation - the next key enabler of automotive products I V. Huard (Dolphin Integration) I Joerg Winkler (GLOBALFOUNDRIES)
- Hardware opportunities for Deep Neural Networks and Artificial Intelligence I Geoffrey W. Burr (IBM)
- An Integrated Dependability Framework for System Design and Architecture I Scott Hareland (Medtronic)
- BTI-A NBTI Reliability Framework from Atoms to Processors I S. Mahapatra (IIT)
- SiC-SiC Power Devices: Overview, Defect Electronics, and Reliability I T. Kimoto (Kyoto Univ.)
- Automotive-Statistical implementations for reliability assessment in automotive manufacturing I Cristiano Capasso (GF)
- Memory-Reliability issues of NAND Flash memory I Riichiro Shirota (NCTU)
- The Emerging Challenge of and Biomimetic Solutions to Self-heating in FINFET, ETSOI, Nanosheet, & Surround-gate

Transistors: A Material, Device and System Perspective I A. Alam (Purdue Univ.)

- Failure modes and mechanisms of GaN HEMTs for microwave an power applications I Enrico Zanoni (Univ. Padova)
- DFT/DFR-Testing of Automotive ICs I Nilanjan Mukherjee (Mentor Graphics)
- Memory-Device Challenges and Opportunities for ReRAM I Kensuke Ota (Toshiba Memory)
- PID-Plasma process charging induced damage (PID) of MOS devices I Andreas Martin (Infineon Technolgies AG)
- FA-Defect Localization Technique Selection for Reliability and Functional Fails I Greg Johnson (Carl Zeiss)
- Circuit Reliability-Closing the gap between Reliability Physics, EDA and Circuit Design I Georgios Konstadinidis (Google)
- CPI-Advanced Packaging Reliability I Kang Wook Lee (SK Hynix)

Workshops

- FinFET Regency I-III I Souvik Mahapatra (IIT) I Chetan Prasad (Intel)
- BEOL & CPI I Jeff Gambino (ON Semi) I Zhuojie (George) Wu (GF)
- DFR/DFRT I Nilanjan Mukherjee (Mentor Graphics) I Vincent Huard (Dolphin Integration)
- GaN/GaN on Si I Sandeep Bahl (TI) I Sameh Khalil (Infineon)
- 3D NAND I Xiaoyu Yang (Western Digital Corp) I Wei-Chen Chen (Macronix)
- System Reliability I Scott Hareland (Medtronic)
- UTB-SOI FET I Tanya Nigam (GF) I Vincent Huard (Dolphin Integration)
- TSV & Advanced packaging I Kristof Croes (imec) I Kangwook Lee (SK hynix)
- Rel. Simulation I Georgios Konstadinidis (Google) I James Tschanz (Intel)
- SiC I Nando Kaminski (Univ. of Bremen) I Anant Agarwal (The Ohio State Univ.)
- STT-MRAM I Tetsuo Endoh (Tohoku Univ.) I Junghyuk Lee (Samsung)
- Neuromorphic I Gennadi Bersuker (Aerospace Corp) I Pey Kin Leong (SUTD)

Year In Review

- YIR 1- NBTI/PBTI: State-of-the-art I Tibor Grasser, TU Wien
- YIR 2 - Metallization reliability I James Lloyd, SUNY Polytechnic Institute
- YIR 3 - Functional Safety, reliability, availability I Riccardo Mariani, Intel Corporation Italia

Highlighted Papers

See Appendix – Full Program pg. 127.

Poster Session

See Appendix – Full Program for Poster Sessions

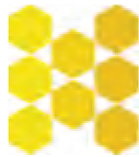
Exhibits & Exhibit Events

Exhibits are an integral part of the International Reliability Physics Symposium. Don't miss this opportunity to showcase your company's products and services.

For 57 years, the International Reliability Physics Symposium has been the premier forum for presentation of new work on the physics of failure mechanisms in electronic and microelectronic devices. We invite you to participate in the Exhibition and showcase your products and services. The Exhibition will be open to all IRPS attendees as well as qualified Exhibit Only participants.

Over 400 Industry Professionals are Expected in Monterey!

IRPS gratefully acknowledges the generous support of our 2021 exhibitors:



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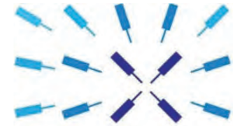

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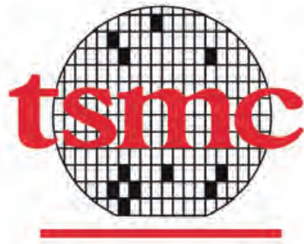

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Appendix - Abstracts, Bios & Technical Program

PREFACE

On behalf of the Management Committee of the IEEE International Reliability Physics Symposium (IRPS) and the IRPS Board of Directors, it is my pleasure to welcome you to IRPS 2019.

For 57 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure and the application environment.

This year we are co-located with IEW (International ESD Workshop). As an IRPS attendee, you are welcome to join your colleagues for their keynote and invited talks, and to discuss the latest ESD research during the joint Poster Reception on Wednesday evening.

The 2019 Technical Program has 107 platform presentations, consisting of 8 invited talks and 3 Focus Sessions: Wide Band-Gap devices, Neuromorphic computing, and Electronic Design Automation reliability modeling. There are 74 IRPS posters and 14 IEW posters. The symposium starts with two days of Tutorials covering introductory and advanced topics in reliability physics. We round out the program with a reliability Year-In-Review on Monday evening, and lively Workshop discussions with food and beer on Tuesday evening.

In addition, there is an equipment exhibit during the week where you can discuss your specific needs as a reliability researcher with company representatives.

The symposium is the result of the dedication and tireless efforts of many individuals. I would like to thank all the authors, speakers, presenters, reviewers, workshop moderators, exhibitors, and corporate patrons for making the symposium strong and successful. I also wish to thank my management committee, our consultants and the Board of Directors for their support.

Every year, we strive to organize a symposium that is technically strong while offering a great attendee experience. We look forward to your feedback so that we can continue to grow. Please take the time to fill out the online surveys or discuss ideas you have with the IRPS management committee throughout the week.

Welcome to the symposium and I hope it will be a memorable experience for you!

Mark Porter
2019 IEEE IRPS General Chair

2019 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

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Mark Your Calendar to Attend IRPS 2020!

IRPS 2020 will be held March 29 through April 2, 2020 in Dallas TX at the Hilton DFW Lakes Executive Conference Center. A lively symposium is being planned, including keynote talks, poster session, tutorials, and a strong technical program.

Please consider submitting an abstract. Abstracts are solicited in all areas of microelectronics reliability, from the physics of device and materials wear-out to circuit and system design-for-reliability. Of special interest are works in the areas of Wide-Bandgap Semiconductor Devices, Circuit and Electronic Systems, Advanced CMOS Nodes, Beyond CMOS Devices, Emerging Memory Technologies and Electrostatic Discharge.

Abstracts must be submitted by October 2019.

Visit **irps.org** for information regarding the abstract submission process or to register for the conference.

Feedback regarding the 2019 IRPS will allow us to plan a 2020 symposium that best meets its attendees' needs. Please complete the attendee surveys.

Gaudenzio Meneghesso
2020 IEEE IRPS General Chair

Charlie Slayman
2020 IEEE IRPS Technical Program Chair

Sunday Tutorial

TS1.1 - Transistor reliability in the FinFET era - *Steve Ramey / Intel*

With the evolution to FinFET-style transistors, there are new features that modulate traditional reliability mechanisms. For example, the vertical sidewalls are typically <110> crystal orientation, which can influence oxide quality and trap behavior. Also, in Tri-gate devices, there are corner effects that can come into play. This tutorial endeavors to provide a review of all transistor reliability mechanisms and highlight interactions associated with three-dimensional transistors. The tutorial begins with a description of transistor reliability physics and electrical behavior. It then reviews the standard reliability mechanisms such as TDDB, BTI and hot carrier, especially in relation to the Tri-gate device. Additional effects are also detailed, such as local self-heating, SILC, and variation. Throughout, examples will be shown from various Tri-gate process technologies, highlighting the impact of continued technology scaling.

Steve Ramey manages the front-end reliability group in Intel's Technology Development Quality and Reliability organization and has helped develop the 90nm through 7nm process technologies. He received his Ph.D. in electrical engineering from Arizona State University, M.S. in electrical engineering from University of Nevada, Las Vegas, and B.S. in Physics from Carnegie Mellon University. He has authored/coauthored more than 50 publications on reliability, device modeling, process development, metrology, and photovoltaic devices.

TS1.2 – Low-K dielectric Reliability Challenges with Technology Scaling - *Rahim Kasim / Intel Corporation*

Technology scaling introduces new challenges for interconnect reliability assurgent from the need for

improved RC as dimensions shrink. Innovative process integration schemes that fully utilize the benefit of low-K dielectric without decreasing reliability margin are crucial to the successful certification of a leading edge processes. The combination of low-K dielectrics and dimensional scaling significantly increases the interconnect reliability risk for both intra-layer and inter-layer dielectrics. Additional process optimizations using novel patterning schemes extends Reliability challenges beyond intrinsic regime and introduces process variability as a consideration for dielectric breakdown characterization and product qualification. This Tutorial will primarily focus on TDDB (Time dependent dielectric breakdown) characterization of low-K dielectrics, breakdown physics, acceleration models and key Reliability challenges at MOL and BEOL.

Rahim Kasim is Reliability Manager in Intel's Logic Technology Development Group working primarily on MOL/BEOL reliability across 14nm, 10nm and 7nm Technology nodes. He joined Intel in 2005 after receiving Ph.D. and M.S degrees in Electrical Engineering from Arizona State University. His research interests includes BEOL/MOL dielectric Reliability and Interconnect Reliability.

TS1.3 - Practical Aspects of Latchup for Low Voltage CMOS: Design Rules, Layout Floor Planning, and Test - *Scott Ruth / NXP Semiconductors*
The goal of this tutorial is to cover various aspects of aspects of latchup that are encountered by individuals in the semiconductor industry in a way that provides a common understanding of the phenomenon and the limitations and nuances of test and prevention measures. From a design perspective, layout floor-planning, design rules, and EDA checks will be covered. From a test perspective, standard DC latch-up testing as well as some discussion of transient latch-up testing will be covered. Finally, real world latch-up failures and diagnoses will be presented.

Scott Ruth joined NXP Semiconductors in 2007 and is currently a staff engineer in the Automotive Microcontrollers and Processers Group in Austin, Texas, responsible for ESD protection design for advanced CMOS processes. Prior to joining NXP Scott worked at Philips Semiconductors for 8 years in various capacities in ESD and latchup qualification, characterization, and design. From 2004-2007 Scott was the ESD technical lead from NXP in the Crolles2 Alliance, with partners ST Microelectronics and Freescale Semiconductor. Scott received a B.S. degree in Physics from the University of California at Davis and a M.S. EE from the University of Colorado at Boulder.

TS1.4 - Hardware opportunities for Deep Neural Networks and Artificial Intelligence - ***Geoffrey W. Burr / IBM Research — Almaden***
For more than 50 years, the capabilities of Von Neumann-style information processing systems improved tremendously, mostly thanks to Dennard's Law: the amazing realization that each generation of scaled-down transistors could in fact be consistently better, in terms of power and speed, than the previous generation. But now that we find ourselves in the

post-Dennard's Law era, attention is turning to computing approaches that are not as dependent on engineering billions of devices that have to work absolutely perfectly. One such approach is to move towards Non-Von Neumann algorithms, and in particular, to Deep Neural Networks (DNNs) and other Artificial Intelligence (AI) architectures motivated by the human brain.
In this tutorial, I will discuss the challenges and review recent progress towards hardware implementation and acceleration of such brain-inspired computing architectures. This progress ranges from systems that combine conventional CMOS devices in different and unconventional ways, to systems built around emerging NVM (Non-Volatile Memory) devices; and from systems designed to accelerate conventional DNNs through hardware innovation, to systems that seek to transcend the known limitations of current DNN algorithms (such as the requirement for batch-based learning using vast datasets of static and labeled data).

Geoffrey W. Burr received his Ph.D. in Electrical Engineering from the California Institute of Technology in 1996. Since that time, Dr. Burr has worked at IBM Research--Almaden in San Jose, California, where he is currently a Principal Research Staff Member. He has worked in a number of diverse areas, including holographic data storage, photon echoes, computational electromagnetics, nanophotonics, computational lithography, phase-change memory, storage class memory, and novel access devices based on Mixed-Ionic-Electronic-Conduction (MIEC) materials. Dr. Burr's current research interests include non-volatile memory and cognitive computing. An IEEE Senior Member, Geoff is also a member of MRS,

SPIE, OSA, Tau Beta Pi, Eta Kappa Nu, and the Institute of Physics (IOP).

TS2.1 - Compact, Efficient, and Precise Characterization of Circuit Aging Using Silicon Odometers - *Chris H. Kim / Seoul National University*
Since 2006, my group has been developing specialized circuits called "Silicon Odometers" for accurately characterizing circuit aging effects. The aging and noise mechanisms we target range include bias temperature instability, hot carrier injection, time-dependent dielectric breakdown, random telegraph noise, and electromigration. In the first part of this talk, I will give an overview of our past odometer designs and introduce odometer circuits currently being designed in my group. Radiation effects in logic gates and flip-flops have not received adequate attention due to the difficulty in collecting high-quality radiation data. In the second part of this talk, I will introduce test circuits designed by my group in FinFET technology for characterizing soft errors in logic circuits.

Chris H. Kim received his B.S. and M.S. degrees from Seoul National University and a Ph.D. degree from Purdue University. He started his academic career in 2004 at the University of Minnesota and is currently a faculty at Seoul National University. Prof. Kim is the recipient of the University of Minnesota Taylor Award for Distinguished Research, Semiconductor Research Corporation (SRC) Technical Excellence Award for his "Silicon Odometer" research, Council of Graduate Students Outstanding Faculty Award, NSF CAREER Award, Mcknight Foundation Land-Grant Professorship, 3M Non- Tenured Faculty Award, DAC/ISSCC Student Design Contest Award (2 times), IBM Faculty Partnership Award (3 times), IEEE Circuits and Systems Society Outstanding Young Author Award, the ICCAD Ten Year Retrospective

Most Influential Paper Award, ISLPED Low Power Design Contest Award (4 times), and ISLPED Best Paper Award (2 times). His group has expertise in digital, mixed-signal, and memory IC design, with special emphasis on circuit reliability, hardware security, memory circuits, radiation effects, time-based circuits, and beyond-CMOS computing. He is an IEEE fellow.

TS2.2 - Radiation Hardening by Design of Digital Circuits - *Kazutoshi Kobayashi / Kyoto Institute of Technology*

Single events by alpha particles and neutrons on the terrestrial region threaten safety, reliability and serviceability of semiconductor devices on which our daily life highly depends on. Radiation hardening by design must be taken into account for mission critical applications such as autonomous driving, aerospace and so on. This tutorial will provide an introduction of single events on digital circuits to cause a single event upset (SEU) on storage cells such as SRAMs, latches and flip-flops. Then several radiation-hardening-by-design (RHBD) techniques will be introduced to mitigate SEU including multimodular structures applicable to both of bulk and SOI and stacking structures effective to SOI.

Kazutoshi Kobayashi received his B.E., M.E. and Ph. D. in Electronic Engineering from Kyoto University, Japan in 1991, 1993, 1999, respectively. Starting as an Assistant Professor in 1993, he was promoted to associate professor in the Graduate School of Informatics, Kyoto University, and stayed in that position until 2009. For two years during this time, he acted as associate professor of VLSI Design and Education Center (VDEC) at the University of Tokyo. Since 2009, he has been a professor at Kyoto Institute of Technology. While in the past he focused on reconfigurable architectures utilizing device variations,

his current research interest is in improving the reliability (Soft Errors, Bias Temperature Instability and Plasma Induced Damage) of current and future VLSIs. He started a research related to gate drivers for power transistors since 2013. He was the recipient of the IEICE best paper award in 2009 and the IRPS best poster award in 2013.

TS2.3 - Dynamic aging compensation - the next key enabler of automotive products - *Vincent Huard / SOITEC*

The automotive products, driven by ADAS needs, are now moving to very advanced CMOS nodes. This trend is helping a lot from soft errors perspective with a reduced architectural cost to achieve required FIT rate. But, on another hand, this trend is also generating enhanced risk with respect to end-of-life electrical wearout. Though such mechanisms can be managed statically with larger design margins, this is now often not possible in a context where leakage must also be reduced to support even higher junction temperatures. New solutions as dynamic aging compensation have been considered for the last decade as a research topic. But some groups are now moving towards an industrial usage of such dynamic aging compensation. This tutorial will guide you through the different research findings over the last decade and will give you clues on the most advanced solutions that will come in the next generation of automotive products.

https://www.linkedin.com/in/vincent-huard-549a622

TS2.4 - An Integrated Dependability Framework for System Design and Architecture - *Scott A. Hareland / Medtronic*

The reliability of a system is much more than the cumulative reliability of all of the parts. This tutorial will focus on a dependability framework that provides guidance and analysis methods for system engineers and architects for the prevention, removal, and tolerance to faults in a system. Methods and tools

normally used during system architecture and development can be coupled with reliability analysis methods in the dependability framework to have significant improvements in system reliability, safety, and availability while maintaining realistic design efforts and expectations. While a focus on faults, physics of failure, and methods to improve component and product reliability will always be needed and studied by reliability engineers, this dependability framework drives early and top-down focus on the fundamental causes of faults, how those faults propagate into system failures, and how system design decisions can often provide more elegant and cost-effective solutions for achieving a dependable system.

Scott Hareland is a Medtronic Technical Fellow and a Distinguished Systems Engineer in the Neurological Restorative Therapies Group in Minneapolis, MN. Previously, he was the lead system architect on cryoablation-based surgical platforms in Medtronic's Cardiac Rhythm and Heart Failure Division. In addition, he has over ten years of experience in implantable cardiac devices and leads including sensor based systems, the industry's first implantable pacemaker designed for MRI environments, and numerous fault-tolerant design concepts. Prior to Medtronic, he was a reliability and device engineer at Intel Corporation working on advanced 3D transistor designs, CMOS integration of functional high-k dielectrics and complementary metal gates, and research on advanced dielectrics and soft error effects. He received the B.S.E.E. degree from Rice University and the M.S.E. and Ph.D. degrees from the University of Texas at Austin. He is a member of Phi Beta Kappa, Tau Beta Pi, and Eta Kappa Nu.

Monday Tutorial

TM1.1 - A NBTI Reliability Framework from Atoms to Processors - *Souvik Mahapatra / IIT Bombay*

Negative Bias Temperature Instability (NBTI) continues to remain as a serious reliability concern in HKMG FinFETs and impacts the long term performance of CMOS circuits. It is therefore important to develop a modeling framework to estimate the NBTI limited end of life degradation in devices and the corresponding degradation in circuits for various mission profiles. Such a framework can be added to the existing Design Technology Co-Optimization (DTCO) flows for concurrent optimization of performance, power, area and aging (PPAA) of advanced CMOS chips.

In this presentation a NBTI reliability framework will be described that can estimate the impact of gate stack processes (atoms) and MOSFET architectures on circuit reliability. A BTI analysis tool will be presented that can analyse experimental data across various technologies and processes. TCAD implementation of the framework will be shown to study FinFET scaling and impact of Gate All Around (GAA) NSFET architectures having different channel materials, and check quantum confinement and strain effects on NBTI. A compact model that can handle circuit degradation under arbitrary gate activity will be discussed, with some examples of circuit degradation under actual workload versus worst case DC cases. A simulation flow will be presented to link device and RO degradation to that of processors, which includes detailed characterization of standard cells under NBTI. Several benchmark circuits will be analyzed. Finally, the statistical aspect of device-level variability and variable reliability will be addressed, and connections will be made to estimate the variability associated with SRAM performance degradation.

Souvik Mahapatra received his PhD in Electrical Engineering from IIT Bombay, Mumbai, India in 1999. During 2000-01 he was with Bell Labs, Lucent Technologies, Murray Hill, NJ, USA. Since 2002 he is with the Electrical Engineering department at IIT Bombay and presently a full professor. His research interests are CMOS scaling, reliability and memory devices. He has published over 150 papers in peer reviewed journals and conferences and delivered invited talks in major international conferences including IEEE IEDM and IRPS. He is a fellow of IEEE (Institute of Electrical and Electronics Engineers), INAE (Indian National Academy of Engineering) and IASc (Indian Academy of Sciences), and a distinguished lecturer of IEEE EDS (Electron Devices Society).

TM1.2 - The Emerging Challenge of and Biomimetic Solutions to Self-heating in FINFET, ETSOI, Nanosheet, & Surround-gate Transistors: A Material, Device and System Perspective -
Muhammad A. Alam / Purdue University

By early 2000s, many researchers would begin their talks with an iconic cartoon that compared the power dissipation of an IC, with that of a rocket nozzle and the Sun. The message was clear: the voltage must be scaled to keep power-dissipation at bay. Fast forward to 2017– the tyranny of short channel effects at the sub 32 nm nodes has led to the development of FINFET and ETSOI technologies, with Si Nanosheet-FET and gate-all-around III-V transistors on the horizon. The short channel effects are controlled, but at the expense of additional self-heating of the system. Stacks of materials (many poor thermal conductors) now surround the very hot channel to make the bad situation worse. In this tutorial, I will explain how self-heating redefines and conflates the traditional notions of performance and reliability of transistors and frontend and backend reliability of modern ICs. I will also explain how high-frequency operation and novel

biomimetic heat-dissipation strategies (e.g. inverse opal, 3D printing, etc.) may help manage this emerging performance and reliability challenge for sub-20nm technologies.

Muhammad A. Alam holds the Jai N. Gupta professorship at Purdue University, where his research focuses on the physics and technology of semiconductor devices. From 1995 to 2003, he was with Bell Laboratories, Murray Hill, NJ. Since joining Purdue in 2004, Dr. Alam has published over 300 papers and he is among the top-20 contributors on diverse topics involving transistors, reliability, biosensors, and solar cells. He is a fellow of IEEE, APS, and AAAS. His awards include the 2006 IEEE Kiyo Tomiyasu Medal for "Contributions to device technology", 2015 SRC Technical Excellence Award for "Fundamental contributions to reliability physics", and 2018 IEEE EDS Award for "For educating, inspiring, and mentoring students and electron device professionals around the world". More than 350,000 students worldwide have learned some aspect of semiconductor devices from his web-enabled courses.

TM1.3 - Plasma process charging induced damage (PID) of MOS devices - *Andreas Martin / Infineon Technologies AG*

This tutorial will present a short introduction to the field of PID followed by a detailed overview of PID reliability characterization methods including stress, test structure concepts and data analysis techniques.

Over 25 years of research in the field of PID would lead to the assumption that required test structures and stress methods are well defined. However, this is not the case and the analysis of PID stress data can discover large obstacles. Further, different circuit application areas for MOS devices require different stress methods. For

complex state of the art process nodes with various FET dielectric thicknesses and device types and many metal layers the number of qualification test structures can easily go up to 1000. An applied characterization method requires fast reliability stresses for the detection of PID. This is described in the tutorial as well as a suitable additional stress for a quantification of the PID event. Recent publications show the effectiveness of this method. Additionally, the tutorial focuses on the test structure design, which can have a significant effect on the PID stress results. Inappropriate layout can either introduce severe damage which is not relevant for a product or suppress relevant plasma damage leaving a dangerous blind spot in product design. Various product relevant test structures and stresses are reviewed for a complete characterization of PID during process qualification. The lack of a comprehensive PID standard in the reliability community leaves many used qualification methods with obvious gaps. Pit falls of the characterization methods and test structures as well as the relevant PID literature will be presented. Simple PID protection schemes will also be discussed which are relevant for test structure and product design.
The tutorial is aimed towards reliability engineers with some basic reliability experience in the field. Experts will enjoy the detailed case stories with "strange" PID data. A lot of hands-on material is presented which can be implemented at your work place.

Andreas Martin received his M.Eng.Sc. in Electrical and Electronic Engineering from the Technical University of Darmstadt, Germany, in 1992. After six years in the silicon technology characterisation group of the research center "Tyndall Institute" (former NMRC), Cork, Ireland he started working for the central Reliability Methodology department of Infineon Technologies AG in Munich, Germany in the

field of fWLR Monitoring. He is involved in advanced and novel test structure design, development of new stress methods and data analysis techniques on the topics: dielectrics, plasma induced damage, metallisation and device degradation topics for a wide range of processing nodes. He is responsible for the PID process qualification and plasma charging design manual rules at Infineon. He has published and co-authored numerous papers/presentations, given tutorials and invited talks at various conferences and served in committees of the IEEE IRW, IEEE IRPS, ESREF and of the "Workshop on Dielectrics in Microelectronics" (WoDiM) for many years. He has published some patents and was involved in paper reviews for several journals. He is a senior member of the IEEE, Infineon's alternate of the JEDEC-subcommittee 14.2, member of the IEC WLR-workgroup TC 47 and co-chair of the German ITG-group 8.5.6 on "WLR and reliability simulations".

TM2.1 - SiC Power Devices: Overview, Defect Electronics, and Reliability - *Tsunenobu Kimoto / Kyoto University*

Through recent progress in silicon carbide (SiC) growth and device technologies, 600–3300 V SiC power MOSFETs and Schottky barrier diodes have been commercialized, demonstrating significant reduction of power loss in various power systems. However, both bulk and interface defects are present in SiC devices, affecting the performance and reliability of SiC power devices. Such defects include stacking faults, threading and basal-plane dislocations, point defects (carbon vacancy, etc.), MOS interface states, and oxide traps. In this tutorial, an overview and reliability issues of SiC power devices are presented together with current physical understanding of defect behaviors. Impacts of various defects on SiC power devices, typical degradation phenomena, and their reduction are reviewed. Methodology of assessing

defects in SiC epitaxial wafers and devices is also discussed.

Tsunenobu Kimoto received the B.E. and M.E. degrees in Electrical Engineering from Kyoto University, Japan, in 1986 and 1988, respectively. He joined Sumitomo Electric Industries, LTD in 1988. In 1990, he started his academic career as an Assistant Professor at Kyoto University, and received the Ph.D. degree from Kyoto University in 1996. >From 1996 to 1997, he was a visiting scientist at Linköping University, Sweden, and since 2006 he has been a Professor at Department of Electronic Science and Engineering, Kyoto University.
His main research activity includes SiC (growth, characterization, process technology, power devices, and high-temperature devices), GaN-based power devices, nano-scale Si and Ge devices, and oxide materials for resistive switching memories. He is an IEEE Fellow and a JSAP Fellow.

TM2.2 - Failure modes and mechanisms of GaN HEMTs for microwave an power applications - *Enrico Zanoni, Carlo De Santi, Matteo Meneghini, Gaudenzio Meneghesso / University of Padova*

Relevance of GaN High Electron Mobility Transistors for communication systems, avionics, energy management and control is becoming increasingly important. On one hand 5G systems will require power amplifiers with high efficiencies, increased bandwidth and operating frequencies; on the other, an increased demand is expected for high-voltage power converters and control systems with efficiencies close to 100%, higher frequency and temperature of operation, increased compactness and robustness. As device scaling and higher voltages, with consequent increase of electric field, represent a potential threat for the reliability of these devices, research on GaN HEMT failure physics has been intensified recent years. This

tutorial will review failure modes and mechanisms of GaN HEMTs, including mechanisms leading to frequency dispersion effects, current collapse and dynamic Ron increase, mechanisms affecting the gate Schottky contact, time-dependent breakdown phenomena, hot-electron degradation related to device dynamic operation in microwave or switching systems

Enrico Zanoni is professor of Microelectronics at the Department of Information Engineering of the University of Padova and a IEEE Fellow. He and his group are involved in research on the characterization, modeling and reliability of Gallium Nitride electronic and optoelectronic devices since 1999. At the University of Padova he contributed to establish a microelectronics research group involved in CMOS analog and rf integrated circuit design, CMOS reliability and radiation hardness, compound semiconductor characterization, modeling and reliability. The facilities of the associated laboratories include several systems for the DC, rf and pulsed characterization of GaN HEMTs, current Deep Level Transient Spectroscopy up to 600 V, accelerated testing in a wide range of environmental conditions, failure analysis using electroluminescence spectroscopy and microscopy techniques, AFM and electron microscopy. Recent studies on GaN material and devices at the University of Padova have analyzed the effects of material defectivity and deep levels on GaN HEMTs, the correlation with dynamic on-resistance measurements, the study of breakdown mechanisms, the analysis of the reliability and of the physical failure mechanisms of GaN LEDs and heterojunction and quantum-dot lasers for silicon photonics. Enrico Zanoni is coauthor of more than 500 publications on the modeling and reliability physics of

silicon and compound semiconductor devices and of 4 patents.

TM2.3 - Defect Localization Technique Selection for Reliability and Functional Fails - *Greg Johnson / Carl Zeiss*

Complete understanding of reliability fails requires physical characterization of the precise element that is failing. Given an "alphabet soup" of acronyms, the choice of the appropriate technique for fault isolation and failure analysis can be very challenging. Additional challenges are provided by the industry moving to advanced technology nodes, novel device architectures, and 3D-stackings at chip and wafer level. Thus, it will be increasingly important to understand not only the cutting-edge techniques but also which existing ones are due to become obsolete.

Drawing on experience from reliability and device array failure analysis across multiple nodes, this talk will provide a physics overview of seven basic concepts, and the defect localization techniques based on them: 1) Electron Beam Absorbed Current, 2) Optical/Electrical/Ion Beam Induced Current, 3) Passive Voltage Contrast, 4) Optical/Electrical/Ion Beam Induced Resistance Change, 5) Thermography, 6) Photon Emission Microscopy, and 7) Probing, as used in techniques like Conductive Atomic Force Microscopy. This whirlwind tour of the FA application space will then be summed up with a decision tree to explain which techniques are best suited for a wide range of defect types seen in FEOL processing. FA examples as well as the strengths and limitations of each technique will be given. This talk will be especially useful for engineers working in electrical characterization and design.

Greg Johnson is a Senior Application Development Engineer in the Probing Group of Carl Zeiss Process Control Solutions. In previous experience at both IBM

and GLOBALFOUNDRIES, he led FEOL defect localization across eight successful technology node qualifications. He serves on review committees of both ISTFA and IPFA. He has a B.S. in materials engineering from Virginia Tech, has authored over a dozen papers on novel fault isolation techniques, and is an inventor on 19 U.S. Patents.

TM3.1 - Statistical implementations for reliability assessment in automotive manufacturing - *Cristiano Capasso / GLOBALFOUNDRIES*

Automotive manufacturing requires a higher level of reliability performance especially when dealing with safety systems (e.g. autonomous driving). Wafer fabrication foundries, in collaboration with their customers, own the responsibility to demonstrate that these levels are met according to meaningful statistical procedures.

With this tutorial we will share and discuss pros and cons of data acquisition and data analysis methodologies, together with their impact on turnaround time, cost and accuracy. We will introduce new ideas on how to refine our understanding of the data and how to optimize lifetime extrapolations by leveraging statistical learning from interdisciplinary studies. A sample case will be presented to show the reliability impact of these new ideas on the silicon manufacturing line.

Cristiano Capasso earned his Doctor Degree in Physics from the University of Rome in 1984. He started his career in the USA as a Post Doctoral researcher at the University of Florida and worked in academia for 10 years. His main body of work was on solid state physics, bio-physics, synchrotron radiation, x-ray optics, x-ray microscopy and x-ray lithography. He joined Motorola in 1994, later Freescale, to continue x-ray lithography development. Over the course of 2 decades with Motorola/Freescale, Cristiano

led Cu interconnect reliability activity, worked on high-K metal gates integration schemes, transferred CMOS technologies to foundries, and supported reliability and test procedures of 45nm SOI products for networking operations. In 2013 he joined GLOBALFOUNDRIES in Malta, NY where he built the product reliability team and lab dealing with both wafer level and package level reliability. He is currently responsible for Malta's automotive development and for reliability statistical modeling methods.

TM3.2 - Testing of Automotive ICs - *Nilanjan Mukherjee / Mentor Graphics*

The design of autonomous cars is rapidly increasing the electronic content within automotive vehicles. The processing power of ICs needed for ADAS (Advanced Driver Assistance Systems) is growing exponentially, thereby pushing the complexity further. Consequently, automotive ICs that traditionally used to lag a few technology nodes for manufacturing are now using the latest technology nodes (for example 7nm) for designing and productizing such sophisticated SOCs. This tutorial will cover some of the test technologies that are being used for automotive ICs to help achieve very high test quality during manufacturing. It will also cover the in-system test requirements and the test solutions that are being deployed for key-on, key-off, and periodic testing throughout the life-span of the device.

Nilanjan Mukherjee received a B.Tech. (Hons) degree in Electronics & Communication Engineering from IIT, Kharagpur, India, and a Ph.D. degree from McGill University, Canada. Dr. Mukherjee is currently the Engineering Director in the Design-to-Silicon division at Mentor Graphics. At Mentor Graphics, he was a co-inventor of the EDT technology and a lead developer for TestKompress, which is the leading test

compression tool in the industry today. Additionally, he is also a con-inventor and helped in productizing the VersaPoint Test Points technology and Low Power Hybrid TestKompress/Logic BIST technology. Prior to joining Mentor Graphics, he worked at Lucent Bell Laboratories in New Jersey.
Dr. Mukherjee has co-authored more than 75 technical papers at various conference proceedings and archival journals. He is a co-inventor of 47 US patents and several international patents. He has received numerous Best Paper awards including the Most Significant Paper Award at ITC 2012, the Best Paper Award at VLSI Design in 2009, the Donald O. Pederson Outstanding Paper Award from the IEEE Circuits and Systems Society in 2006, the Teruhiko Yamada Memorial Best Student Paper Award at ATS 2001, and the Best Paper Award at VTS 1995. Dr. Mukherjee has served on the program committee for various technical conferences and workshops. He has represented Mentor Graphics at the Semiconductor Research Organization (SRC), at the International Technology Roadmap for Semiconductors (ITRS), and as a panelist for National Science Foundation (NSF). Dr. Mukherjee has given several tutorials at DAC, ITC, and VLSI Design conferences, offered short term courses on DFT, and has given talks at various conferences and company sponsored events.

TM3.3 - Closing the gap between Reliability Physics, EDA and Circuit Design - *Georgios Konstadinidis / Google*

Accurate Circuit Reliability analysis is essential in reducing design margins and time to market, while at the same time enabling high levels of product performance and reliability.
The goal of this Tutorial is to bring awareness and mutual understanding of the constraints across the various disciplines, and help strike a balance in the definition of the reliability rules, their implementation

in EDA tools and their proper usage by the circuit designers.
Following a brief description of the circuit reliability issues, the Physics behind them and the main characterization techniques we will provide an overview of the circuit techniques used to account for and mitigate these issues, and elaborate on the requirements imposed on the EDA tools. We will highlight common in situ monitoring and adaptive techniques to control the reliability and maximize performance over the lifetime of the product, and provide a brief introduction to product level testing techniques and what to do or not do during HTOL.
Understanding how all this fits together is critical in establishing the skeleton of a Reliability Physics, EDA, and circuit design closed loop methodology.

Georgios K. Konstadinidis is a Technology and Chip Implementation Lead at Google focusing on the R&D of Machine Learning Accelerators. He received the Ph.D degree in electrical engineering from the Technical University of Berlin, Germany and a B.Sc. Degree in Physics, M.Sc. in electronics from the Aristoteles University Thessaloniki Greece. From 2010 to 2017 he was a Senior Hardware Architect at Oracle, focused on high performance microprocessor physical design. He has been involved in the technology, design porting, physical design, reliability, optimization, circuit methodology, signal integrity, timing, and CAD tools for several projects. From 1991 to 1995 he was the leader of the high performance bipolar ICs design team at the R&D Center of SGS Thomson in England and in Catania, Italy. He was involved in the design of several ICs for telecommunications, in device modeling and process optimization.
Dr. Konstadinidis holds 12 patents and has several IEEE publications. He served as a member of the ISSCC Digital Program Committee from 2002 to 2007,

and as Guest Editor for the IEEE Journal of Solid State Circuits. He is a co-author of the book "Clocking in Modern VLSI Systems", Springer, 2009. He currently serves as Chair of the IRPS Digital Circuit Reliability sub-committee.

TM4.1 - Reliability issues of NAND Flash memory - *Riichiro Shirota and Hiroshi Watanabe / National Chiao Tung University*

Studies of reliability issues in Flash memory has a long, long history. The difficulty comes from that both electric field across and current flowing through oxide is high during program and erase. This causes a lot of traps and surface states. Nevertheless, the mechanism is still an open problem. In addition, recent products of NAND Flash have already transited from 2D to 3D, which has caused new reliability issues. One is related to grain boundaries in poly Si channel. The other is related to charge storage layer including Si-nitride. In this tutorial, we will review two topics considering above mentioned circumstances. First is independent from technology node and universal among many kinds of reliability issues. Next is related especially to 3D-NAND.

Riichiro Shirota: He received the B.Sc., M.Sc., and Ph.D degrees in physics from the University of Nagoya, in Japan, in 1977, 1979, 1982, respectively. He has been a Professor with the Department of Electrical and Computer Engineering, National Chiao Tung University, Taiwan, since 2010. From 2006 to 2010, he was a professor of National Tsing Hur University in Taiwan. From 1982 to 2006, he was in Toshiba Corporation, and had been in charge of NAND Flash development from 1987 to 2006. His recent main research field is the reliability of Flash memory.

Hiroshi Watanabe: He received the B.Sc., M.Sc., and Ph.D. degrees in physics from the University of

Tsukuba, Japan, in 1989, 1991, and 1994, respectively. He has been a Professor with the Department of Electrical and Computer Engineering, National Chiao Tung University, Taiwan, since 2010. He has been in charge of theoretical physics related to the semiconductor devices from 1994, and his recent main field is the analysis of elementary steps of charge trap and its application.

TM4.2 - Device Challenges and Opportunities for ReRAM - *Kensuke Ota / Toshiba Memory Corporation*

The resistive random access memory (ReRAM) has attracted much attention since its discovery. Because of the simple structure, ReRAM is considered as potential candidates for future non-volatile memory applications. There are two types of resistive switching phenomena; filamentary switching and non-filamentary switching. Furthermore, filamentary switching can be classified into oxygen based RAM (OxRAM) where the filament is composed of oxygen vacancies, and conductive bridge RAM (CBRAM) utilizing the redox reaction of metal ions. Device challenges are different between these types of switching phenomena. In this tutorial, pros and cons of each type of ReRAM on performances and reliabilities are reviewed on the basis of the switching mechanisms.

Kensuke Ota is a research scientist at Toshiba Memory Corporation. He received the B.S., M.S., and Ph.D. degrees from Department of Basic Science, the University of Tokyo, Tokyo, Japan, in 2004, 2006, and 2009, respectively. In 2009, he joined Advanced LSI Technology Laboratory, Corporate Research and Development Center, Toshiba Corporation, where he has been engaged in the research on performance enhancement and reliability issue of nanowire transistors. He has been a Toshiba assignee to IMEC from 2015 to 2016. His current work includes

emerging memory devices. He is a committee member of ESSDERC and SSDM.

TM4.3 - Advanced Packaging Reliability - *Kang-Wook Lee / SK Hynix*

With diminishing returns from traditional transistor scaling further improvements in power and performance of systems are likely to come from advanced packaging technologies. Furthermore, the increased focus on mobile computing, HPC, cloud networking, and AI has highlighted the need for improved form-factor, improved performance, and low power technologies. This can be achieved only via increased emphasis on advanced packaging concepts such as 2.5D/3D integration and fan-out wafer level packaging technologies. Further trend of 3D integration towards thinner chip, more layer stacking, and more joining density to maximize area efficiency. 2.5D and fan - out packaging requires more fine width/space, multi - layers of Cu RDL and large package size for multi - dies integration. These trends could induce severe reliability challenges.

This session will focus on advanced packaging reliability challenges of 2.5D, 3D and fan-out packaging for topic for further system scale.

Kang-Wook Lee is currently VP, Package Development, SK Hynix, Korea. He received the Ph.D. degree in machine intelligence and systems engineering from Tohoku University, Japan, in 2000. From 2000 to 2001, he was a Researcher with Japan Science and Technology Corporation, Japan. From 2001 to 2002, he was a Postdoctoral Researcher with the Department of Electrical, Computer, and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY, USA. From 2002 to 2008, he worked with Memory Division, Samsung Electronics Ltd., Korea, as a Principal Engineer. From 2008 to 2016, he worked

with the New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan as a Professor. From 2017 to 2018, he worked with R&D, Amkor Technology Korea, as a VP.

He has led the development of 2.5D/3D integration technologies for high performance/density memories, multi - functional convergence systems, fan-out wafer-level packaging for system scale, and the reliability studies about the impacts of 3D integration process on device performance. He is a Senior Member of IEEE.

2019 IRPS Reliability Year in Review
Monday, April 1
Regency Main
3:00 pm – 5:00 pm

YIR 1- NBTI/PBTI: State-of-the-art

Tibor Grasser, TU Wien

Abstract: During the past decade bias temperature instabilities (BTI) have retained their center-stage position as one of the most relevant reliability issues in modern MOS transistors. While positive BTI (PBTI) has occasionally received a lot of attention after the introduction of new high-k dielectrics, it is negative BTI (NBTI) which appears to be dominant for well optimized gate stacks. Following a brief historical review on the history of BTI, recent developments are summarized and discussed, such as the various new measurement methods and attempts in explaining this elusive phenomenon. In particular, the long-lasting controversy on whether diffusion- or reaction-limited processes are responsible for BTI has gained new momentum during the previous years and the state of the discussion will be summarized.

Prof. Tibor Grasser is an IEEE Fellow and head of the Institute for Microelectronics at TU Wien. He has numerous reliability-related publications, edited various books, e.g. on the bias temperature instability and hot carrier degradation (both Springer), is a distinguished lecturer of the IEEE EDS, has been involved in outstanding conferences such as IEDM, IRPS, SISPAD, ESSDERC, and IIRW, is a recipient of the Best and Outstanding Paper Awards at IRPS

(2008, 2010, 2012, and 2014), IPFA (2013 and 2014), ESREF (2008) and the IEEE EDS Paul Rappaport Award (2011). He currently serves as an Associate Editor for the IEEE Transactions on Electron Devices following his assignment for Microelectronics Reliability (Elsevier).

YIR 2 - Metallization reliability

James Lloyd, SUNY Polytechnic Institute

Abstract: With new materials replacing the traditional Cu metallization, back end reliability is taking on a new face. Cobalt and other exotic schemes are exciting and enabling improvements in performance and reliability. The latest results will be reviewed in this presentation.

Bio: Over 50 years experience in reliability physics, concentrating on back end conductors and dielectrics. From IBM, Digital Equipment Corporation, Max-Planck-Institut, Jet Propulsion Laboratory and now SUNY Polytechnic Institute, **Dr. Lloyd** has made many contributions to the understanding of metallization and TDDB related reliability. He is now active in education and continuing research into these important issues.

YIR 3 - Functional Safety, reliability, availability

Riccardo Mariani, Intel Corporation Italia

Abstract: The new world of autonomous vehicles (AV) is posing many challenges to automotive safety.

The new world of autonomous vehicles (AV) and SW defined industrial systems (SDIS) is posing many safety, reliability and availability challenges to automotive and industrial equipment and eventually to semiconductor industry. The talk will be a 2 years perspective on the status of functional safety publications, with specific emphasis on ISO 26262, ISO 21448 (SOTIF), cybersecurity and other related topics (such as Availability and Responsibility Sensitive Safety).

Riccardo Mariani is an Intel Fellow and the chief functional safety technologist in the Internet of Things Group at Intel Corporation. He is responsible for defining strategies, roadmaps and technologies for Internet of Things applications that require functional safety and high performance, including transportation and industrial systems. He is also the functional safety global domain lead for Intel's CISA Architecture Working Model Initiative. Mariani joined Intel in 2016 with the acquisition of Yogitech S.p.A., a leading provider of functional safety technologies.

2019 IRPS Workshops
Tuesday, April 2
Food and Beverages
6:00 PM – 7:00 PM
Regency Foyer Terrace

Workshops
7:00 PM - 9:20 PM

Time	Workshop topic/ Location	Moderator(s)
7:00 PM	**FinFET** Regency I-III	*Souvik Mahapatra (IIT) Chetan Prasad (Intel)*
7:00 PM	**BEOL & CPI** Windjammer III-IV	*Jeff Gambino (ON Semi) Zhuojie (George) Wu (GF)*
7:00 PM	**DFR/DFRT** Windjammer I-II	*Nilanjan Mukherjee (Mentor Graphics) Vincent Huard (Dolphin Integration)*
7:00 PM	**GaN/GaN on Si** Cypress	*Sandeep Bahl (TI) Sameh Khalil (Infineon)*
7:00 PM	**3D NAND** Regency IV-VI	*Xiaoyu Yang (Western Digital Corp) Wei-Chen Chen (Macronix)*
7:00 PM	**System Reliability** Big Sur	*Scott Hareland (Medtronic)*
8:00 PM - ***Break***		
8:05 PM	**UTB-SOI FET** Regency I-III	*Tanya Nigam (GF) Vincent Huard (Dolphin Integration)*
8:05 PM	**TSV & Advanced packaging** Windjammer III-IV	*Kristof Croes (imec) Kangwook Lee (SK hynix)*
8:05 PM	**Rel. Simulation** Windjammer I-II	*Georgios Konstadinidis (Google) James Tschanz (Intel)*
8:05 PM	**SiC** Cypress	*Nando Kaminski (Univ. of Bremen)*
8:05 PM	**STT-MRAM** Regency IV-VI	*Tetsuo Endoh (Tohoku Univ.) Junghyuk Lee (Samsung)*
8:05 PM	**Neuromorphic** Big Sur	*Gennadi Bersuker (Aerospace Corp) Pey Kin Leong (SUTD)*
9:05 PM	**Meeting Moderators** TBD	
9:20 PM - ***Close***		

KEYNOTE TALKS

IRPS Keynotes & IEW Keynote and Invited Talks

Monday, April 1
General Session
Monterey Ballroom

9:30 am
IEW Invited Talk 1: System Level Testing of Components
Doctor Kathy Muhonen, Qorvo
5:20 pm
IEW Keynote: Radio-Frequency Interference in Wireless Devices
Professor Jun Fan, Missouri University of Science and Technology

Tuesday, April 2
General Session
Regency Main

8:35 am
IRPS Keynote 1: Abundant-Data Computing: The *N3XT* 1,000X
Professor Subhasish Mitra, Stanford University
9:20 am
IRPS Keynote 2: The Era of Hyperscaling in Electronics
Professor Suman Datta, University of Notre Dame

Wednesday, April 3
General Session
Monterey Ballroom

9:00 am
IEW Invited Talk 2: Cost-Efficient Methods for Latch-up Prevention in CMOS Integrated Circuits
Professor Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University, Taiwan

Wednesday, April 3
Joint Poster Session & Reception
6:00 pm – 9:00 pm
Monterey Ballroom

SESSIONS

TUESDAY

Session 2A - MB

Tuesday, 2nd April

10:25 AM – Session Introduction

10:30 AM
2A.1 Efficient Simulation of Electromigration Damage in Large Chip Power Grids Using Accurate Physical Models
Farid N. Najm and Valeriy Sukharev, ECE Department University of Toronto, Mentor, A Siemens Business Fremont, CA 94538, USA

10:55 AM
2A.2 An Analytical Transient Joule Heating Model for an Interconnect in a Modern IC: Material Selection (Cu, Co, Ru) and Cooling Strategies
Woojin Ahn, Yen-Pu Chen, and Muhammad Ashraful Alam, Department of ECE, Purdue University, West Lafayette, IN 47907 USA

11:20 AM
2A.3 Time Dependent Dielectric Breakdown of Cobalt and Ruthenium Interconnects at 36nm Pitch
H. Huang, P. S. McLaughin, J. J. Kelly, C. -C. Yang, R. G. Southwick, M. Wang, G. Bonilla, and G. Karve, Semiconductor Technology Research, IBM, Albany, NY USA

11:45 AM
2A.4 Robust BEOL MIMCAP for Long and Controllable TDDB Lifetime
Lili Cheng, Seungman Choi, Sean Ogden, Teck Jung Tang, and Robert Fox, GLOBALFOUNDRIES, Malta, NY, USA

Session 2B - TX

Tuesday, 2nd April

10:25 AM – Session Introduction

10:30 AM
2B.1 Reliability Limiting Defects in MOS Gate Oxides: Mechanisms and Modeling Implications
Daniel M. Fleetwood, Vanderbilt University Department of Electrical Engineering and Computer Science, Nashville, TN 37235 USA

10:55 AM
2B.2 Accelerated Capture and Emission (ACE) Measurement Pattern for Efficient BTI Characterization and Modeling
Zhicheng Wu[1], Jacopo Franco, Dieter Claes[1], Gerhard Rzepa[2], Philippe J. Roussel, Nadine Collaert, Guido Groeseneken[1], Dimitri Linten, Tibor Grasser[2], and Ben Kaczer, imec, Leuven, Kapeldreef 75, B3001 Leuven, Belgium, [1]also at ESAT-MICAS, KU Leuven, Belgium, [2]institute for microelectronics, T.U. Vienna, Austria*

11:20 AM
2B.3 A New Time Efficient Methodology for the Massive Characterization of RTN in CMOS Devices
G. Pedreira[1], J. Martin-Martinez[1], J. Diaz-Fortuny[1], P. Saraza-Canflanca[2], R. Rodriguez[1], R. Castro-Lopez[2], E. Roca[2], F. V. Fernandez[2], and M. Nafria[1], [1]Electronic Engineering Department. Universitat Autonoma de Barcelona (UAB), Spain, [2]Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, Spain

11:45 AM
2B.4 Bias Temperature Instability Reliability in Stacked Gate-All-Around Nanosheet Transistor
Miaomiao Wang[1], Jingyun Zhang[1], Huimei Zhou[1], Richard G. Southwick[1], Robin Hsin Kuo Chao[1], Xin Miao[1], Veeraraghavan S. Basker[1], Tenko Yamashita[1], Dechao Guo[1], Gauri Karve[1], Huiming Bu[1], and James H. Stathis[2], [1]IBM Research Division, Albany Nanotech, Albany, NY, 12203, USA, [2]IBM Research Division T. J. Watson Research Center Yorktown Heights, NY, 10598, USA

Session 2C – MY

Tuesday, 2nd April

10:25 AM – Session Introduction

10:30 AM
2C.1 New Insights into the Imprint Effect in FE-HfO_2 and its Recovery
Y. Higashi[2], K. Florent[1,3], A. Subirats[1,4], B. Kaczer[1], L. Di Piazza[1], S. Clima[1], N. Ronchi[1], S. R. C. McMitchell[1], K. Banerjee[1], U. Celano[1], M. Suzuki[2], D. Linten[1], and J. Van Houdt[1,3], [1]imec, Kapeldreef 7, B-3001 Leuven, Belgium, [2]Toshiba Memory Europe GmbH assigned at imec, [3]ESAT Department, KU Leuven, Leuven, Belgium, [4]Now with Micron, Technology Inc, 8000 S Federal Way, Boise, ID 83707, USA

10:55 AM
2C.2 Superior Endurance Performance of 22-nm Embedded MRAM Technology
V. B. Naik, J. H. Lim, K. Yamane, D. Zeng, H. Yang, N. Thiyagarajah, J. Kwon, N. L. Chung, R. Chao, T. Ling, and K. Lee, GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore 738406.

11:20 AM
2C.3 Reliability of 8Mbit Embedded-STT-MRAM in 28nm FDSOI Technology
Y. Ji, H. J. Goo, J. Lim, S. B. Lee, S. Lee, T. Uemura, J. C. Park, S. I. Han, S. C. Shin, J. H. Lee[#], Y. J. Song, K. M. Lee[#], H. M. Shin[#], S. H. Hwang, B. Y. Seo, Y. K. Lee, J. C. Kim, G. H. Koh[#], K. C. Park, S. Pae, G. T. Jeong, J. S. Yoon, and E. S. Jung, Foundry Business, Samsung Electronics, Kiheung, Korea, San #24 Nongseo-Dong Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea 446-711, [#]R&D Center, Samsung Electronics, Hwasung, Korea

12:30 PM - Break

Session 3A – WB SiC

Tuesday, 2nd April

01:30 PM – Session Introduction

01:35 PM
3A.1 Gaining Confidence - A Review of Silicon Carbide's Reliability Status
Nando Kaminski, Sarah Rugen, and Felix Hoffmann, University of Bremen, Institute for Electrical Drives, Power Electronics and Devices (IALB), Bremen, Germany

02:00 PM
3A.2 Avalanche and Short-Circuit Robustness of 4600 V SiC DMOSFETs

Siddarth Sundaresan, Vamsi Mulpuri, Stoyan Jeliazkov, and Ranbir Singh, GeneSiC Semiconductor, 43670 Trade Center Pl, Suite 155, Dulles VA 20166, USA

02:25 PM
3A.3 High Resolution Observation of Subsurface Defects at SiO_2/4H-SiC Interfaces by Local Deep Level Transient Spectroscopy Based on Time-Resolved Scanning Nonlinear Dielectric Microscopy
Yuji Yamagishi and Yasuo Cho, Research Institute of Electrical Communication, Tohoku University, Sendai, Japan

02:50 PM
3A.4 Permanent and Transient Effects of High-Temperature Bias Stress on Room-Temperature V_T Drift Measurements in SiC Power MOSFETs
Daniel B. Habersat, Ronald Green, and Aivars J. Lelis, Power Conditioning Branch, U.S. Army Research Laboratory, Adelphi, MD, USA

Session 3B – PI

Tuesday, 2nd April

01:30 PM – Session Introduction

01:35 PM
3B.1 Gate-Stack Engineered NBTI Improvements in High-Voltage Logic-for-Memory High-κ/Metal Gate Devices
B.J. O'Sullivan, R. Ritzenthaler, G.Rzepa, Z. Wu, E. Dentoni Litta, O. Richard, T. Conard, V. Machkaoutsan**, P. Fazan**, C. Kim***, J. Franco, B. Kaczer, T. Grasser*, A. Spessot, D Linten, and N. Horiguchi, imec, Leuven, Belgium, *TU, Wien, Austria, **Micron, ***SK Hynix*

02:00 PM

3B.2 Hot Carrier Reliability Improvement of Thicker Gate Oxide nFET Devices in Advanced FinFETs

M. Iqbal Mahmud, A. Gupta, M. Toledano-Luque, N. Mavilla, J. Johnson, P. Srinivasan, A. Zainuddin, S. Rao, S. Cimino, B. Min, and T. Nigam, Reliability Engineering, GLOBALFOUNDRIES Inc., 400 Stone Break Road extension, Malta, NY 12020, USA

02:25 PM

3B.3 Novel Oxide Top-off Process Enabling Reliable PC-CA TDDB on IO Devices with Self Aligned Contact

Tian Shen, Abu Naser Zainuddin, Purushothaman Srinivasan, Zakariae Chbili, Kai Zhao, and Patrick Justison, GLOBALFOUNDRIES Inc., 400 Stone Break Road Extension, Malta, NY 12020

02:50 PM

3B.4 Process Optimization for HCI Improvement in I/O Analog Devices

C. Diouf, N. Guitard, M. Rafik, J. J. Martinez, X. Federspiel,
A. Bravaix, D. Muller, and D. Roy, ST Microelectronics, 850 rue Jean Monnet, Crolles, France.

Session 3C – NM Focus

Tuesday, 2nd April

01:30 PM – Session Introduction

01:35 PM

3C.1 Reliability Challenges with Materials for Analog Computing

Eduard A. Cartier[1], Wanki Kim[1], Nanbo Gong[1], Tayfun Gokmen[1], Martin M. Frank[1], Douglas M. Bishop[1], Youngseok Kim[2],
Seyoung Kim[1], Takashi Ando[1], Ernest Y. Wu[3], Praneet Adusumilli[1], John Rozen[1], Paul M. Solomon[1], Wilfried

Haensch[1], Matthew J. BrightSky[1], Abu Sebastian[4], Geoffrey W. Burr[5], and Vijay Narayanan[1], [1]IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, USA, [2]IBM Research Division, 257 Fuller Road, Albany, NY, USA, [3]IBM Research Division, Essex Junction, VT, USA, [4]IBM Research Division, Zurich, 8803 Ruschlikon, Switzerland, [5]IBM Research Division, Almaden, San Jose, CA, USA

02:00 PM
3C.2 Reliability Perspective on Neuromorphic Computing Based on Analog RRAM
Huaqiang Wu, Meiran Zhao, Yuyi Liu, Peng Yao, Yue Xi, Xinyi Li, Wei Wu Qingtian Zhang, Jianshi Tang, Bin Gao, and He Qian, Institute of Microelectronics, Tsinghua University, Beijing 100084, China

02:25 PM
3C.3 From Emerging Memory to Novel Devices for Neuromorphic Systems: Consequences for the Reliability Requirements of Memristive Devices
D.J. Wouters, Institute of Electronic Materials (IWE 2) & JARA-FIT, RWTH-Aachen University, Sommerfeldstraße 24, 52074, Aachen, Germany

02:50 PM
3C.4 Reliability Issues in Analog ReRAM Based Neural-Network Processor
Ryutaro Yasuhara, Takashi Ono, Reiji Mochida, Shunsaku Muraoka, Kazuyuki Kouno, Koji Katayama, Yuriko Hayata, Masayoshi Nakayama, Hitoshi Suwa, Yukio Hayakawa, Takumi Mikawa, Yasushi Gohou, and Shinichi Yoneda, Semiconductor Business Unit, Panasonic Semiconductor Solutions Co., Ltd., Nagaokakyo, Japan

Session 3D – RT

Tuesday, 2nd April

03:35 PM – Session Introduction

03:40 PM

3D.1 Alternating Temperature Stress and Deduction of Effective Stress Levels from Mission Profiles for Semiconductor Reliability

A. Hirler, A. Alsioufy*, J. Biba*, T. Lehndorff*, D. Lipp†, H. Lochner‡, M. Siddabathula†, S. Simon‡, T. Sulima*, M. Wiatr†, and W. Hansch*, *Institute of Physics, Universitat der Bundeswehr München, Werner-Heisenberg-Weg 39, 85577 Neubiberg, Germany, †GLOBALFOUNDRIES Dresden Module Two LLC, Wilschdorfer Landstraße 101, 01109 Dresden, Germany, ‡AUDI AG, Auto-Union-Straße 1, 85045 Ingolstadt, Germany*

04:05 PM

3D.2 A Fast and Test-Proven Methodology of Assessing RTN/Fluctuation on Deeply Scaled Nano pMOSFETs

Rui Gao[1], Zhiyuan He[1], Yiqiang Chen[1], Chang Liu[1], Yun Huang[1], Yunfei En[1], Zhigang Ji[2], and Jianfu Zhang[2], [1]Science and Technology on Reliability Physics and Application of Electronic Component Laboratory No.5 Electronics Research, Institute of the Ministry of Industry and Information Technology Guangzhou, 510610, Guangdong, P. R. China, [2]School of Engineering, Liverpool John Moores University, Byrom Street, Liverpool, L3 3AF, UK

04:30 PM

3D.3 Machine Learning for Detection of Competing Wearout Mechanisms

Shu-han Hsu, Kexin Yang, and Linda Milor, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA

04:55 PM

3D.4 HCI Improvement on 14nm FinFET IO Device by Optimization of 3D Junction Profile

Xinggon Wan[1], Baofu Zhu[2], Meera Mohan[3], Keija Wu[3], Dongil Choi[3], and Arfa Gondal[1], [1]Quality and Reliability Assurance Department, [2]Global TCAD, [3]PDYE Device, GLOBALFOUNDRIES Inc., 400 Stone Break Road Extension, Malta, NY, 12020, USA

Session 3E – CR Focus

Tuesday, 2nd April

03:35 PM – Session Introduction

03:40 PM
3E.1 Advanced Circuit Reliability Verification for Robust Design
Antony Fan, Joddy Wang, and Vladimir Aptekar, Analog and Mixed-Signal Simulation Synopsys Inc., Mountain View, California

04:05 PM
3E.2 Applying Machine Learning to Design for Reliability Coverage
Norman Chang[1], Wentze Chuang[1,2], Ganesh Kumar Tsavatapalli[1], Joao Geada[1], Hao Zhuang[1], Sankar Ramachandran [1], Rahul Rajan [1], Ying-Shiun Li [1], Yaowei Jia [1], Mathew Kaipanatu [1], Suresh Kumar Mantena [1], Ming-Chih Shih [1], Anita Yang [1], and Roger Jang [2], [1]ANSYS Inc., [2]National Taiwan University

04:30 PM
3E.3 Physics to Tapeout: The Challenge of Scaling Reliability Verification
Sridhar Srinivasan and Matthew Hogan, Mentor, a Siemens Business, Wilsonville, OR, U.S.A.

04:55 PM
3E.4 Recent Updates to Transistor Level Reliability Analysis
Art Schaldenbrand, Jushan Xie, and Hany Elhak, Cadence Design Systems, Inc., Custom IC and PCB Group, San Jose, CA

Session 3F – NM

Tuesday, 2nd April

03:35 PM – Session Introduction

03:40 PM
3F.1 Wafer-Scale TaO_x Device Variability and Implications for Neuromorphic Computing Applications
Christopher H. Bennett[1], Diana Garland[1], Robin B. Jacobs-Gedrim[1], Sapan Agarwal[1], and Matthew J. Marinella[1], [1]Sandia National Laboratories, Albuquerque, NM 87185-1084, USA

04:05 PM
3F.2 Switching Variability Factors in Compliance-Free Metal Oxide RRAM
D. Veksler[1], G. Bersuker[1], A. W. Bushmaker[1], P. R. Shrestha[2], K. P. Cheung[2], and J. P. Campbell[2], [1]MTD, The Aerospace Corporation, Los Angeles CA, [2]NDCD, National Institute of Standards and Technology, Gaithersburg, MD

04:30 PM
3F.3 Low Voltage Transient RESET Kinetic Modeling of OxRRAM for Neuromorphic Applications
J. Doevenspeck[1,2], R. Degraeve[1], A. Fantini[1], P. Debacker[1], D. Verkest[1], R. Lauwereins[1,2], and W. Dehaene[1,2], [1]imec, Kapeldreef 75 - B-3001, Heverlee, Belgium, [2]KU Leuven, Dept. ESAT, Kasteelpark Arenberg 10, B-3001, Heverlee, Belgium

04:55 PM
3F.4 First Demonstration and Physical Insights into Time-Dependent Breakdown of Graphene Channel and Interconnects
Abhishek Mishra[1,2], Adil Meersha[1], N.K. Kranthi[1], Kruti Trivedi[1], Harsha B. Variar[1], N S Veenadhari Bellamkonda[1], Srinivasan Raghavan[2], and Mayank Shrivastava[1], [1]Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, India, [2]Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore, India

Session 4A – WB GaN

Wednesday, 3rd April

08:00 AM – Session Introduction

08:05 AM
4A.1 A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions
Sandeep R. Bahl and Paul Brohlin, High Voltage Power, Texas Instruments Incorporated, 2900 Semiconductor Dr., Santa Clara, CA 95052, 12500 TI Blvd, Dallas TX 75243, USA

08:30 AM
4A.2 Influence of Donor-Type Hole Traps under p-GaN Gate in GaN-Based Gate Injection Transistor (GIT)
Kenichiro Tanaka, Masahiro Hikita, and Tetsuzo Ueda, Automotive and Industrial Systems Company, Panasonic Corporation, 3-1-1, Yagumo-naka-machi, Moriguchi City, Osaka, Japan 570-8501

08:55 AM
4A.3 Accelerated Device Degradation of High-Speed Ge Waveguide Photodetectors
A. Lesniewska, S. A. Srinivasan, J. Van Campenhout, B. J. O'Sullivan, and K. Croes, Imec, Kapeldreef 75, 3001 Leuven, Belgium

09:20 AM
4A.4 Low-Side GaN Power Device Dynamic R_{on} Characteristics under different Substrate Biases
Wen Yang[1], Jiann-Shiun Yuan[1], Balakrishnan Krishnan[2], and Patrick Shea[3], [1]Department of Electrical and Computer Engineering, University of Central Florida, Orlando, Florida 32816, U.S.A., [2]BRIDG, 200 NeoCity Way, Kissimmee, Florida 32744, U.S.A., [3]Renensas, 1650 Robert J. Conlan Blvd. NE, Palm Bay, Florida 32905, U.S.A.

Session 4B – DL

Wednesday, 3rd April

08:00 AM – Session Introduction

08:05 AM
4B.1 Charge Transport and Degradation in TMOs: A Multi-Scale Defect-Centric Approach
Luca Larcher (UniMORE)

08:30 AM
4B.2 Spatio-Temporal Defect Generation Process in Irradiated HfO_2 MOS Stacks: Correlated versus Uncorrelated Mechanisms
Fernando Leonel Aguirre[1], Andrea Padovani[2], Alok Ranjan[3], Nagarajan Raghavan[3], Nahuel Vega[4], Nahuel Müller[4], Sebastián Matías Pazos[1], Mario Debray[4], Joel Molina[5], Kin Leong Pey[3], and Félix Palumbo[1], [1]Unidad de Investigación y Desarrollo de las Ingenierías - CONICET / Depto. Ingeniería Electrónica, Universidad Tecnológica Nacional Facultad Regional Buenos Aires, Av. Medrano 951, Ciudad Autónoma de Buenos Aires, Argentina, [2]MDLSoft, Inc, 5201 Great America Parkway, Suite 320, 95054, Santa Clara, CA, USA, [3]Engineering Product Development Pillar, Singapore University of Technology and Design, 8 Somapah Road, Singapore, 487372, [4]Laboratorio TANDAR - Gerencia de Investigación y Aplicaciones, Comisión Nacional de Energía Atómica – Centro, Atómico Constituyentes, Av. Gral. Paz 1499, San Martín, Buenos Aires, Argentina. [5]National Institute of Astrophysics, Optics and Electronics, Tonantzintla, Puebla, 72840 Mexico

08:55 AM
4B.3 Correct Extrapolation Model for TDDB of STT-MRAM MgO Magnetic Tunnel Junctions
J.H. Lim[1,2], N. Raghavan[1], V.B. Naik[2], J.H. Kwon[2], K. Yamane[2], H. Yang[2], K.H. Lee[2], and K.L. Pey[1], Engineering Product Development (EPD) Pillar, Singapore University of Technology and Design (SUTD), Singapore - 487 372., [2]GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore 738406.

09:20 AM

4B.4 Role of Defects in the Reliability of HfO_2/Si-Based Spacer Dielectric Stacks for Local Interconnects

C.Wu[1], A. Chasin[1], A. Padovani[2], A. Lesniewska[1], S. Demuynck[1], and K. Croes[1], [1]IMEC, Kapeldreef 75, Leuven, Belgium., [2]MDLSoft Inc., 5201 Great America Parkway, Suite 320, Santa Clara, CA 95054

09:45 AM

4B.5 Transformation of Ramped Current Stress V_{BD} to Constant Voltage Stress TDDB T_{BD}

Andrew Kim[1], Ernest Wu[2], Baozhen Li[3], and Barry Linder[1], [1]IBM System, Hopewell Junction, NY 12533, [2]IBM Research, Essex Junction, VT 5452, [3]Essex Junction, VT 05452

Session 4C – PR

Wednesday, 3rd April

08:00 AM – Session Introduction

08:05 AM

4C.1 Design-For-Reliability Flow in 7nm Products with Data Center and Automotive Applications

Jae-Gyung Ahn, I-Ru Chen, Ping-Chin Yeh, and Jonathan Chang, Hardware and System Product Development Group, Xilinx, Inc. 2100 All Programmable Drive San Jose, CA 95124

08:30 AM

4C.2 Enhanced Fail Rate projections using Negative Design Assist in Automotive Grade SRAMs

Sriram Balasubramnian, Hari Balan, Lei Liu, Kevin Khua, Wah Peng Neo, Dianji Sui and Tze Ho Simon Chan, GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore 738406

08:55 AM
4C.3 Experimental Implementation of 8.9Kgate Stress Monitor in 28nm MCU along with Safety Software Library for IoT Device Maintenance
Kan Takeuchi, Masaki Shimada, Shinya Konishi, Daisuke Oshida, Naoya Ota, Takashi Yasumasu, Koji Shibutani, Tomohiro Iwashita, Tetsuya Kokubun, and Fumio Tsuchiya, Renesas Electronics Corporation, 5-20-1, Josuihon-cho, Kodaira-shi, Tokyo 187-8588, Japan

09:20 AM
4C.4 High Voltage Tolerant Design with Advanced Process for TV Application
S. E. Liu[1], M. H Hsieh[1], Y. R. Chen[2], J. Y. Jao[2], M. Z. Lin[1], Y. H Fang[1], and M. J. Lin[1],[1]Quality Assurance, [2]Analog Design and Circuit Technology, MediaTek Inc., Hsinchu city, Taiwan

09:45 AM
4C.5 Product Reliability Methods to Enable High Performance CPU's
Roman Rechter, Robert Kwasnick, Almog Reshef, Oren Zonensain, Tal Raz, Anisur Rahman, Praveen Polasam, and Maxim Levit, Intel Corporation, Matam Industrial Park, 31015, Haifa, Israel

Session 4D – WB Focus

Wednesday, 3rd April

10:30 AM – Session Introduction

10:35 AM
4D.1 SiC Power MOSFETs: Designing for Reliability in Wide-Bandgap Semiconductors
Kevin Matocha[1], In-Hwan Ji[1], Xuning Zhang[1], and Sauvik Chowdhury[2], [1]Littelfuse Inc., Round Rock, TX USA, [2]Now at On Semiconductor, Phoenix, AZ USA

11:00 AM
4D.2 Design Strategies for Rugged SiC Power Devices
Diang Xing, Tianshi Liu, Susanna Yu, Minseok Kang, Arash Salemi, Marvin White, and Anant Agarwal, Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, 43210, USA

11:25 AM
4D.3 A Physical-Statistical Approach to AlGaN/GaN HEMT Reliability
Peter Moens[1] and Arno Stockman[1,2], [1]ON Semiconductor, Corporate R&D, Oudenaarde, Belgium, [2]University of Gent, Belgium

11:50 AM
4D.4 Perimeter Driven Transport in the p-GaN Gate as a Limiting Factor for Gate Reliability
S. Stoffels[1], N. Posthuma[1], S. Decoutere[1,] B. Bakeroot[2], A.N. Tallarico[3], Enrico Sangiorgi[3], Claudio Fiegna[3], J. Zheng[4], X. Ma[4], M. Borga[5], Elena Fabris[5], M. Meneghini[5], E. Zanoni[5], G. Meneghesso[5], J. Priesol[6], and A. Šatka[6], [1]imec - interuniversitair micro electronica centrum, Kapeldreef 75, Heverlee, Belgium, [2]Centre for Microsystems Technology, imec and Ghent University, 9052 Ghent, Belgium, [3]Department of Electrical, Electronic, and Information Engineering, University of Bologna, 47522, Cesena, Italy, [4]The Key Laboratory of Wide Band-Gap Semiconductor Material and Devices, Xidian University, Xi'an, CO 710071, China, [5]Department of Information Engineering, University of Padova, 35131 Padova, Italy, [6]Slovak University of Technology in Bratislava, IEP FEI, Ilkovičova 3, 812 19 Bratislava, Slovakia

12:15 PM
4D.5 Impact of Sidewall Etching on the Dynamic Performance of GaN-on-Si E-Mode Transistors
A. Tajalli[a], E. Canato[a], A. Nardo[a], M. Meneghini[a], A. Stockman[bc],P. Moens[b], E. Zanoni[a], and G. Meneghesso[a], [a] Department of Information Engineering, University of Padova, Italy, [b]ON

Semiconductor, Oudenaarde, Belgium, [c]CMST, University of Ghent, Belgium

Session 4E – DL

Wednesday, 3rd April

10:30 AM – Session Introduction

10:35 AM
4E.1 Dielectric Breakdown in 2D Layered Hexagonal Boron Nitride - The Knowns and The Unknowns
*K.L. Pey[1], A. Ranjan[1, 2], N. Raghavan[1], K. Shubhakar[1], and S.J. O'Shea[2], [1]Engineering Product Development, Singapore University of Technology and Design, Singapore - 487 372., [2]Institute of Materials Research and Engineering, A*STAR, 2 Fusionopolis Way, Singapore - 138 634.*

11:00 AM
4E.2 Comprehensive Methodology for Multiple Spots Competing Progressive Breakdown for BEOL/FEOL Applications— Impact of Variability: From Uncorrelated to Correlated Post-Breakdown —
Ernest Y. Wu[1+], Baozhen Li[2+], James H. Stathis[1], and Andrew Kim[2#], [1]IBM Research Div., *Yorktown Heights, NY, [+]Essex Junction, VT, USA, [2]IBM Systems Div., [#]Hopewell Junction, NY, USA*

11:25 AM
4E.3 Impact of Passive & Active Load Gate Impedance on Breakdown Hardness in 28nm FDSOI Technology
A.P. Nguyen[1], X. Garros[1], M. Rafik[2], F. Cacho[2], D. Roy[2], X. Federspiel[1], and F. Gaillard[1], [1]CEA-Leti, 17 Avenue des Martyrs, Grenoble, France, [2]ST Microelectronics, 850 rue Jean Monnet, Crolles, France

11:50 AM
4E.4 A Statistical Learning Model for Accurate Prediction of Time-Dependent Dielectric Degradation for Low Failure Rates
Kaustubh Joshi, Yung-Huei Lee, Yu-Cheng Yao, Shu-Wen Chang, Siao-Syong Bian, P. J. Liao, Jiaw-Ren Shih, and Min-Jan Chen, Quality and Reliability, Taiwan Semiconductor Manufacturing Company, 121, Park Ave. 3, Hsinchu Science Park Hsinchu, Taiwan 300-77, R.O.C

12:15 PM
4E.5 Time-Dependent Dielectric Breakdown under AC Stress in GaN MIS-HEMTs
Ethan S. Lee[1], Luis Hurtado[2], Jungwoo Joh[3], Srikanth Krishnan[3], Sameer Pendharkar[3], and Jesús A. del Alamo[1], [1]Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, 02139, U.S.A., [2]Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL, 32816, U.S.A., [3]Analog Technology Development, Texas Instruments, Dallas, TX, 75243, U.S.A.

Session 4F – SY

Wednesday, 3rd April

10:30 AM – Session Introduction

10:35 AM
4F.1 Novel Cumulative Degradation Approach to Predict Components Failure Rates
George Thiel and Flavio Griggio, Hardware Reliability, Microsoft Corporation, Redmond, WA, USA

11:00 AM
4F.2 Operational Workload Impact on Robust Solid-State Storage Analyzed with Interpretable Machine Learning

Jay Sarkar and Cory Peterson, Western Digital Corporation, 5601 Great Oaks Parkway, San Jose, California - 95119, U.S.A.

11:25 AM

4F.3 Evaluating Impact Information Uncertainties on Component Reliability Assessment

Diganta Das[1], Edmond Elburn[1], Michael Pecht[1], and Bhanu Sood[2], [1]Center for Advanced Life Cycle Engineering, University of Maryland, College Park, Maryland, USA, [2]NASA Goddard Space Flight Center, Greenbelt, Maryland

11:50 AM

4F.4 Process Variation of Pixel Definition and Effects of Flexible OLED Luminance Degradation

Jongwon Lee, Sangkil Kim, Yoonsuk Choi, and Jongwoo Park, Technology Reliability, OLED Business Samsung Display Co., 181, Samsung-ro, Tangjeong-myeon, Asan-si, Chungcheongnam-Do, Korea

12:15 PM

4F.5 New Failure Mechanism of Signal Path Damage at the Interface between Two Separated Power Domains in Different Deep N-Wells

Hsi-Yu Kuo, Yu-Lin Chu, Sheng-Fu Hsu, Chuan-Li Chang, Ming-Yi Wang, and Kenneth Wu, Quality & Reliability, HV ESD R & D*, TSMC Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C.*

1:00 PM - Break

Session 5A – SE

Wednesday, 3rd April

02:25 PM – Session Introduction

02:30 PM

5A.1 Soft Error Performance of High-Speed Pulsed-DICE-Latch Design in 16 nm and 7 nm FinFET Processes

B. Narasimham[1], K. Chandrasekharan[1], J. K. Wang[1], and B. L. Bhuva[2], [1]Broadcom Inc, Irvine CA USA, [2]Vanderbilt University, Nashville TN USA

02:55 PM

5A.2 SEIFF: Soft Error Immune Flip-Flop for Mitigating Single Event Upset and Single Event Transient in 10 nm FinFET

Taiki Uemura, Soonyoung Lee, Dahye Min, Ihlhwa Moon, Seungbae Lee, and Sangwoo Pae, Technology Quality & Reliability, Samsung Foundry, Samsung Electronics, Korea

03:20 PM

5A.3 Evaluation of Single Event Effects in SRAM and RRAM based Neuromorphic Computing System for Inference

Zhilu Ye[1], Rui Liu[1], Hugh Barnaby[1], and Shimeng Yu[2], [1]School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ, 85281, USA, [2]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332, USA

03:45 PM

5A.4 Single-Event Upset Responses of Dual- and Triple-Well D Flip-Flop Designs in 7-nm Bulk FinFET Technology

L. Xu[1], J. Cao[1], B. L. Bhuva[1], I. Chatterjee[2], S. -J. Wen[3], R. Wong[3], and L. W. Massengill[1], [1]Vanderbilt University, Nashville, TN 37212, [2]Airbus SE, Germany, [3]Cisco Systems, Inc., San Jose, CA

04:10 PM

5A.5 Negative and Positive Muon-induced SEU Cross Sections in 28-nm and 65-nm Planar Bulk CMOS SRAMs

Wang Liao[1], Masanori Hashimoto[1], Seiya Manabe[2], Yukinobu Watanabe[2], Shin-ichiro Abe[3], Keita Nakano[2], Hayato Takeshita[2], Motonobu Tampo[4], Soshi

Takeshita[4], and Yasuhiro Miyake[4,5], [1]Department of Information System Engineering, Osaka University, Suita, Japan, [2]Department of Advanced Energy Engineering Science, Kyushu University, Fukuoka, Japan, [3]Research Group for Radiation Transport Analysis, Japan Atomic Energy Agency (JAEA), Tokai, Japan, [4]Muon Science Laboratory, High Energy Accelerator Research Organization (KEK), Tokai, Japan, [5]Materials and Life Science Division, J-PARC Center, Tokai, Japan

04:35 PM
5A.6 Exploration of the Impact of Physical Integration Schemes on Soft Errors in 3D ICs using Monte Carlo Simulation
M. L. Breeding[1], R. A. Reed[2], K. M. Warren[2], and M. L. Alles[2], [1]Interdisciplinary Materials Science and Engineering Program, Vanderbilt University, Nashville, TN USA, [2]Electrical Engineering and Computer Science Department, Vanderbilt University, Nashville, TN USA

Session 5B – CR

Wednesday, 3rd April

02:25 PM – Session Introduction

02:30 PM
5B.1 From Device Aging Physics to Automated Circuit Reliability Sign off
Christian Schlünder[1], Katja Waschneck[2], Peter Rotter[1], Susanne Lachenmann[1], Hans Reisinger[2], Franz Ungar[1] and Georg Georgakos[1], [1]Design Enabling & Services Department, Infineon Technologies AG, 85579 Neubiberg, Germany, [2]Reliability & Qualification Department, Infineon Technologies AG, 85579 Neubiberg, Germany

02:55 PM

5B.2 Study of Local BTI Variation and Its Impact on Logic Circuit and SRAM in 7 nm Fin-FET Process

Mitsuhiko Igarashi, Yuuki Uchida, Yoshio Takazawa, Makoto Yabuuchi, Yasumasa Tsukamoto, and Koji Shibutani, Design Platform Technology Department 1, Renesas Electronics Corporation, 5-20-1, Josuihoncho, Kodaira-shi, 187-8588, Tokyo, Japan

03:20 PM

5B.3 Aging-Aware Design Verification Methods under Real Product Operating Conditions

Hyewon Shim, Jeongmin Jo, Yoohwan Kim, Bongyong Jeong, Minji Shon, Hai Jiang, and Sangwoo Pae, Technology Quality & Reliability, Foundry Business, Samsung Electronics, Yongin-si, Gyeonggi-do, 17113, Republic of Korea

03:45 PM

5B.4 Utilizing a Thorough Understanding of Critical Aging and Failure Mechanisms in finFET Technologies to Enable Reliable High Performance Circuits

Bonnie Weir, Vani Prasad, Shahriar Moinian, SangJune Park[1], Joseph Blasko, Jason Brown[2], and Jayanthi Pallinti[3], Broadcom, Inc., Allentown, PA, 18109, USA, [1]Colorado Springs, CO, [2]Fort Collins, CO, [3]San Jose, CA

04:10 PM

5B.5 Investigating the Aging Dynamics of Diode-Connected MOS Devices using an Array-based Characterization Vehicle in a 65nm Process

Nakul Pande[1], Gyusung Park[1], Chris H. Kim[1], Srikanth Krishnan[2], and Vijay Reddy[2], [1]Department of Electrical and Computer Engineering, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455, USA, [2]Texas Instruments 13121 TI Blvd, Dallas, TX 75243

04:35 PM
5B.6 Investigation of NBTI Dynamic Behavior with Ultra-Fast Measurement
F. Cacho, X. Federspiel, D. Nouguier, C. Diouf, and Y. Carminati, STMicroelectronics, 850 rue Jean Monnet 38926 Crolles, France

Session 5C – EL

Wednesday, 3rd April

02:25 PM – Session Introduction

02:30 PM
5C.1 Physical Insights into the Low Current ESD Failure of LDMOS-SCR and Its Implication on Power Scalability
Nagothu Karmel Kranthi[1], B. Sampath Kumar[1], Akram Salman[2], Gianluca Boselli[2], and Mayank Shrivastava[1], [1]Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India;, [2]Texas Instruments Inc, Dallas, USA

02:55 PM
5C.2 CDM-Time Domain Turn-on Transient of ESD Diodes in Bulk FinFET and GAA NW Technologies
S.-H. Chen, D. Linten, G. Hellings, M. Simicic, B. Kaczer, T. Chiarella, H. Mertens, J. Mitard, A. Mocuta, and N. Horiguchi, Department of Technology Solutions and Enablement, imec, Leuven, Belgium

03:20 PM
5C.3 Current Filament Dynamics under ESD Stress in High Voltage (Bidirectional) SCRs and It's Implications on Power Law Behavior
Nagothu Karmel Kranthi[1], Akram Salman[2], Gianluca Boselli[2], and Mayank Shrivastava[1], [1]Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India, [2]Texas Instruments Inc, Dallas, USA

03:45 PM
5C.4 Concise Analytical Expression for Wunsch-Bell 1-D Pulsed Heating and Applications in ESD using TLP
Geert Hellings[1], Philippe Roussel[1], Nian Wang[1], Roman Boschke[1], Shih-Hung Chen[1], Marko Simicic[1], Mirko Scholz[1], Soeren Stoedel[1], Kris Myny[1], Dimitri Linten[1], Paul Hellings[2], and Nowab Reza MD Ashif[3], [1]Semiconductor Technology and Systems Unit, imec, Leuven, Belgium, [2]Faculty of Engineering Technology, KU Leuven Campus GroepT, Leuven, Belgium, [3]Karlsruhe School of Optics and Photonics, Karlsruhe Institute of Technology, Karlsruhe, Germany

04:10 PM
5C.5 Physical Model for ESD Human Body Model to Transmission Line Pulse
Jian-Hsing Lee[1], Natarajan Mahadeva Iyer[2], and Timothy J. Maloney[3], [1]Device Department, VIS Micro Inc., Campbell, CA, USA, [2]Quality and Reliability Allegro Microsystems, Marlborough, MA, USA, [3]Center for Analytic Insights (CAI), Palo Alto, CA, USA

04:35 PM
5C.6 Tunable Holding-Voltage High Voltage ESD Devices
Jian-Hsing Lee[1] and Natarajan Mahadeva Iyer[2], [1]Device Department, VIS Micro Inc., Campbell, CA, USA, [2]Quality and Reliability Allegro Microsystems, 100 Crowley Drive, Marlborough, MA, USA

Wednesday, April 3
Joint Poster Session & Reception
6:00 pm – 9:00 pm
Monterey Ballroom

Session – Joint Poster Session

Wednesday, 3rd April

06:00 PM – Session Introduction

P.CR.1 Modelling Degradation of Matched-Circuits in Operational Conditions: Active and Stand-by Modes
Khai Nguyen and Geoff Liang, Component Level Reliability Engineering NVIDIA Corporation, 2701 San Tomas Express Way, Santa Clara, California, USA

P.CR.2 Reliability Analysis of a Delay-Locked Loop Under HCI and BTI Degradation
Tonmoy Dhar and Sachin S. Sapatnekar, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, 55455, USA.

P.CR.3 Analysis of Random Telegraph Noise (RTN) at Near-Threshold Operation by Measuring 154k Ring Oscillators
A.K.M. Mahfuzul Islam*, Ryota Shimizu[†], and Hidetoshi Onodera[†], **Graduate School of Engineering, Kyoto University, Kyoto Daigaku Katsura, Nishikyo-ku, Kyoto 615-8510, JAPAN, [†]Graduate School of Informatics, Kyoto University, Yoshida-honmachi, Sakyo-ku, Kyoto 606-8501, JAPAN.*

P.CR.4 On the Effect of NBTI Induced Aging of Power Stage on the Transient Performance of On-Chip Voltage Regulators
Venkata Chaitanya Krishna Chekuri, Arvind Singh, Nihar Dasari, and Saibal Mukhopadhyay, School of Electronics and Computer Engineering, Georgia Institute of Technology, Atlanta, GA-30318, USA

P.DL.1 A Novel Constant E-field Methodology for Intrinsic TDDB Lifetime Projection
A.S. Teng, C.W. Lin, M.N. Chang, Aaron Wang, and Ryan Lu, Advanced Technology Quality & Reliability Division, Taiwan Semiconductor Manufacturing Company, Ltd., 121, Park Ave. 3, Science-Based Industrial Park, Hsinchu, Taiwan

P.DL.2 Distinguishing Interfacial Hole Traps in (110), (100) High-k Gate Stack
Yueyang Liu[1], Xiangwei Jiang[1], Liwei Wang[2], Yunfei En[2], and Runsheng Wang[3], [1]State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, P. R. China. 100083, [2]Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, No. 5 Electronics Research Institute of the Ministry of Industry and Information Technology, Guangdong, 510610, P. R. China, [3]Institute of Microelectronics, Peking University, Beijing, P. R. China., 100871

P.DL.3 On the Frequency Dependence of Bulk Trap Generation During AC Stress in Si and SiGe RMG p-FinFETs
Narendra Parihar[1], Uma Sharma[1], Richard G. Southwick[2], Miaomiao Wang[2], James H. Stathis[3], and Souvik Mahapatra[1], [1]Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India, [2]IBM Research Division, Albany Nanotech, Albany, NY, 12203, USA, [3]IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, 10598, USA

P.DL.4 A Realistic Modeling Approach To Explain the Physical Mechanism of the TDDB Weibull Slope with Advanced FinFET Technology Scaling
C. H. Yang, T. H. Tsai, C. S. Kuo, S. Mukhopadhyay, S. C. Chen, Clement Huang, Y. S. Tsai, J. H. Lee, Ryan

Lu, and J. He, Technology Quality & Reliability Division, Taiwan Semiconductor Manufacturing Company, Ltd., 121, Park Ave. 3, Science Park, Hsinchu, Taiwan

P.DL.5 Comparative Analysis of the Degradation Mechanisms in Logic and I/O FinFET Devices Induced by Plasma Damage

Gaspard Hiblot, Yefan Liu, Geert Hellings, and Geert Van der Plas, IMEC, Kapeldreef 75, 3001 Leuven, Belgium

P.DL.6 Tristate Resistive Switching in Heterogenous Van Der Waals Dielectric Structures

Kaichen Zhu[1], Xianhu Liang[1], Bin Yuan[1], Marco A. Villena[1], Chao Wen[1], Tao Wang[1], Shaochuan Chen[1], Mario Lanza[1], Fei Hui[2,3], Yuanyuan Shi[2,3], [1]Institute of Functional Nano & Soft Materials, Collaborative Innovation Center for Suzhou Nanoscience and Technology, Soochow University, Suzhou, 215123, China, [2]Department of Materials Science & Engineering, Guangdong Technion—Israel Institute of Technology, Shantou, China, Department of Materials Science & Engineering, Technion—Israel Institute of Technology, Haifa, Israel

P.EL.1 A Novel HV-NPN ESD Protection Device with Buried Floating P-Type Implant

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P.EL.2 Thin-film FD-SOI BIMOS Topologies for ESD Protection

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P.EL.3 Characterization and Modeling of the Transient Safe Operating Area in LDMOS Transistors

Hang Li[1], Kalpathy B. Sundaram[1], Yuanzhong Zhou[2], Javier A. Salcedo[2], and Jean-Jacques Hajjar[2], [1]Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL, USA, [2]ADI Global Electrostatic Discharge Organization, Analog Devices, Inc., Wilmington, MA, USA

P.EL.4 Design and Optimization of the NAND ESD Clamp in CMOS Technology

Jian Liu and Nathaniel Peachey, ESD Engineering, Qorvo Inc., Greensboro, NC, USA

P.EL.5 Novel RC-Clamp Design for High Supply Voltage

Yuh-Yue Chen, Tsyr-Shyang Liou, and Shyh-Chyi Wong, Richwave Technology Corp., Taipei, Taiwan

P.EL.7 Investigation on Latch-Up Path between I/O PMOS and Core PMOS in a 0.18-μm CMOS Process

Chun-Cheng Chen and Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

P.FA.1 Cr-free Alternatives for Crystal Defect Delineation

Federica Gencarelli and Tony Colpaert, Quality department, ON Semiconductor, Oudenaarde, Belgium

P.MB.1 Low-Frequency Noise Measurements to Characterize Cu-Electromigration down to 44nm Metal Pitch

Sofie Beyne[1,2], Olalla Varela Pedreira[2], Ingrid De Wolf[12], Zsolt Tőkei[2], and Kristof Croes[2], [1]MTM, KU Leuven, Kasteelpark Arenberg 44 bus 2450, B-3001, Leuven, Belgium, [2]imec, Kapeldreef 75, B-3001, Leuven, Belgium

P.MB.2 BEOL Process Development Using Fast Power Cycling on Test Structures

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P.MB.3 Impact of Process Variations on Vertical IMD TDDB Lifetime Extrapolations

S. Jose[1], M. Combrie[1], C. Yin[1], Y. Chen[1], C. M. Hong[1], M. D. Shroff[1], X. L. Zhao[2], X. Zeng[2], F. Zhang[2], and L. Q. Luo[2], [1]NXP Semiconductors, Nijmegen, The Netherlands, [2]GLOBALFOUNDRIES, 60 Woodlands Industrial Park D Street 2, Singapore 738406

P.MB.4 Comparative Study of TDDB Models on BEOL Interconnects for sub-20 nm Spacings

Niaz Mahmud, Nabihah Azhari, and J. R. Lloyd, College of Nanoscale Science and Engineering (CNSE), SUNY Polytechnic Institute, 257 Fuller Road, Albany, NY 12203, USA

P.MB.5 Variation-Aware Physics Based Electromigration Modeling and Experimental Calibration for VLSI Interconnects

Sarath Mohanachandran Nair[1], Rajendra Bishnoi[1], Mehdi B. Tahoori[1], Houman Zahedmanesh[2], Kristof Croes[2], Kevin Garello[2], Gouri Sankar Kar[2] and Francky Catthoor[2], [1]Karlsruhe Institute of Technology, Germany, [2]Imec vzw, Leuven, Belgium

P.MB.6 Current Crowding Impact on Electromigration in Al Interconnects

Young-Joon Park, Jungwoo Joh, Jayhoon Chung, and Srikanth Krishnan, Analog Technology Development, Texas Instruments, Dallas, TX, U.S.A.

P.MB.7 Understanding EM-degradation Mechanisms in Metal Heaters Used for Si Photonics Applications

K. Croes.V. Simons[1], S. Beyne[1], V. Cherman[1], H. Oprins[1], M. Stucchi[1] Ph. Absil[1], A. Glabman[2], and E. Wilcox[2], [1]Imec, Kapeldreef 75, 3001 Leuven, Belgium, [2]FormFactor, 2350 Helen Street, Suite B, North St. Paul, MN 55109

P.MB.8 Verification of Copper Stress Migration under Low Temperature Long Time Stress

Hideya Matsuyama[1], Takashi Suzuki[2], Motoki Shiozu[3], Hideo Ehara[3], Takeshi Soeda[4], Hirokazu Hosoi[4] Masao Oshima[1], and Kikuo Yamabe[5], [1]Socionext Inc., KSP R&D D10F, Kawasaki, Kanagawa 213-0012, Japan, [2]Fujitsu Laboratories Ltd. Digital Co-Creation Project, Kawasaki, Kanagawa 211-8588, Japan, [3]Mie Fuj itsu Semiconductor Ltd., Kuwana, Mie 511-0192, Japan, [4]Fujitsu Laboratories Ltd., Atsugi, Kanagawa 243-0197, Japan, [5]Graduate School of Pure and Applied Sciences, University of Tsukuba, Tsukuba, Ibaraki, 305-8573, Japan

P.MB.9 A Simple Prediction Method for Chip-Level Electromigration Lifetime using Generalized Gamma Distribution

Shinji Yokogawa[1], and Kyosuke Kunii[2], [1]The Info-Powered Energy System Research Center, The University of Electro-Communications, Tokyo, Japan, [2]Graduate School of Informatics and Engineering, The University of Electro-Communications, Tokyo, Japan

P.MB.10 Stress Migration Followed by Electromigration Reliability Testing
J.M. Passage, N. Azhari, and J.R. Lloyd, SUNY Polytechnic Institute, 12203, Albany, USA

P.MB.11 Wafer Level Approach for the Investigation of the Long-Term Stability of Resistive Platinum Devices at Elevated Temperatures
Timo Schössler[1], Florian Schön[1] Christian Lemier[1], Gerald Urban[2], and [1]Robert Bosch GmbH, Automotive Electronics, Reutlingen, Germany, [2]Department of Microsystems Engineering, IMTEK, University of Freiburg, Freiburg, Germany

P.MY.1 Probing Write Error Rate and Random Telegraph Noise of MgO Based Magnetic Tunnel Juction Using a High Throughput Characterization System
Shifan Gao[1], Bing Chen[1], Nuo Xu[2], Yiming Qu[1], and Yi Zhao[1], [1]College of Information Science and Electronic Engineering, Zhejiang University, 310027, Hangzhou, China, [2]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA

P.MY.2 Modeling of Apparent Activation Energy and Lifetime Estimation for Retention of 3D SGVC Memory
Wei-Hao Hsiao, Nian-Jia Wang, Ming-Yi Lee, Li-Kuang Kuo, Ding-Jhang Lin, Yen-Hai Chao, and Chih-Yuan Lu, Macronix International Co. Ltd, No. 16, Li-Hsin Road, Science Park, Hsinchu 300, Taiwan

P.MY.3 Cycling Induced Trap Generation and Recovery Near the Top Select Gate Transistor in 3D NAND
Xingqi Zou[1], Liang Yan[1], Lei Jin[1,2], Da Li[2], Feng Xu[2], Di Ai[1], An Zhang[2], Hongtao Liu[2], Ming Wang[2], Wei Li[2], Yali Song[2], Huazheng Wei[2], Yi Chen[2], Chunlong Li[1], and Zongliang Huo[1,2], [1]Institute of Microelectronics of Chinese Academy of Sciences, China, Beijing, [2]Yangtze Memory Technologies Co., Ltd., China, Wuhan

P.MY.4 eNVM MRAM Retention Reliability Modeling in 22FFL FinFET Technology

James A. O'Donnell, Chris Connor, Tanmoy Pramanik, Jeff Hicks, Juan G. Alzate, Fatih Hamzaoglu, Justin Brockman, Oleg Golonzka, and Kevin Fischer, Intel Corporation, 2501 NE Century Blvd, Hillsboro, OR 97124, USA

P.MY.6 Performance Improvement on HfO_2-Based 1T Ferroelectric NVM by Electrical Preconditioning

C. Cagli[1], L. Perniola[1], F. Gaillard[1], S. Duenkel[2], T. Melde[2], B. Mueller[2], M. Trentzsch[2], S. Wittek[2], and S. Beyer[2], [1]Univ. Grenoble Alpes, CEA, LETI, MINATEC Campus, Grenoble, France, [2]GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany

P.MY.7 Automatic Data Repair Overwrite Pulse for 3D-TLC NAND Flash Memories with 38x Data-Retention Lifetime Extension

Kyoji Mizoguchi, Kyosuke Maeda, and Ken Takeuchi, Department of Electrical, Electronic, and Communication Engineering, Chuo University, Tokyo, Japan

P.MY.9 Program/Erase Cycling Enhanced Lateral Charge Diffusion in Triple-Level Cell Charge-trapping 3D NAND Flash Memory

Rui Cao[1], Jixuan Wu[1], Wenjing Yang[1], Jiezhi Chen[1], and Xiangwei Jiang[2], [1]School of Information Science and Engineering, Shandong University, Qingdao, P. R. China, [2]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, P. R. China

P.MY.10 An Evaluation of X-Ray Irradiation Induced Dynamic Refresh Characterization in DRAM

KyungWoo Lee[1], Chae-Hyuk Yun[2], HyungAh Seo[2], Taehun Kang[2], Yunsung Lee[2], and Kangyong Cho[2], [1]Samsung Electronics., Hwaseong-si, Rep. of Korea, [2]Samsung Electronics., Hwaseong-si, Rep. of Korea

P.MY.12 Characterization and Analysis of Bit Errors in 3D TLC NAND Flash Memory

Nikolaos Papandreou[1], Haralampos Pozidis[1], Thomas Parnell[1], Nikolas Ioannou[1], Roman Pletka[1], Sasa Tomic[1], Patrick Breen[2], Gary Tressler[2], Aaron Fry[3], and Timothy Fisher[3], [1]IBM Research - Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland, [2]IBM Systems, 2455 South Road, Poughkeepsie, NY, USA, [3]IBM Systems, 10777 Westheimer Road, Houston, TX, USA

P.NM.1 Reinforcement Learning System Comprising Resistive Analog Neuromorphic Devices

Song-Ju Kim[1], Kaori Ohkoda[1], Masashi Aono[2], Hisashi Shima[3], Makoto Takahashi[3], Yasuhisa Naitoh[3], and Hiroyuki Akinaga[3], [1]Graduate School of Media and Governance, Keio University, 5322 Endo, Fujisawa, Kanagawa 252-0882, Japan, [2]Faculty of Environment and Information Studies, Keio University, 5322 Endo, Fujisawa, Kanagawa 252-0882, Japan, [3]Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba Central 5, 1-1-1 Higashi, Tsukuba, Ibaraki 305-8565, Japan

P.NM.2 Reliability of CMOS Integrated Memristive HfO_2 Arrays with Respect to Neuromorphic Computing

M.K. Mahadevaiah[1], E. Perez[1], Ch. Wenger[1,2], A. Grossi[3], C. Zambelli[3], P. Olivo[3], F. Zahari[4], H. Kohlstedt[4], and M. Ziegler[5], [1]IHP - Leibniz-Institut für innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany, [2]Brandenburg medical School Theodor Fontane, Fehrbelliner Strasse 38, 16816 Neuruppin, Germany, [3]Dip. di Ingegneria, Università degli Studi di Ferrara, 44122 Ferrara, Italy, [4]Nanoelektronik, Technische Fakultät, Christian-Albrechts-Universität zu Kiel, 24143 Kiel, Germany, [5]Dept. of Microelectronic and Nanoelectronic Systems, TU Ilmenau, 98684 Ilmenau, Germany

P.NM.3 Process-Induced Anomalous Current Transport in Graphene/InAlN/GaN Heterostructured Diodes

Peter F. Satterthwaite[1], Ananth Saran Yalamarthy[2], Sam Vaziri[1], Miguel Muñoz Rojo[1,3], Eric Pop[1,4], and Debbie G. Senesky[1,5], [1]Department of Electrical Engineering, Stanford University, Stanford University, 94305 Stanford, USA, [2]Department of Mechanical Engineering, Stanford University, 94305 Stanford, USA, [3]Department of Thermal and Fluid Engineering, University of Twente, Enschede, 7500 AE, Netherlands, [4]Department of Materials Science and Engineering, Stanford University, 94305 Stanford, USA, [5]Department of Aeronautics and Astronautics, Stanford University, 94305 Stanford, USA

P.NM.4 Tolerance of Deep Neural Network Against the Bit Error Rate of NAND Flash Memory

Md Mehedi Hasan and Biswajit Ray, Electrical and Computer Engineering Department, The University of Alabama in Huntsville, Huntsville, AL, 35899, USA

P.PI.1 Plasma Antenna Charging in CMOS Image Sensors

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P.PI.2 Study of the Mechanical Stress Impact on Silicide Contact Resistance by 4-Point Bending

Yefan Liu[1,2], Hao Yu[1], Gaspard Hiblot[1], Anastasiia Kruv[1,2], Marc Schaekers[1], Naoto Horiguchi[1], Dimitrios Velenis[1], and Ingrid De Wolf[1,2], [1]IMEC, Kapeldreef 75, Leuven, Belgium, [2]Department of Materials Engineering, KU Leuven, Kasteelpark Arenberg 44, Leuven, Belgium

P.PK.1 Ultra-High Efficient Integrated MicroChannel Cooling for Multi-Unit Microsystems

Jiejun Wang[1,2], Tao Wang[1,2], Qiuyan Li[1,2], Yiming Li[1,2], Wenbo Luo[1,2], Yao Shuai[1,2], Chuangui Wu[1,2], and Wanli Zhang[1,2], [1]School of Electro Sci. and Eng., Uni. of Electro Sci. and Tech of China, Chengdu, China, [2]State Key Lab of Electro Thin Film and Integrated Device, No.2006, Xiyuan Ave, West Hi-Tech Zone, 611731, Chengdu, China*

P.PK.2 A Comparison of Environmental Stressing Data and Simulation at the Corner of a Test Chip in a FC-BGA Package

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P.PR.1 Degradation Monitoring --From a Vision to Reality

Evelyn Landman[1], Shai Cohen[1], Noam Brousard[1], Raanan Gewirtzman[1], Inbar Weintrob[1], Eyal Fayne[1], Yahel David, Yuval Bonen[1], Omer Niv[1], Shai Tzroia[1], Alex Burlak[1], and J. W. McPherson[2], [1]proteanTecs, Sderot Hapalyam 2, 3309502, Haifa, Israel, [2]McPherson Reliability Consulting, LLC, 2805 Shelton Way, Plano TX 75093

P.RT.1 Reliability Evaluation of Silicon Interconnect Fabric Technology

Kannan K. Thankappan, Adeel Bajwa, Boris Vaisband, SivaChandra Jangam, and Subramanian S. Iyer, Electrical and Computer Engineering Department, University of California, Los Angeles, CA 90095

P.RT.2 Bilayer Passivation Film for Cu Interconnects on Si Interconnect Fabric

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P.RT.3 Stability of 4H-SiC JBS Diodes under Repetitive Avalanche Stress

Ajit Kanale, Kijeong Han, B. Jayant Baliga, and Subhashish Bhattacharya, Department of ECE, NCSU, Raleigh, NC, USA

P.SE.1 Alpha Particle Soft-Error Rates for D-FF Designs in 16-nm and 7-nm Bulk FinFET Technologies

J. Cao[1], L. Xu[1], B. L. Bhuva[1], S. -J. Wen[2], R. Wong[2], B. Narasimham[3], and L. W. Massengill[1], [1]Vanderbilt University, Nashville, TN, [2]Cisco Systems, Inc., San Jose, CA, [3]Broadcom Inc., Irvine, CA

P.SE.2 Neutron Beam Attenuation through Semiconductor Devices during SEU Testing

S. A. Wender[1], J. M. O'Donnell[1], L. Zavorka[1], and B. L. Bhuva[2], [1]Los Alamos National Laboratory, Los Alamos, NM 87544 USA, [2]Vanderbilt University, Nashville, TN 37235 USA

P.SE.3 Impact of Combinational Logic Delay for Single Event Upset on Flip Flops in a 65 nm FDSOI Process

Jun Furuta, Yuto Tsukita, Kodai Yamada, Mitsunori Ebara, Kentaro Kojima, and Kazutoshi Kobayashi, Graduate School of Science & Technology, Kyoto Institute of Technology

P.SE.4 An Accurate Device-Level Simulation Method to Estimate Cross Sections of Single Event Upsets by Silicon Thickness in Raised Layer

Kentaro Kojima, Kodai Yamada, Jun Furuta, and Kazutoshi Kobayashi, Graduate School of Science & Technology, Kyoto Insititute of Technology, Kyoto, Japan

P.SE.5 Impact of NBTI on Increasing the Susceptibility of FinFET to Radiation

Frank Sill Torres[1,2], Hussam Amrouch[3], Jörg Henkel[3], and Rolf Drechsler[1,2], [1]Group of Computer Architecture, University of Bremen, Germany, [2]Cyber Physical Systems, DFKI GmbH, Bremen, Germany, [3]Department of Computer Science, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany

P.SE.6 Mitigation of Soft Error Rate Using Design, Process and Material Improvements

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P.SY.1 Nonlinear Mixed Model and Reliability Prediction for OLED Luminance Degradation

Kanghyun Choi, Jongwon Lee, and Jongwoo Park, Technology Reliability, OLED Business Samsung Display, 181, Samsung-ro, Tangjeong-myeon, Asan-si, Chungcheongnam-Do, Korea

P.SY.2 Flight Safety Certification Implications for Complex Multi-Core Processor Based Avionics Systems
Jyotika Athavale, Riccardo Mariani, and Michael Paulitsch, Intel Corporation

P.TX.1 Response of Switching Hole Traps in the Small-Area P-MOSFET under Channel Hot-Hole Effect
X. Ju and D. S. Ang, School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore 639798, Singapore

P.TX.2 Positive Bias Instability in ZnO TFTs with Al_2O_3 Gate Dielectric
Pavel Bolshakov, Rodolfo A. Rodriguez-Davila, Manuel Quevedo-Lopez, and Chadwin D. Young, Department of Materials Science and Engineering, University of Texas at Dallas, 800 West Campbell Road, Richardson, TX, USA

P.TX.3 Comprehensive Study for OFF-State Hot Carrier Degrdation of Scaled nMOSFETs in DRAM
Nam-Hyun Lee, Jongkyun Kim, Donghee Son, Kangjun Kim, and Jung Eun Seok, Memory Division, Samsung Electronics, Hwasung, Gyeonggi 445-701, Republic of Korea

P.TX.4 TCAD Simulation on FinFET n-Type POWER Device HCI Reliability Improvement
B. Zhu, E. M. Bazizi, J.H.M. Tng, Z. Li, E. K. Banghart, M. K. Hassan, Y. Hu, D. Zhou, D. Choi, L. Qin, X. Wan, Global TCAD, QRA REL ENG Product, GLOBALFOUNDRIES, Malta, USA 12020 USA

P.TX.5 Fundamental Understanding of Oxide Defects in HfO_2 and Y_2O_3 on GaAs(001) with High Thermal Stability

H. W. Wan[1], Y. J. Hong[1], L. B. Young[1], M. Hong[1], and J. Kwo[2], [1]Graduate Institute of Applied Physics and Department of Physics, National Taiwan University, Taipei, Taiwan, [2]Department of Physics, National Tsing Hua University, Hsinchu, Taiwan

P.TX.6 Experimental Study on Effects of Boron Transient Enhanced Diffusion on Channel Size Dependences of Low Frequency Noise in NMOSFETs

Shuntaro Fujii, Isao Maru, Soichi Morita, and Tsutomu Miyazaki, Process Technology & Development Section, Asahi Kasei Microsystems Corporation, Nobeoka, Japan

P.TX.7 Scaling Behaviour of State-to-State Coupling During Hole Trapping at Si/SiO_2

Xiaolei Ma[1,2], Xiangwei Jiang[1], Jiezhi Chen[2], Liwei Wang[3], and Yunfei En[3], [1]State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, P. R. China. 100083, [2]School of Information Science and Engineering, Shandong University, Qingdao, P. R. China. 266237, [3]Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, No. 5 Electronics Research Institute of the Ministry of Industry and Information Technology, Guangdong, 510610, P. R. China

P.TX.8 BTI Characterization of MBE Si-capped Ge Gate Stack and Defect Reduction via Forming Gas Annealing

H. W. Wan[1], Y. J. Hong[1], Y. T. Cheng[1], M. Hong[1], and J. Kwo[2], [1]Graduate Institute of Applied Physics and Department of Physics, National Taiwan University, Taipei, Taiwan, [2]Department of Physics, National Tsing Hua University, Hsinchu, Taiwan

P.TX.9 GIDL Increase due to HCI Stress: Correlation Study of MOSFET Degradation Parameters and Modelling for Reliability Simulation

Edoardo Ceccarelli[1], Kevin Manning[2], Seamus Maxwell[2], and Colm Heffernan[1], [1]Analog Devices BV, Raheen Bay F1, V94RT99, Limerick, Ireland, [2]Analog Devices Inc., 804 Woburn Street, 01887, Wilmington (MA), USA

P.WB.1 Characterization and Modelling of High Speed Ge Photodetectors Reliability

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P. Grosse[3], D. Roy[1], and J.-E. Broquin[2], [1]STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles cedex, France, [2]Université Grenoble Alpes, CNRS, Grenoble INP, IMEP-LAHC, 38000 Grenoble, France, Université Savoie Mont Blanc, IMEP-LAHC, 74000 Annecy, France, [3]CEA Leti, 17 Avenue des Martyrs, 38054 Grenoble, France

P.WB.2 Stability in Fluorine-Treated Al-Rich High Electron Mobility Transistors with 85% Al-Barrier Composition

Albert G. Baca, B. A. Klein, A. M. Armstrong, A. A. Allerman, E. A. Douglas, T. R. Fortune, and R. J. Kaplar, Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185-1085 USA

P.WB.3 Reliability and Performance Issues in SiC MOSFETs: Insight Provided by Spin Dependent Recombination

James P. Ashton[1] Patrick M. Lenahan[1], Daniel J. Lichtenwalner[2], Aivars J. Lelis[3], and Mark. A. Anders[4], [1]Department of Engineering Science and Mechanics,

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P.WB.4 UV-Assisted Probing of Deep-Level Interface Traps in GaN MISHEMTs and Their Role in Threshold Voltage & Gate Leakage Instabilities

Sayak Dutta Gupta[1], Vipin Joshi[1], Bhawani Shankar[1], Swati Shikha[1], Srinivasan Raghavan[2], and Mayank Shrivastava[1], [1]Department of Electronic Systems Engineering (DESE), [2]Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore, India

P.WB.5 V_{TH}-Hysteresis and Interface States Characterisation in SiC Power MOSFETs with Planar and Trench Gate

Besar Asllani[1,2], Alberto Castellazzi[2], Oriol Aviño Salvado[1], Asad Fayyaz[2], Hervé Morel[1], and Dominique Planson[1], [1]Univ Lyon, INSA Lyon, Univ. Claude Bernard Lyon 1, Ecole Centrale Lyon, CNRS, Ampère, F-69621, France, [2]University of Nottingham, University Park, NG7 2RD, Nottingham, UK

P.WB.6 Novel Gyrotron Beam Annealing Method for Mg-Implanted Bulk GaN

K. Hogan[1], S. Tozier[1], E. Rocco[1], I. Mahaboob[1], V. Meyers[1], B. McEwen[1], F. Shahedipour-Sandvik[1], R. Tompkins[2], M. Derenge[2], Kenneth Jones[2], M. Shevelev[3], V. Sklyar[3], A. Lang[4], J. Hart[4], M. Taheri[4], and M. Reshchikov[5], [1]Colleges of Nanoscale Science and Engineering, SUNY Polytechnic Institute Albany NY, 12203, USA, [2]Army Research Laboratory Adelphi MD, 20783, USA, [3]Gyrotron Technology Inc.

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P.WB.7 Reliability Testing of SiC MOS Devices at 500°C

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Session 6A - FA

Thursday, 4th April

09:00 AM - Session Introduction

09:05 AM
6A.1 New Access to Soft Breakdown Parameters of Low-k Dielectrics through Localisation-Based Analysis
N. Herfurth[1], A. Beyreuther[1], E. Amini[1], C. Boit[1], M. Simon-Najasek[2], S. Hübner[2] F. Altmann[2], R. Herfurth[3], C. Wu[4], I. De Wolf[4], and K. Croes[4], [1]Department for Semiconductor Devices, Technical University Berlin, Berlin, Germany, [2]Center for Applied Microstructure Diagnostics (CAM), Fraunhofer Institute for Microstructure of Materials and Systems, Halle, Germany, [3]R&D Dept. power generation, Siemens, Berlin, Germany, [4]IMEC, *also at Dept. Materials Engineering, KU Leuven Leuven, Belgium*

09:30 AM
6A.2 Use of High Voltage OBIRCH Fault Isolation Technique in Failure Analysis of High Voltage IC's
Chenran Lei, Albert Lee, Qinkan Kang, MinKwang Lee, Seiji Yang, Dan Oliver, and Tu Giao, Power Integrations Inc., San Jose, CA, USA

09:55 AM
6A.3 In-Situ Electrothermal TEM Investigation of Electromigration in Fully Embedded Cu/Co Interconnects
Miji Lee, Dohwan Chung, Hyoyoung Kim, M-J Lee, Moon Soo Lee, Jinseok Kim, Hwasung Rhee, and Sangwoo Pae, Samsung Foundry Business, Samsung Electronics, Gi-Heung, Korea, 17113

10:20 AM
6A.4 Surrogate Model Assisted Design of Silicon Anode Considering Lithiation Induced Stresses

Zhuoyuan Zheng[a], Bo Chen[a], Yashraj Gurumukhi[b], John Cook[e], Mehmet N. Ates[e], Nenad Miljkovic[b], Paul V. Braun[b,c,d], and Pingfeng Wang[a], [a]Dept. of Industrial and Enterprise Systems Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA, [b]Dept. of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA, [c]Dept. of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA, [d]Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA, [e]Xerion Advanced Battery Corporation, 3100 Research Boulevard St. 320, Kettering, OH 45420, USA

10:45 AM
6A.5 Do Solar Proton Events Reduce the Number of Faults in Supercomputers?: A Comparative Analysis of Faults during and without Solar Proton Events
Claire McKay Bowen[1], Nathan DeBardeleben[2], Sean Blanchard[2], and Christine Anderson-Cook[1], [1]Statistical Sciences Group, Los Alamos National Laboratory, [2]Ultrascale Systems Research Center, Los Alamos National Laboratory

Session 6B - PK

Thursday, 4th April

09:00 AM - Session Introduction

09:05 AM
6B.1 Assesement of CPI Stress Impact on IC Reliability and Performance in 2.5D/3D Packages
A. Kteyan[1], H. Hovsepyan[1], J.-H. Choy[2], and V. Sukharev[2], [1]Mentor, a Siemens Business Design-to-Silicon, Yerevan, Armenia, Mentor, a Siemens Business Design-to-Silicon, Fremont, CA, USA

09:30 AM

6B.2 CPI Reliability Challenges of Large Flip Chip Packages and Effects of Kerf Size and Substrate

Zhuo-Jie Wu[1], Manish Nayini[1], Charles Carey[2], Samantha Donovan[2], David Questad[1], and Edmund Blackshear[1], [1]GLOBALFOUNDRIES US Inc., Hopewell Junction, NY 12533, USA, [2]GLOBALFOUNDRIES US Inc., Essex Junction, VT 12020, USA

09:55 AM

6B.3 A Comprehensive Wafer Level Reliability Study on 65nm Silicon Interposer

PremachandranCS, ThuyTran-Quinn, Lloyd Burrell*, and Patrick Justison, GLOBALFOUNDRIESUS Inc., 400 Stone break Road Extension, Malta, and New York 12020 USA, *GLOBALFOUNDRIESUS Inc., 2070 Route 52, Hopewell Junction, NY1253*

10:20 AM

6B.4 PCB Strip Scale Numerical Study on Vacuum Molded Underfill Void Entrapment in FC-POP Devices

Moon Soo Lee, In Hak Baick, Jiyoung Kwon, Minwoo Lee, Byungwook Kim, Miji Lee, Hanbyul Kang, and Sangwoo Pae, Quality and Reliability Team, Samsung Foundry Business, San #24 Nongseo-Dong Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea 446-711

10:45 AM

6B.5 Electromigration Early Failures for Cu Pillar Interconnections with an ENEPIG Pad Finish and Its Suppression

Hideaki Tsuchiya[1], Naohito Suzumura[1], Ryuji Shibata[1], Hideki Aono[1], Makoto Ogasawara[1], Toshihiko Akiba[2], Kenji Sakata[2], Kazuyuki Nakagawa[2], and Takuo Funaya[2], [1]Advanced Device Technology Department, Renesas Electronics Corporation, 751, Horiguchi, Hitachinaka, Ibaraki, Japan, [2]LSI Package Development Department, Renesas Electronics Corporation, 5-20-1, Josuihon-cho, Kodaira, Tokyo, Japan

Session 6C - TX

Thursday, 4th April

09:00 AM - Session Introduction

09:05 AM

6C.1 Array-Based Statistical Characterization of CMOS Degradation Modes and Modeling of the Time-Dependent Variability Induced by Different Stress Patterns in the {V_G,V_D} Bias Space

E. Bury[1], A. Chasin[1], K.-H. Chuang[1,2], M. Vandemaele[1,2], S. Van Beek[1], J. Franco[1], B. Kaczer[1], and D. Linten[1], Hmec, Kapeldreef 75, 3001 Leuven, Belgium, [2]KU Leuven, ESAT-COSIC, Kasteelpark Arenberg 10, bus 2452, 3001 Leuven, Belgium

09:30 AM

6C.2 Modeling the Effect of Random Dopants on Hot-Carrier Degradation in FinFETs

A. Makarov[1], B. Kaczer[2], Ph. Roussel[2], A. Chasin[2], A. Grill[1], M. Vandemaele[3,2], G. Hellings[2], A.-M. El-Sayed[1], T. Grasser[1], D. Linten[2], and S. Tyaginov[2,1,4], [1]Institute for Microelectronics, Technische Universität Wien, Gußhausstraße 27-29, 1040 Vienna, Austria, [2]imec, Kapeldreef 75, B-3001 Leuven, Belgium, [3]ESAT, KU Leuven, Kasteelpark Arenberg 10 bus 2440, B-3001 Leuven, Belgium, [4]A.F. Ioffe Physical-Technical Institute, Polytechnicheskaya 26, 194021 Saint-Petersburg, Russia

09:55 AM

6C.3 Full (V_g,V_d) Bias Space Modeling of Hot-Carrier Degradation in Nanowire FETs

Michiel Vandemaele[1,2], Ben Kaczer[2], Stanislav Tyaginov[2,3,4], Zlatan Stanojević[5], Alexander Makarov[3], Adrian Chasin[2], Erik Bury[2], Hans Mertens[2], Dimitri Linten[2], and Guido Groeseneken[1,2], [1]ESAT, KU Leuven, Leuven, Belgium, [2]imec, Leuven, Belgium, [5]Global

TCAD Solutions GmbH, Vienna, Austria, [3]Institute for Microelectronics, TU Wien, Vienna, Austria, [4]Ioffe Physical-Technical Institute, St.-Petersburg, Russia

10:20 AM
6C.4 Localized Layout Effect Related Reliability Approach in 8nm FinFETs Technology: From Transistor to Circuit
Hai Jiang, Hyunchul Sagong, Jinju Kim, Junekyun Park, Sangchul Shin, and Sangwoo Pae, Foundry Business, Samsung Electronics, San #24 Nongseo-Dong Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea 446-771.

10:45 AM
6C.5 Low-Frequency Noise Reduction in 22FDX®: Impact of Device Geometry and Back Bias
L. Pirro[1], A. Zaka[1], O. Zimmerhackl[1], T. Herrmann[1], M. Otto[1], El M. Bazizi[1], J. Hoentschel[1], X. Li[1], and R. Taylor[2], [1]GLOBALFOUNDRIES Fab1 LLC & Co.KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Saxony, Germany, [2]GLOBALFOUNDRIES Santa Clara, Santa Clara California CA 95054 United States

11:30 AM - Break

Session 7A – WB GaN

Thursday, 4th April

01:00 PM - Session Introduction

01:05 PM
7A.1 Influence of Gate Length on pBTI in GaN-on-Si E-Mode MOSc-HEMT
A.G. Viey[1,2,3],W. Vandendaele[1], MA Jaud[1], R. Gwoziecki[1], A. Torres[1], M. Plissonnier[1], F. Gaillard[1], G. Ghibaudo[2], R. Modica[3], F. Iucolano[3], M. Meneghini[4], and G. Meneghesso[4], [1]CEA-Leti, 17 Avenue des Martyrs, Grenoble, 38054, France, [2]IMEP-LAHC MINATEC, 3, Parvis Louis Néel - CS 50257 - 38016 Grenoble France, [3]STMicroelectronics,

Stradale Primosole 50, 95121 Catania, Italy, [4]University of Padova, Department of Information Engineering, Via Gradenigo 6/B, 35131, Padova, Italy

01:30 PM

7A.2 Gate Stability and Robustness of In-Situ Oxide GaN Interlayer Based Vertical Trench MOSFETs (OG-FETs)

Maria Ruzzarin[1], Matteo Borga[1], Enrico Zanoni[1], Matteo Meneghini[1], Gaudenzio Meneghesso[1], Dong Ji[2], Wenwen Li[2], Silvia H. Chan[3], Anchal Agarwal[3], Chirag Gupta[3], Stacia Keller[3], Umesh K. Mishra[3], and Srabanti Chowdhury[2], [1]Department of Information Engineering, University of Padova, 35131, Padova, Italy, [2]Department of Electrical and Computer Engineering, University of California, Davis, 95616, CA, USA, [3]Department of Electrical and Computer Engineering, University of California, Santa Barbara 93106, CA, USA, [*]Present address: Electrical Engineering, Stanford University, Stanford, California 94305, United States*

01:55 PM

7A.3 Hot-Electron Effects in GaN GITs and HD-GITs: A Comprehensive Analysis

E. Fabris[1], M. Meneghini[1], C. De Santi[1], M. Borga[1], G. Meneghesso[1], E. Zanoni[1], Y. Kinoshita[2], K. Tanaka[2], H. Ishida[2],
and T. Ueda[2], [1]Department of Information Engineering, University of Padova, Padova, Italy, Via Gradenigo 6/B, 35131, [2]Automotive and Industrial Systems Company, Panasonic Corporation, 3-1-1 Yagumo-Nakamachi Moriguchi, Osaka 570-8501, Japan

02:20 PM

7A.4 µs-Range Evaluation of Threshold Voltage Instabilities of GaN-on-Si HEMTs with p-GaN Gate

E. Canato[1], F. Masin[1], M. Borga[1], E. Zanoni[1], M. Meneghini[1], G. Meneghesso[1], A. Stockman[2], A. Banerjee[2], and P. Moens[2], [1]Department of Information Engineering, University of Padova via Gradenigo 6/B, 35131, Padova, Italy, [2]ONSemiconductor, Westerring 15, Oudenaarde, Belgium

Session 7B – MB

Thursday, 4th April

01:00 PM - Session Introduction

01:05 PM
7B.1 Characterization of Critical Peak Current and General Model of Interconnect Systems under Short Pulse-Width Conditions
M. H. Lin, W. S. Chou, Y. T. Yang, and A. S. Oates, Taiwan Semiconductor Manufacturing Company. Ltd.

01:20 PM
7B.2 Reliability of an Al_2O_3/SiO_2 MIM Capacitor for 180nm (3.3V) Technology
J. Gambino[1], D. Allman[1], G. Hall[1], D. Price[1], L. Sheng[2], R. Takada[3], and Y. Kanuma[3], [1]ON Semiconductor, Gresham, OR, USA, [2]ON Semiconductor, Pocatello, ID, USA, [3]ON Semiconductor, Gunma, Japan

01:55 PM
7B.3 Long Term NBTI Relaxation under AC and DC Biased Stress and Recovery
Elnatan Mataev[1], James Stathis[2], Giuseppe La Rosa and Barry P. Linder[1], [1]IBM Systems, 2070 Route 52, Hopewell Junction, NY 12533, USA, [2]IBM Research, 1101 Kitchawan Rd, Yorktown Heights, NY 10598, USA

Session 7C – MY

Thursday, 4th April

01:00 PM - Session Introduction

01:05 PM

7C.1 Understanding and Variability of Lateral Charge Migration in 3D CT-NAND Flash With and Without Band-Gap Engineered Barriers

Andrea Padovani[1], Milan Pesic[1], Mondol Anik Kumar[1], Pieter Blomme[2], Alexandre Subirats[3] Senthil Vadakupudhupalayam[3], Zunaid Baten[4], and Luca Larcher[5], [1]MDLSoft Inc., Santa Clara, CA, USA, [2]Micron, Leuven, Belgium, [3]imec, Leuven, Belgium, [4]Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, [5]DISMI, University of Modena and Reggio Emilia, Reggio Emilia, Italy

01:30 PM

7C.2 Impact of Mechanical Stress on the Electrical Performance of 3D NAND

A. Kruv[1,2], A. Arreghini[2], M. Gonzalez[2] , D. Verreck[2], G. Van den bosch[2], I. De Wolf[1,2], and A. Furnémont[2], [1]Department of Materials Science KU Leuven Leuven, Belgium, [2]imec Leuven, Belgium

01:55 PM

7C.3 Comprehensive Analysis of Data-Retention and Endurance Trade-off of 40nm TaOx-based ReRAM

Shouhei Fukuyama[1], Atsuna Hayakawa[1], Ryutaro Yasuhara[3], Shinpei Matsuda[1,2], Hiroshi Kinoshita[1], and Ken Takeuchi[1,2], [1]Department of Electrical, Electronic and Communication Engineering, Chuo University, Tokyo, 112-8551, Japan, [2]Research and Development Initiative, Chuo University, Tokyo, 112-8551, Japan, [3]Panasonic Semiconductor Solutions Co., Ltd., 1 Kotari-yakemachi, Nagaokakyo, Kyoto, 617-8520, Japan

2018 IRPS Paper Awards to be Recognized at 2019 IRPS

BEST PAPER AWARD

“A novel insight of pBTI degradation in GaN-on-Si E-mode MOSc-HEMT”

W. Vandendaele, X. Garros, T. Lorin, E. Morvan, A. Torres, R. Escoffier,
MA Jaud, M. Plissonnier, F. Gaillard

BEST STUDENT PAPER AWARD

“Degradation of Vertical GaN FETs Under Gate and Drain Stress”

M. Ruzzarin, M. Meneghini, C. De Santi, G. Meneghesso, E. Zanoni,
M. Sun, T. Palacios

BEST POSTER AWARD

“A Multi-bit/cell PUF Using Analog Breakdown Positions in CMOS”

K.-H. Chuang, E. Bury, R. Degraeve, B. Kaczer, T. Kallstenius, G. Groeseneken,
D. Linten, I. Verbauwhede

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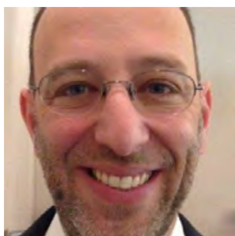

Conference Manager
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FinFET Reliability Workshop Summary

Moderators:

- Chetan Prasad (Intel Corp.)
- Souvik Mahapatra (IIT Bombay)

Background

FinFET devices have become the workhorses of advanced technology nodes, providing improved electrostatic control and power vs. performance trade-offs compared to their planar counterparts. As a consequence of the 3D nature of these devices, they exhibit a higher inherent physical complexity with respect to the reliability mechanisms. This workshop intends to focus on a list of topics that span transistor aging degradation, self-heating impacts, oxide failures and other associated modes unique to FinFET devices.

Attendance

Attendee Count ~ 43 (balanced attendance, with over 30% each from universities and industry).

Discussion Details

Moderators introduced themselves and reviewed the list of discussion topics.
A question was raised on whether we should be concerned about how MOL effects are made worse by FinFETs, but no further discussion occurred on this topic.

Concerns about Translating Aging Results from Device to Circuit Level

- Concern was expressed that all the "doom and gloom" scenarios were at device level, but many sources were not seeing practical circuit level fallout that matched these negative expectations.
- Circuit resiliency and driver strength: need to be comprehended.
- Tool challenges: there seem to be some limited studies, where teams have taken device degradation statistics and implemented custom models, but there seem to be no clear off the shelf options.
- Impact assessments can be broadly classified into two areas: parametric shift (aging), and non-parametric shift (oxide BD). There are probabilistic models for latter, which is a non-deterministic effect (much more complex to implement in circuit modeling).
- Calibration: Critical to understand how calibration to circuit data is done (experimentally speaking). From simulation perspective, how important is it to know the details of the use conditions.
- Impact difference: SBD for retention flop or SRAM are very different in impact than for RO – ckt failure is very topology dependent. This could open up the option to treat different IP blocks independently – but it wouldn't change device level characterization expectations or efforts. Bridging these two is what is essential.

Bridging the Gap through a Change in Benchmarks?

- Considering NAND/NOR characterization (all modes): the results depends on applications; one possibility is to convince foundry customers that such IP blocks would be better benchmarks vs. single devices.

- In-situ monitoring: this is a great option to not need to know the underlying physics, but to instead get empirical data that helps drive the desired lifetime result. Regarding the concerns from Si area/power impact perspective, new techniques exist that are less impactive.
- Performance guys always have a standardized set of benchmarks – could not reliability do the same? Maybe drive it through JEDEC, with an aim to treat digital/analog/AMS/IO/etc. separately.
- Could benchmark circuits that are aligned across the industry help address this? Could in-situ aging monitors themselves be these benchmarks?
- ***Giuseppe LaRosa is the main contact for this, and will try to drive this through his HC spec efforts.***

Aging from an IP Qualification Perspective

- Foundry perspective: L1 and L2 qualifications are the standard. L2 tends to stress an integrated vehicle that looks product like (mainly SRAM and some latch chains). However, the challenge is everything is zero fails – which does not allow for any form of model development.
- Foundry response: qualification is not driven by any device level to circuit level translations. The use of SRAM as the integrated vehicle of choice is because it is well established and easy to implement. Realistically, foundries want to do the minimum activity that ensures that the qualification is done.
- HTOL for IP qualification: Lot of design houses rely on HTOL for IP qualification, but the challenge is zero defect sampling. Pre- and post-HTOL characterization is done, but degradation depends strongly on vectors and visibility. Not all patterns show the "right" results.
- All of the above approaches deal with bottoms-up view. A thought was raised to see if a tops-down approach may work. Could we do this with big data analytics and use large IP blocks and multiple vectors to get the translation to device level?
- Other challenges: product IP is owned by the customer and foundries have no access to it (in many cases). Since aging depends on topology, standard vehicles like SRAM may not capture enough.

Aging in New Market Areas

- There was some discussion on non-digital constructs: conventional digital/analog aging impacts are better known, but other new areas such as machine learning (ML) and artificial intelligence (AI) could be much more tolerant to failures. Does this signify a new paradigm for how we approach reliability in these areas?
- Response: this is not fundamentally different from certain cases such as wireless buffers, where the air re-transmit rates can define the failure tolerances. Could the ML and AI areas just be treated through a use condition approach, but at a higher level? The core idea would be to reflect the tolerance of AI/ML and the corresponding intolerance of ADAS/FuSa use conditions.
- The above discussion led to the concept of whether the standardization of mission profiles across the industry could be considered as well? The main inputs for this would be from the design customers, but if parity is achieved, it could improve the understanding of envelopes significantly.
- ***Could this be as a branch of JEDEC action?***

Workshop on BEOL and CPI

Moderators:

- Jeff Gambino (On Semi)
- Zhuojie George Wu (Globalfoundries)

Background

For leading edge devices, achieving acceptable interconnect reliability for electromigration and time-dependent dielectric breakdown (TDDB) becomes more challenging with each technology node. For all technologies (even mature technologies), package reliability is always a challenge, especially in automotive applications, where use conditions are at higher temperatures and longer times compared to consumer products. In this workshop, we will discuss the following.

Discussion Topics & Summary

1. Electromigration
    a. 5nm node and beyond; Do we need alternative metals or is Cu good enough?
    "Cu works fine in 7nm. Current design rules are conservative and there is margin." Wafer fab perspective: "We actually don't know how big the margin is". The consensus is that we need Co for 5nm node and beyond. (for lower resistance, as well as longer EM lifetime).
    b. What is the electromigration mechanism in p-type materials such as Ru?
    Good discussion on conduction mechanism of p-type metals.. It is argued that it is not hole conduction in valence band. Rather, it is conduction of electrons with negative effective mass. Ru can change from p-type to n-type upon stress condition. Similarly, the effective charge number Z of Co can also change sign at elevated temperature. Does it matter? we all agree that Ru has improved reliability vs Cu.*
    c. How to account for localized heating effects?
    Thermal cycle induced from self-heating is more of a concern than constant high temperature. It can cause void formation from metal fatigue. Temperature-aware EM check can be used to confirm reliability at high constant temperature. But the temperature gradient may cause additional atomic flux and result in void formation. Hot spot size is also important. Large hot spots are of more concern than small hot spots. But no good definition on how big is big. It also depends on circuit; Low duty cycle circuits are of more concern for thermal cycle effects.
2. BEOL Time-Dependent Dielectric Breakdown (TDDB)
    a. What is the best model to use for TDDB?
    Model lifetime prediction diverges only in low field. Multi-year TDDB stress performed at IBM, IMEC, Suny Poly suggest power law, square root E and lucky electron can fit data. Mechanisms for high E stress and low E stress not necessarily the same. It is believed

that physical mechanism is bond breaking rather than Cu drifting since metal with liner only or Co also has TDDB fail, although it takes longer than Cu.

b. How to account for process variation? (CD variation, line-edge roughness, etc.)
Method to account for process variation varies from company to company. Reconstruction method has been used to account for LER bu may not be applicable to BEOL. Models assume infinite variation which is pessimistic, because in reality distribution is truncated since it is limited by process control spec.

3. Chip-Package Interaction (CPI)
   a. How to relate test structure data to product lifetime predictions, especially considering that most fails are due to extrinsic mechanisms?
   No discussion due to time limit
   b. Is there a way to electrically detect and screen “weak” solder bump structures or “weak” wire bond structures?
   No discussion due to time limit

DFR/DFRT

Moderators:

- Nilanjan Mukherjee (Mentor Graphics)
- Vincent Huard (Dolphin Integration)

The content isn't available at the time of publication. Please check the updates on https://irps.org/program/workshops/

GaN/GaN-on-Si Workshop

IRPS

Moderators:

Sameh Khalil, Infineon Technologies
Sandeep Bahl, Texas Instruments

Invited Experts:
Ronald Barr: Transphorm
Charles Cheung, NIST

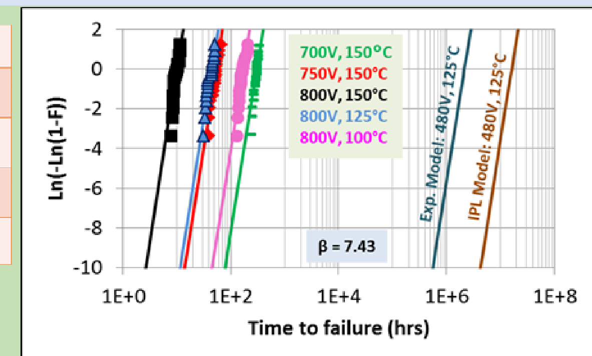
Extrinsics in GaN TDB (HTRB): Synergies between GaN and Si/SiO_2 Reliability

IRPS
International Reliability Physics Symposium

Intrinsic

- Reliability of GaN under HTRB condition follows Time-Dependent-Breakdown-Like behavior analogous to the Si/SiO_2 system
- GaN Lifetime prediction methodology is also derived from Silicon dielectric reliability

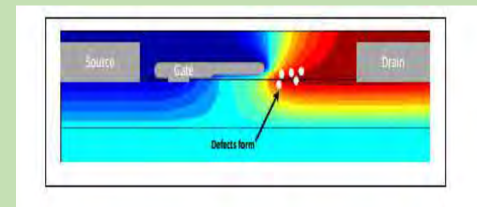
Temp Leg	Voltage Leg 700V	Voltage Leg 750V	Voltage Leg 800V
100°C			x
125°C			x
150°C	x	x	x



H. Kannan et al. (Infineon) WiPDA 2017 & IRPS 2017

Extrinsic

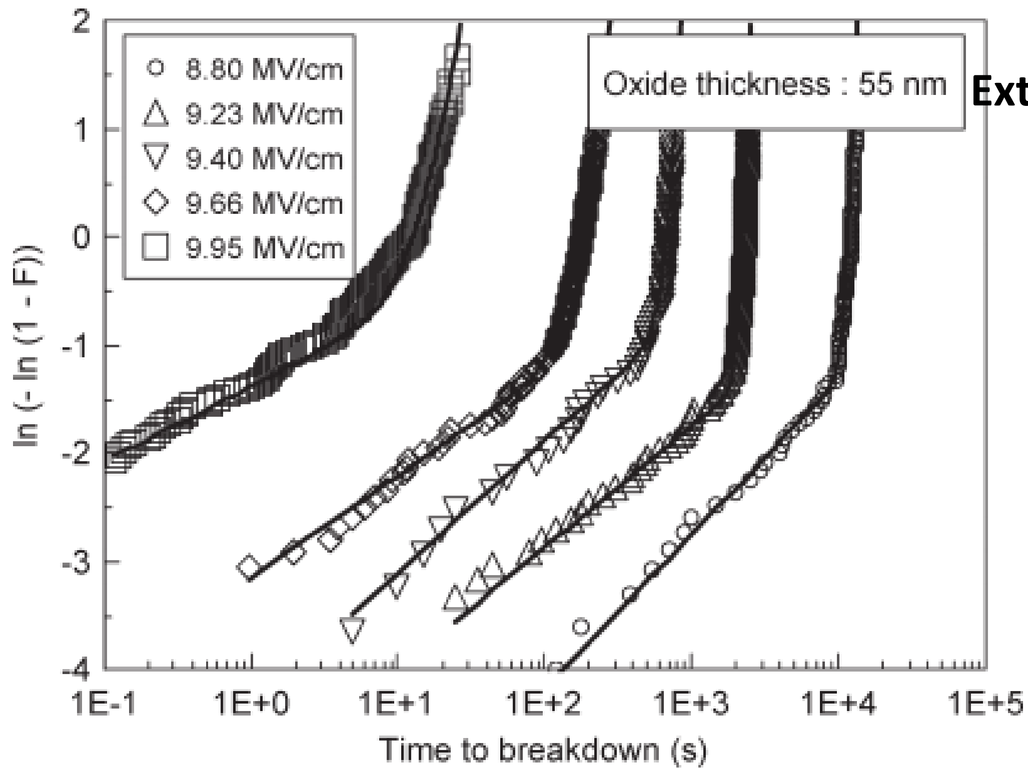
- New topic to GaN publications/literature
- Paper at WiPDA 2018 by Transphorm was first to address Extrinsic in GaN



Ronald Barr et al. (Transphorm) WiPDA 2018

Our Objectives today:

- Discuss the synergies between GaN reliability and Si/SiO2 system (or gate dielectric of Si) from **extrinsic TDB** reliability stand point
- What kind of learning and knowledge from the Silicon world need to be leveraged and applied to GaN Reliability so we do not re-invent the wheel!



Extrinsic gate oxide TDDB failure:

Large sample size required

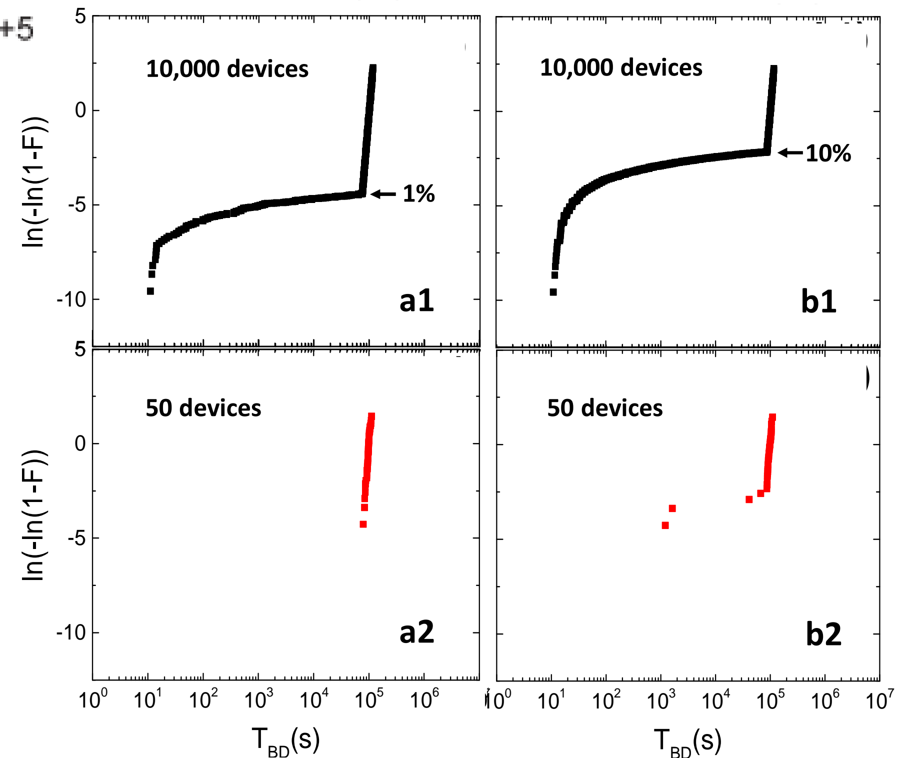
Analyzed by joint distribution

Controls lifetime even after screening

Weibull factor $\beta < 1$

➔ area and probability scaling issues

S. Oussalah and B. Djezzar, TED54(7), 1713(2007)



Small sample size can fool you!!!

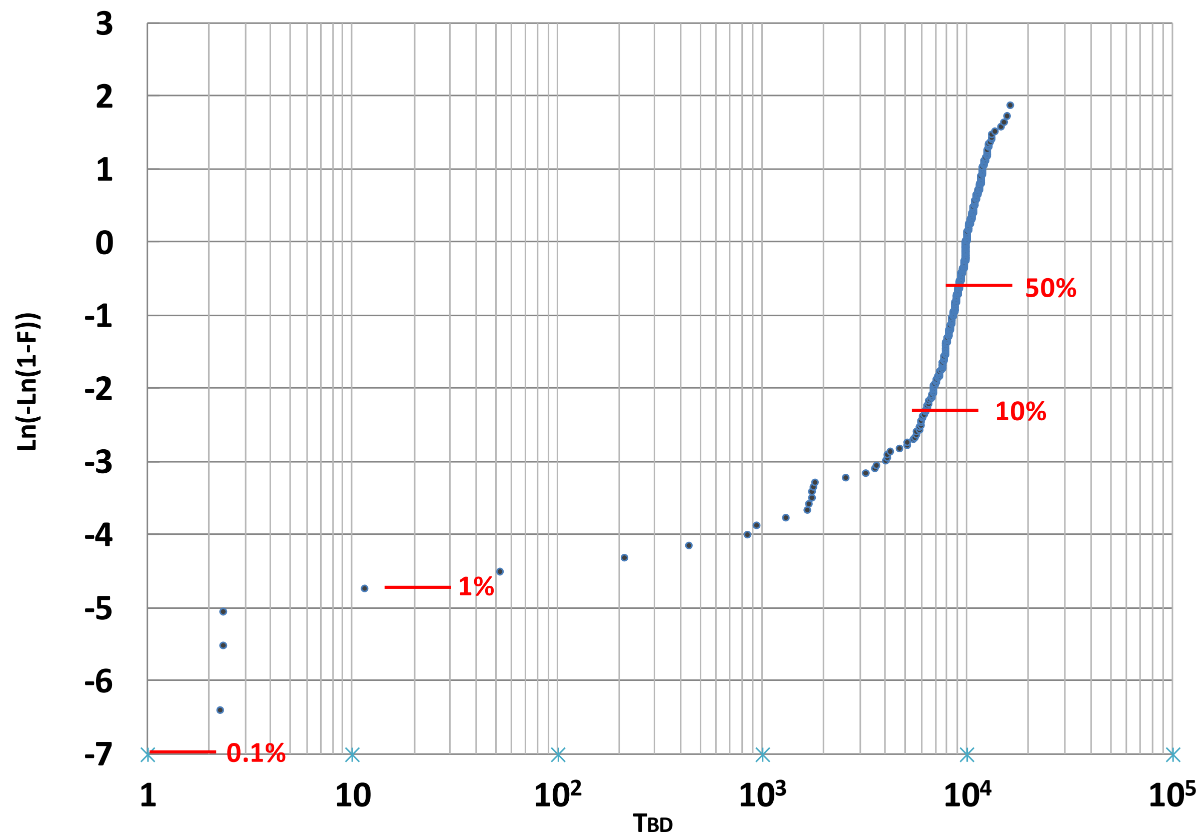
Silicon experience should be taken with care

Recent silicon gate oxide reliability literature are not applicable for thick oxide

Silicon thick oxide extrinsic failure problem were never understood.

Only model is the effective thinning model which does not explain data well

For SiC gate oxide, this was learnt the hard way.



The significance of Weibull slope β

Failure fraction scaling: $\tau_{F1} = \tau_{F2}\left(\frac{\ln(1-F_1)}{\ln(1-F_2)}\right)^{1/\beta}$ **Active area scaling:** $\tau_{63}^{P} = \tau_{63}^{T}\left(\frac{A_T}{A_P}\right)^{1/\beta}$

	β = 0.5	β = 15
From characteristic failure time (t_{63}) to 0.63% failure time:	T_{63}/10000	T_{63}/1.36
From 100µ x 100µ test structure failure time to 10 cm^2 product failure time:	10 billion times shorter	2.15 times shorter

For intrinsic lifetime of thick oxide, *t_{63}@E* of any size test device is adequate.

For extrinsic lifetime of any oxide, failure fraction and test device area must be accounted for.

Problem: Temperature Acceleration Alone to demonstrate ELF FIT<1 requires large number of parts/resources define FIT

Sample Size Required for 1 FIT @ 85C HTRB @150C @Operating Voltage	
Eaa	**# Parts**
1.0	6,286
0.7	28,008
0.5	75,839
0.3	205,355
0.1	556,052
0.0	915,000
-0.1	1,505,659
-0.3	4,076,974
-0.5	11,039,493
-0.7	29,892,371
-0.9	80,941,563
-1.0	133,191,711

 # Parts needed based on standard HTRB testing for 1000 hrs per test

Silicon (← 0.7 / 28,008)

Power Electronics run at relatively **high temperatures,** reduces acceleration factor of standard HTRB testing

Eaa differs from silicon, and between GaN Suppliers

Solution: GaN does not avalanche enabling Voltage Accelerated Early Life Failure Test

Test Conditions
HTRB @800V @ 85C
(Transient voltage rating)
“Gentle acceleration”

~2.2K Devices
~1.1 million device test hours
Zero Failures

TP65H050WS: Generation 3

	FIT	MTBF (hours)	Accelerated Hours	
520 V	0.60	2E+09	2E+09	Max Operating Voltage
480 V	0.21	5E+09	4E+09	
400 V	0.03	4E+10	3E+10	Typical Use Case

@ 85C (Normal Use Temperature)

V model (most conservative) used for calculations
AFv = exp (ϒ x ΔV) = exp(.026 x ΔV)
Based on published data

Question for IRPS panel

- The silicon industry has been using temperature acceleration to define ELF (Early Life Failure) data for years. GaN is well suited to the use of voltage acceleration either alone or in combination with temperature acceleration as it does not avalanche like a silicon MOSFET.
- **What additional data would need to be developed to demonstrate reliability and gain confidence with end users?**

Yield – Reliability Correlation

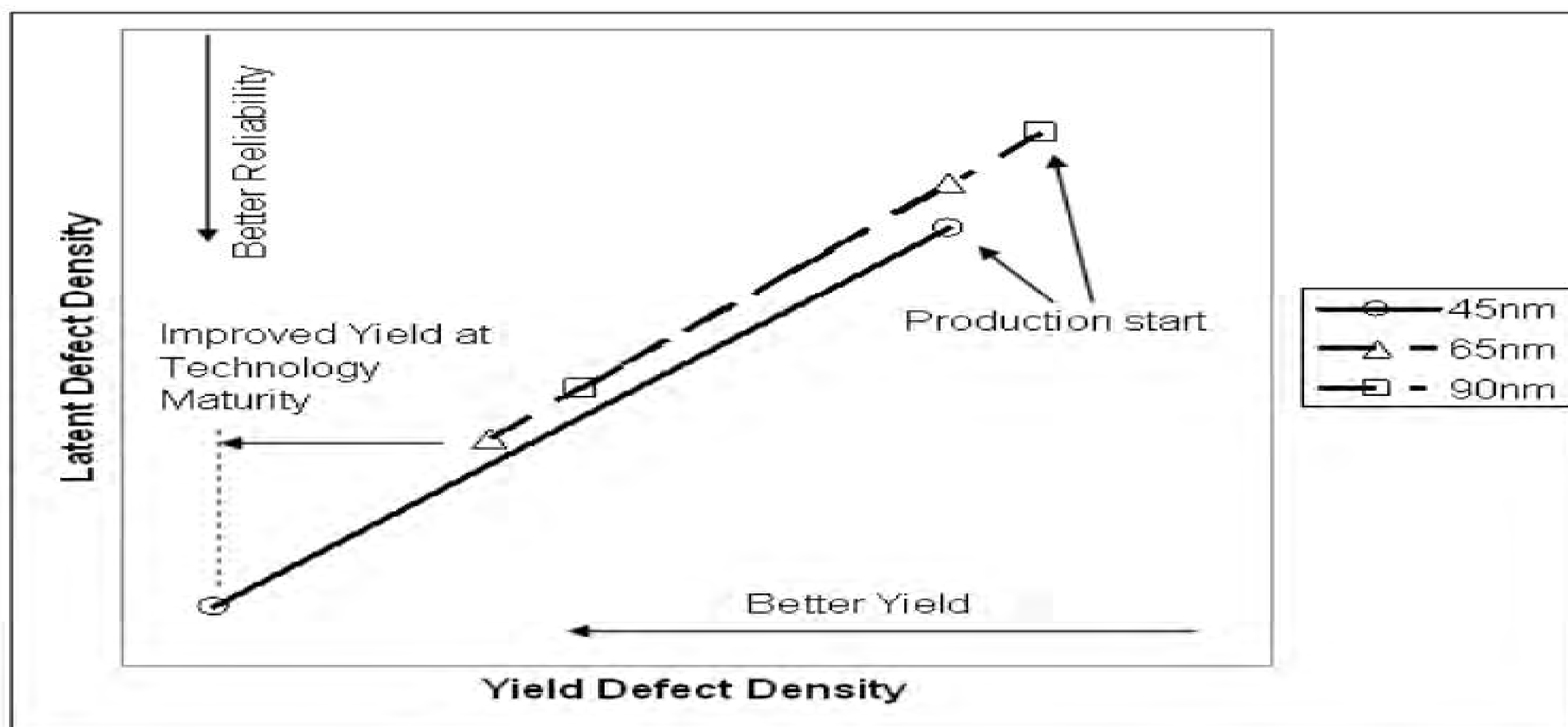


FIGURE 10. BURN-IN DEFECT DENSITY AS A FUNCTION OF PROCESS YIELD DEFECT DENSITY

R. Kasim et al., IRPS 2009 (Intel Corp.)

3D NAND

Moderators:

- Xiaoyu Yang (Western Digital Corp)
- Wei-Chen Chen (Macronix)

Background

When we transfer from 2D to 3D NAND technology, one big advantage is less WL/WL coupling. This enables X4 technology with 3D NAND. However, as 3D NAND Flash is expected to see more than 200 stacked layers in the future, technological solutions to ease the scaling challenges are deemed indispensable. The Z-direction pitch (i.e. gate pitch) shall be reduced to maintain a reasonable string length for the sake of current and for ensuring an easier control of the etching profile of the memory hole. The associated implications would be more severe cell-to-cell interference. In additional, for the mainstream CTF-type (charge trapping Flash) 3D NAND, the charge trapping layer is shared among the cells, meaning that the charge lateral migration and the fast charge loss effect will be more profound once the cell-to-cell distance is made shorter. This causes wider cell Vt distribution and it becomes more serious for X4 which requires much tighter Vt distribution. Other undesired consequences include more daunting metal gate filling. This may result in challenge on the performance. Other prospective challenge for 3D NAND is stress/ wafer warpage; as well as polycrystal channel and gate dielectric/interface quality when the stacking is higher.

Discussion Topics

In this workshop, we will focus our discussion on cell interference and charge loss/gain physical mechanism. We may discuss some of the pressing issues and the way going forward.

Summary

Detailed questions and discussions:

1. How many more stacking layer to expect before the cost benefit of 3D NAND is lost?

-The current trend of continuous increase of the layer number does not see a clear showstopper in the sense that the low sensing current is still manageable and stress-induced warpage can be alleviated via proper processing schemes. Meanwhile, 500 is forecast to be the ultimate layer number when the bit cost is no longer scalable.

2. What are the device impacts of charge lateral migration and fast charge loss?

-From a material perspective, there have been a few papers via simulation discussing the possibility of doping the SiN film with proper atoms to alter the electron migration mobility within the film, which could help retard the detrimental effect of charge migration and charge loss.

-From an electric perspective, complicated programming algorithms and patterns can be applied to deal with this effect. As an example, as opposed to the typical full-sequence PGM, coarse-fine based PGM

algorithm combined with WL-iteration is one effective way to tackle the fast charge loss and interference effects.

3. What are other reliability issues 3D NAND might encounter?

-GIDL-induced ERS was raised as one possible concern because cell-to-cell ERS variability has been reported to be significant as it takes a relatively long period of time (ms) to boost the channel potential and cells in the vicinity of CSL/BL junctions tend to exhibit faster ERS performance than those further away from CSL/BL.

-Now that QLC functionality has been demonstrated, quintuple-level-cell seems the next step forward in further pushing the cell density. However, this needs to be achieved along with a more advanced ECC and a better control of cell behavior. No clear sign on how this will proceed at this moment.

-Research institutes have studied the use of channel materials apart from Si in an attempt to enhance the string current in light of the ever-increasing string length. However, most attendees agreed that the feasibility is quite low in the case of non-Si technology. To meet the possible requirement of extremely low sensing current, innovative sensing schemes should be utilized.

System Reliability

Moderators:

- Scott Hareland (Medtronic)
- TBD

Background

In many modern system designs, the system of interest may be dependent upon a larger system-of-systems for its performance, functionality, and operation. Some simple examples of this are the need for a medical care facility (hospital system) to operate on the National or Regional Power Grid or streaming video or e-commerce services to require that the internet is up and functioning. Even though the system team is tasked to design the system of interest to serve the needs of the stakeholders, that same team may have little, or zero, influence on the other systems in the system-of-systems context that may be key for the reliability of the system they are developing.

Discussion Topics

In light of a system designer's dependence on external forces and entities that are outside of their domain of control or influence, the workshop will discuss some strategies for providing high reliability systems in this context. Hospitals, as life sustaining operations, address their dependence on the power grid by maintaining backup power capability. Non-life-critical systems may simply choose to be unavailable if the larger system is down. The success of a system to operate, even in a reduced capacity, when other systems are unavailable is a consideration that should be evaluated and considered as part of a system reliability analysis and mitigation approach. The workshop will discuss system reliability issues in this area.

UTB SOI Transistor Reliability

Moderators:

- Tanya Nigam (Globalfoundries)
- Vincent Huard (Dolphin Integration)

Background

High Power computing and other products are driving towards FINFET based technology solutions in scaled nodes. But market segments targeted towards low power, low cost and RF are eyeing the UTB SOI roadmap for future products. UTB offers similar advantages as FINFET for controlling SCEs but in addition the Vt can be tuned using back bias allowing lower Vmin. UTB specific reliability challenges include optimizing high voltage devices, Hot Carrier induced degradation, modeling and calibrating self-heating during operation and accelerated reliability testing. The role of back bias in reliability needs careful modeling too. One of the many interesting question in UTB SOI is, can back bias be used for minimizing end-of-life degradation to eliminate product failure. It is important to identify which mechanisms benefit from back bias and which are neutral to it. Some of the key challenges which are shared in bulk FINFETs and UTB SOI is variability. Role of time-zero variability versus degradation induced variability also needs to be quantified and modeled.

Discussion Topics

Please join us on Tuesday evening for an exciting discussion on UTB SOI Transistor reliability. We encourage you to bring your energy, thoughts and technical insight to make this workshop a success.

- Discuss failure mechanisms which require careful technology optimization in UTB SOI
- Impact of self-heating on reliability in SOI UTB
- Impact of Back bias on reliability
- Sources of variability at T0 and post stress

TSV and Advanced Packaging

Moderators:

- Kristof Cores (imec)
- Kangwook Lee (SK hynix)

Background

We would like to have discussions on reliability issues that need to be addressed in advanced packages, with focus on TSV and 2.5/3D. Main questions we want to answer: What are the reliability issues we need to look into? How about testability? Do we need to come up with new tests or do the standard tests apply? How about failure localization/detection? Is the development of new FA-methods needed?

Discussion Topics

To make sure we have enough time to have in-depth discussions, we propose to focus on the following topics (the first two are related to a specific technology, the last two are more general and applicable to different applications)

- TSV
- Wafer-to-wafer bonding
- Fine pitch multi-layer Cu RDL
- Thermal and thermos-mechanical issues in large packages

Summary

After the introduction of the TSV and advanced packaging trends and main their challenges by the moderators, discussions were mainly centered around "High Reliability" of TSV integration, wafer bonding and fan-out packages.

Reliability concerns of TSV integration were discussed for both for via-last and via-middle TSVs. Major reliability concerns are metal migration and thermo-mechanical issues by the Cu TSV with the via middle approach and plasma damage during M1 exposure with the last approach. One attendee questioned TSV design rule (KOZ) to avoid the impact of TSV. It was agreed TSV-EM, at current dimensions, is not the biggest concern. Revision of current JEDEC-standards might be appropriate as well.

Main reliability concerns for W2W stacking were Cu migration (if pitch becomes too small), EM issues due to dielectric layer-Cu electrode contact and delamination issues between dielectric layer and Cu electrode, including particle problems.

One attendee raised a question about impact of contact open size on Cu bump reliability.

Package thermals are raised as a general concern to manage advanced 2.5D/3D packaging solutions.

As suggestions for next year:

1. Maybe making an attendance-list would be good?

2. Maybe doing a 10-15’ briefing before the workshop would be good to get all moderators in the same room and on the same pitch.

IRPS2019 Circuit Reliability Workshop

Reliability Simulation

Georgios Konstadinidis (Google), Jim Tschanz (Intel)

Workshop was well-attended (~50 participants) with good participation from the group. There was also a wide variety of expertise and perspectives (circuit designers, EDA experts, product reliability, foundry, etc.)

Background/Motivation:

- Circuit designers need to deal with multiple reliability mechanisms (BTI, HCI, TDDB, EM, fin self-heat, etc.) while meeting challenging product power/performance/cost constraints.
- Most reliability models and designer "rules of thumb" are based on DC device reliability characterization. However circuits behave very differently, leading to a gap in circuit reliability compared to device predictions.
- Circuit reliability is strongly impacted by physical design, signal timing and slopes, etc. CAD flows are needed which capture this level of detail, while running efficiently on large designs.

What are the largest challenges? Consensus is that this is a major challenge, so we should address the largest gaps first. Several attendees pointed to electromigration as the toughest challenge, where there are significant differences in circuit EM and product specifications, and the lack of clear failure specifications. There was a proposal to build and characterize EM benchmark circuits to better understand current EM margins. Other attendees felt that BTI and HCI were the largest gaps, especially when impact of process variation is considered. Special circuits (high-speed analog, high-frequency clock trees) were discussed as key limiters when aging is considered.

Potential solutions include building more reliability information into the library itself and into the Spice models. While this is effective for analyzing individual circuits, it isn't feasible for block-level or product-level reliability validation: top-level CAD flows are needed here. More circuit benchmarks can also be built to study reliability of key circuits and understand whether margins are set correctly. There was some discussion about the challenging nature of the foundry business – foundries are obligated to provide good parts which meet all specifications, so they typically are very conservative with reliability models. Some customers develop their own reliability models to remove this conservatism. CAD vendors have difficulties dealing with the encrypted models from foundries, which make debug of issues very difficult.

Next steps: There was general agreement from the entire group that these circuit reliability challenges/gaps are real and need to be addressed. There was also agreement that discussing this once per year for an hour at IRPS isn't enough. Some suggestions include holding a longer (4 hour?) IRPS "side event" where these topics can be explored in more detail, as well as potential IRPS focus sessions (similar to this year's CAD invited talks) on reliability simulation and circuit reliability flows.

SiC Power Device Reliability-- Squeezing the most out of SiC chips

Moderators:

- Nando Kaminski (Univ. of Bremen)
- Anant Agarwal (The Ohio State Univ.)

Background

SiC chips have reached an excellent level of performance and reliability and in some areas they already approach the theoretical limits given by the material. Of course, there remain some issues like threshold voltage drift and low channel mobility. However, the real obstacles for the SiC technology originate from the packaging.

SiC is much stiffer than silicon and, thus, soldering and wire bonding provide a significantly lower power cycling capability, if no counter measures are taken. This issue also compromises the high temperature capability of the devices, which usually goes together with enlarged temperature swings.

Another issue is parasitics, i.e. stray inductances and stray capacitances in the package and the surrounding circuitry. Together with the extremely fast switching the SiC chips provide, stray inductances can drive the devices into avalanche or trigger oscillations, which make the devices uncontrollable. Even worse, stray capacitances can cause false triggering, which can lead to a phase shoot through.

Discussion Topics

All this can overstress the SiC chips or can compromise their reliability, although it is rather a packaging than a chip issue. In the workshop, these packaging induced issues (i.e. low power cycling capability and parasitics) and their impact on the device reliability will be discussed.

Summary

"Squeezing the most out of SiC chips" was the motto of a workshop on SiC devices. SiC chips have reached an excellent level of performance and reliability and in some areas they already approach the theoretical limits given by the material. However, packaging related issues turn more and more into obstacles for a better utilisation of the SiC technology. SiC is much stiffer than silicon and, thus, soldering and wire bonding provide a significantly lower power cycling capability. Counter measures are available but increase process complexity and cost just to be on a par with silicon. Package induced parasitics was another topic. The extremely fast switching of SiC chips together with stray inductances can drive the devices into avalanche or trigger oscillations, while stray capacitances can cause false triggering. The about 20 participants agreed widely with these statements, so there was not much dispute. The discussion became a bit livelier when the workshop went on to the long-term subject threshold instability. What is acceptable for circuit designers and what is not? It was again widely agreed that the threshold drift is crucial, while the hysteresis is rather annoying. In any case, there will be surely further discussion at future IRPSs!

STT-MRAM

Moderators:

- Tetsuo Endoh (Tohoku Univ.)
- Junghyuk Lee (Samsung)

Background

Current embedded memory such as SRAM and e-Flash memory face serious issues such as large power consumption and small process margin with CMOS logic. To overcome the issues, STT-MRAM becomes one of key solution and its risk mass production has already started from many major foundries. On the other hand, STT-MRAM has some technical challenge, similar to the other memory technologies.

Discussion Topics

In this workshop, we would like to guide the attendees to discuss the potential of STT-MRAM, the technical challenges, such as soft error rate events, including WER (Write Error Rate) and RDR (Read Disturb Rate) errors of STT-MRAM, and issues for its mass production.

Summary

The most interesting topic was how to achieve good endurance and good retention reliability at the same time. MRAM scaling down was considered to be one of the possible solutions since MRAM efficiency tends to keep improving as scaling down continues.

However, etch damage should be avoided in order to take advantage of scaling down, otherwise MRAM degradation might reach untolerable level.

Attendees agree that many companies are already at the point of initiation of mass production stage.

Malicious magnetic attack could be one of the serious issues when MRAM product enters the consumer markets such as hand held device applications.

Magnetic shield or system level assist also needs to be considered for the success of MRAM products.

Neuromorphic

Moderators:

- Gennadi Bersuker (Aerospace Corp)
- Pey Kin Leong (SUTD)

Background

The aim of this workshop is to connect reliability and neuromorphic communities – the latter outlines device parameters/characteristics relevant to NC operations at the device, as well as circuit and system, levels that help reliability experts and scientists to better formulate related measurements.

What is the scope of device reliability in neuromorphic applications?

At this stage of technology development, it is constructive and timely to widen considerations beyond conventional degradation: Reliability study is expected to address any features/variabilities in device characteristics that detrimentally affects NC operations. The reliability question of practical importance is, then, whether devices meet the ultimate circuit/system performance requirements. For instance, synaptic weight update should exhibit linear and symmetric change of the device conductance – thus, identifying a possible range of operation conditions (and related structural features) when these characteristics are suboptimal presents an important reliability assessment task.

Discussion Topics

We will discuss topics related to degradation and variability as part of reliability assessment and their impacts to test/analysis requirements.

Toward the end, the expectation is that we will outline a basic framework for the reliability assessment of neuromorphic devices that will help both the reliability and neuromorphic communities to further refine their approaches and methodologies in NC.

Summary

A workshop “Neuromorphic Device Reliability: beyond conventional degradation” was organized in conjunction with the main program. It was discussing drifting/fluctuating of device parameters that affects changes in device characteristics detrimentally impacting NC operations. Question of practical importance: does device meet circuit/system performance requirements? It requires identifying parameters to monitor and determining test conditions relevant to circuitry operations.

Discussion was initially focused on practical aspects – what/how measurements can be done to catch performance problems. We started with variability related to changes induced by employed operations and then extended it to instability caused by spontaneous fluctuating changes occurring over time, somewhat related to retention generally considered as a continuoes shift of the memory read value. We outlined 3 types of read variability: (a) device-to-device that affects cross-bar network operations; (b) switching variability (for each individual device) when conductance value fluctuates/drifts while it’s expected to return to previously reached value – can be caused by local structural changes; (c) noise-

induced variability – read is affected by the noise magnitudes/frequency that may change with each switching event (due to different distributions of capture/emission defects).

The workshop discussion then shifted to device characteristics affected by their use conditions. It clearly indicated that generic approach to reliability assessment apparently doesn’t work well in NC where device performance requirements strongly depend on the employed algorithms and architecture. Each type of NC implementations should be evaluated considering its operation conditions. Such specificity of reliability characteristics to an NC implementation can be the cause of confusion and contradictory claims when materials, structures and operation conditions are not clearly defined.

IRPS 2019 Highlighted Papers

Study of Local BTI Variation and Its Impact on Logic Circuit and SRAM in 7 nm Fin-FET Process

Mitsuhiko Igarashi, Yuuki Uchida, Yoshio Takazawa, Makoto Yabuuchi, Yasumasa Tsukamoto and Koji Shibutani

Design Platform Technology Department 1, Renesas Electronics Corporation
5-20-1, Josuihoncho, Kodaira-shi, 187-8588, Tokyo, Japan

Automotive applications especially the ones tailored to autonomous driving require circuits with high reliability, high performance and at a low power budget demanding low voltage operation. This paper analyzes the reliability impact on circuits and Vmin on SRAMs obtained from a 7nm FinFet technology test chip based on ring oscillator reliability sensitivity analysis measurements.

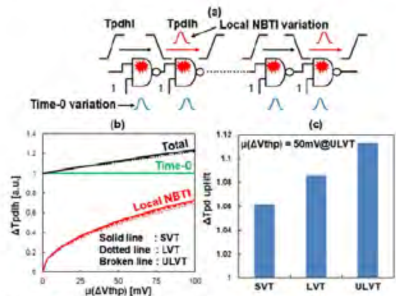


Figure 8. (b) benchmark logic circuit, (b) impact of time-0, local NBTI and total variation on logic circuit based on measurement data and simulation a (c) Consideration of Vth dependency of NBTI

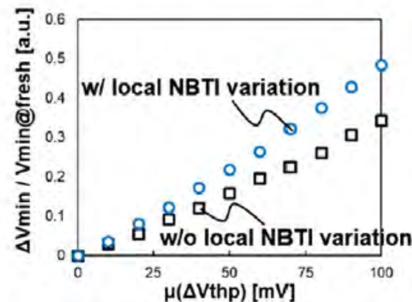


Figure 9. Analysis of local NBTI variation induced SRAM Vmin degradation

Monte Carlo Simulations to Explore the Impact of Physical Integration Schemes on Soft Errors in 3D ICs

M. L. Breeding[1], R. A. Reed[1,2], K. M. Warren[2] and M. L. Alles[1,2]

1. Department of Interdisciplinary Materials Science & Engineering, Vanderbilt University, Nashville, TN, USA
2. Department of Electrical Engineering, Vanderbilt University, Nashville, TN, USA

***Abstract*— The complex stacked structures of 2.5D/3D integrated circuits present new challenges for analyzing soft errors both experimentally and by simulation. New metals and additional interconnects are present with each added layer of circuitry in vertically integrated technologies. The proximity of these metal layers to sensitive regions may result in materials-dependent responses to radiation. Here we apply Monte-Carlo simulations to investigate the impact of geometry and material on resulting radiation transport characteristics in 3D IC structures.**

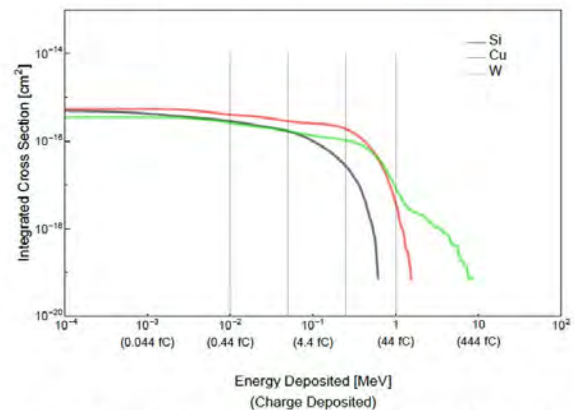


Figure 2. *Example of integrated cross section plot generated from energy deposition histograms. The vertical lines denote energy thresholds, i.e. the relative probability of depositing energy greater than or equal to the threshold amount.*

Soft Errors Session

IRPS 2019, Monterey, CA, March 31st – April 4th

Evaluation of Single Event Effects in SRAM and RRAM based Neuromorphic Computing System

Zhilu Ye[1], Rui Liu[1], Hugh Barnaby[1] and Shimeng Yu[2]

[1]School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ, 85281, USA
[2]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332, USA

Abstract—**In this work, single event effects (SEEs) are analyzed in SRAM- and RRAM-based neuromorphic computing systems. SPICE simulation is employed to model SEEs at the array level. SEEs are mapped to the weight pattern change of a multilayer perceptron (MLP), a representative artificial neural network for MNIST handwritten digit recognition. Simulations show the RRAM-based MLP has much less susceptibility to SEEs compared to the SRAM architecture. Improvements to SRAM-based MLP single event reliability may be achieved by lowering bit-width and enlarging network size.**

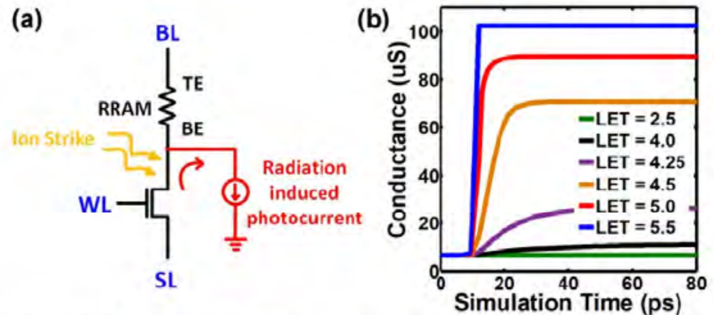


Fig. 3. (a) Schematic of 1T1R structure. (b) Simulated analog RRAM's conductance transients under heavy ion strike with different LET values. The unit of LET is MeV*cm^2/mg.

Soft Errors Session

IRPS 2019, Monterey, CA, March 31st – April 4th

On the influence of gate length on pBTI in GaN-on-Si E-mode MOSc-HEMT

A.G. Viey (1,2,4), W. Vandendaele(1), M.A. Jaud(1), R. Gwoziecki (1), A. Torres(1), M. Plissonnier(1), F. Gaillard(1), G. Ghibaudo(2), R. Modica(3), F. Iucolano(3), M. Meneghini(4), G. Meneghesso(4)

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(2) IMEP-LAHC MINATEC, 3, Parvis Louis Néel - CS 50257 - 38016 Grenoble France
(3) STMicroelectronics, Stradale Primosole 50, 95121 Catania, Italy
(4) University of Padova, Department of Information Engineering,Via Gradenigo 6/B, 35131, Padova, Italy

GaN-on-Si HEMT technology is undoubtedly considered as the major candidate for multi-MHz moderated power (<2kW) applications [1,2]. Current collapse issues being now mainly solved [3, 4], Vth instabilities are now a major concern to increase lifetime of the transistors. Recent n/pBTI on E-mode pGaN gate HEMTs [5,6] as well as on the MIS gate configuration [7] start to show Vth instabilities which would severely affect the dynamic performance of the transistors over the time. Advanced E-mode MOSc-HEMT (MOS-channel HEMT) configuration is also envisaged as an E-mode solution and has been recently studied under AC and DC pBTI conditions [8]. In this paper we explore the influence of the fully recessed gate length on Vth instabilities with ultra-fast pBTI measurements (< 10µs) on GaN-on-Si E-mode MOSc-HEMTs.

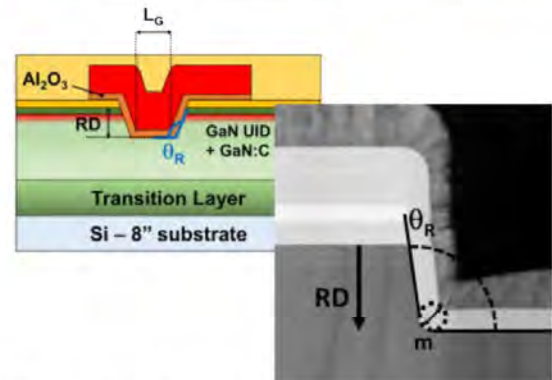

Figure 1. Schematic of the GaN-on-Si E-mode MOSc-HEMT and TEM cross section illustrating the recess depth (RD), etching angle (θ_R) and curvature radius (m) of the gate corner.

Wide Bandgap Session

IRPS 2019, Monterey, CA, March 31st – April 4th

A fast and test-proven methodology of assessing RTN/fluctuation on deeply scaled nano pMOSFETs

R. Gao[1,2*] (r.gao_90@outlook.com), Z. Ji[2], J.F. Zhang[2], Z.Y. He[1], Y.Q. Chen[1], Y, Huang[1], Y.F. En[1]
[1]Science and Technology on Reliability Physics and Application of Electronic Component Laboratory No.5 Electronics Research Institute of the Ministry of Industry and Information Technology Guangzhou, 510610, Guangdong, P. R. China
[2]School of Engineering, Liverpool John Moores University, Byrom Street, Liverpool, L3 3AF, UK

Abstract— **Random Telegraph Noise (RTN)/fluctuation becomes one of the most serious reliability issues in nowadays deeply scaled CMOS. The current RTN characterization methods need to select devices and can only capture the fast traps, thus is very difficult predict and validate device long-term fluctuation behavior. A new fast and test-proven methodology of assessing RTN/fluctuation is proposed in this work. By using the Within Device Fluctuation (WDF), all the devices' fluctuation can be captured. Moreover, WDF can be well explained and simulated as a sum of all the As-grown Traps (AT) induced RTN.**

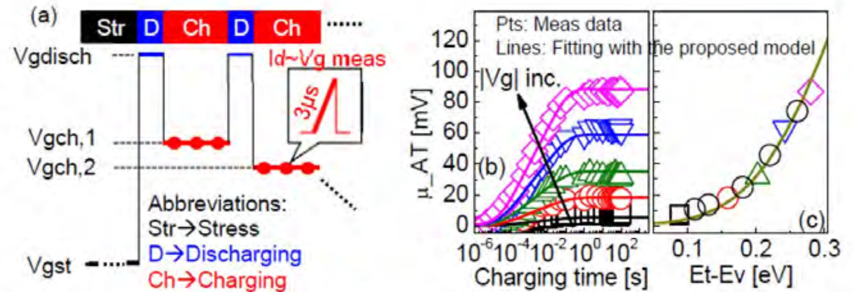

Fig.7 (a) The test procedure. The device is firstly heavily stressed and discharged to ensure the negligible generation in the following charging process. **(b)** The charging kinetics averaged from multiple-device measurements under different overdrive voltages, Vgov. **(c)** The measured energy profile of AT (pts) and the fitted curve with Gaussian distribution.

Reliability Testing Session

IRPS 2019, Monterey, CA, March 31st – April 4th

Accelerated Capture and Emission (ACE) Measurement Pattern for Efficient BTI Characterization and Modeling

Zhicheng Wu[1*], J. Franco, D. Claes, G. Rzepa[2], P. Roussel, N. Collaert, G. Groeseneken[1], D. Linten, T. Grasser[2], B. Kaczer
imec, Leuven, Belgium; [1]also at KU Leuven, ESAT-MICAS; [2]T.U. Vienna; *Email: Zhicheng.Wu@imec.be

Abstract— A new gate pattern is proposed to minimize test time while maximizing charge capture and emission into/from oxide defects for efficient and accurate BTI modeling. In conjunction with the imec/T.U. Vienna BTI simulation framework "Comphy", which encapsulates the microscopic behavior of individual defects, the Accelerated Capture and Emission (ACE) gate pattern streamlines a bottom-up approach for BTI evaluation from device to circuit level. The new pattern is systematically compared with the well-established Constant-Voltage-Stress (CVS) and Ramped-Voltage-Stress (RVS) methods and is found to show substantial improvements regarding both characterization and model-calibration efficiencies. We further validate our flow by showing excellent agreement between the direct projections of the model calibrated with the new pattern and experimental results of AC stress tests with various duty factors.

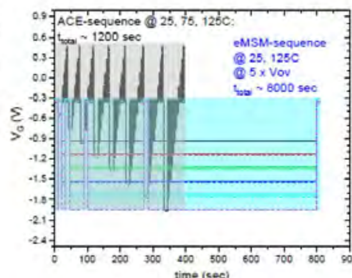

Fig. 8: A commonly used NBTI eMSM test compared to ACE sequence. Note the different test duration and voltage

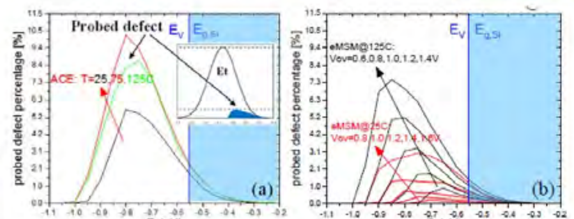

Fig. 9: Fraction of HK defects probed by the **(a)** ACE and **(b)** eMSM, as a function of defect energy level (E_t). ACE shows improved characterization efficiency compared to eMSM. Note: these values are proportional to the max V_{ov}, which is limited to avoid triggering other degradation mechanisms (e.g. the reduced peak at *125C* w.r.t *75C* in (a) is related to a truncated max V_{ov}, same in **Fig. 10a**). The inset sketches the probed defect w.r.t. the entire modeled defect bands.

Transistor Session

IRPS 2019, Monterey, CA, March 31st – April 4th

A NEW APPROACH TO VALIDATE GaN FET RELIABILITY TO POWER-LINE SURGES UNDER USE CONDITIONS

Sandeep R. Bahl and Paul Brohlin
High Voltage Power, Texas Instruments Incorporated, 2900 Semiconductor Dr., Santa Clara, CA 95052 and
12500 TI Blvd, Dallas TX 75243, USA

IRPS
International Reliability Physics Symposium

***Abstract*— The robustness of FETs to power-line surges has a tremendous impact on field reliability and is an important consideration for the adoption of new technologies like GaN. The methodology for silicon FETs, however, causes concern for GaN because of the low avalanching ability of present-day GaN FETs. GaN FETs, however, are designed with better overvoltage capability than Si FETs, making this property important. This paper defines, for the first time, a methodology for the surge rating of GaN FETs using their superior transient overvoltage capability. It leads to a device-level surge parametric specification. This is an important consideration for the design of surge-robust power supplies using GaN. It is also shown, for the first time, that GaN FETs are robust to power line surges.**

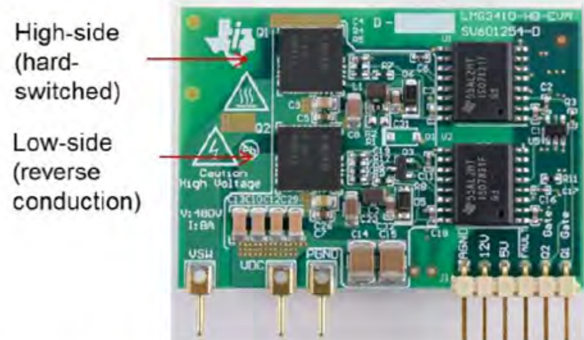

Figure 4. *TI-GaN EVM half-bridge card used for the device test. It plugs into a buck converter motherboard. The use of a half-bridge allows surge testing for both polarities: hard-switching turn-on and reverse conduction.*

Wide Bandgap Session

IRPS 2019, Monterey, CA, March 31st – April 4th