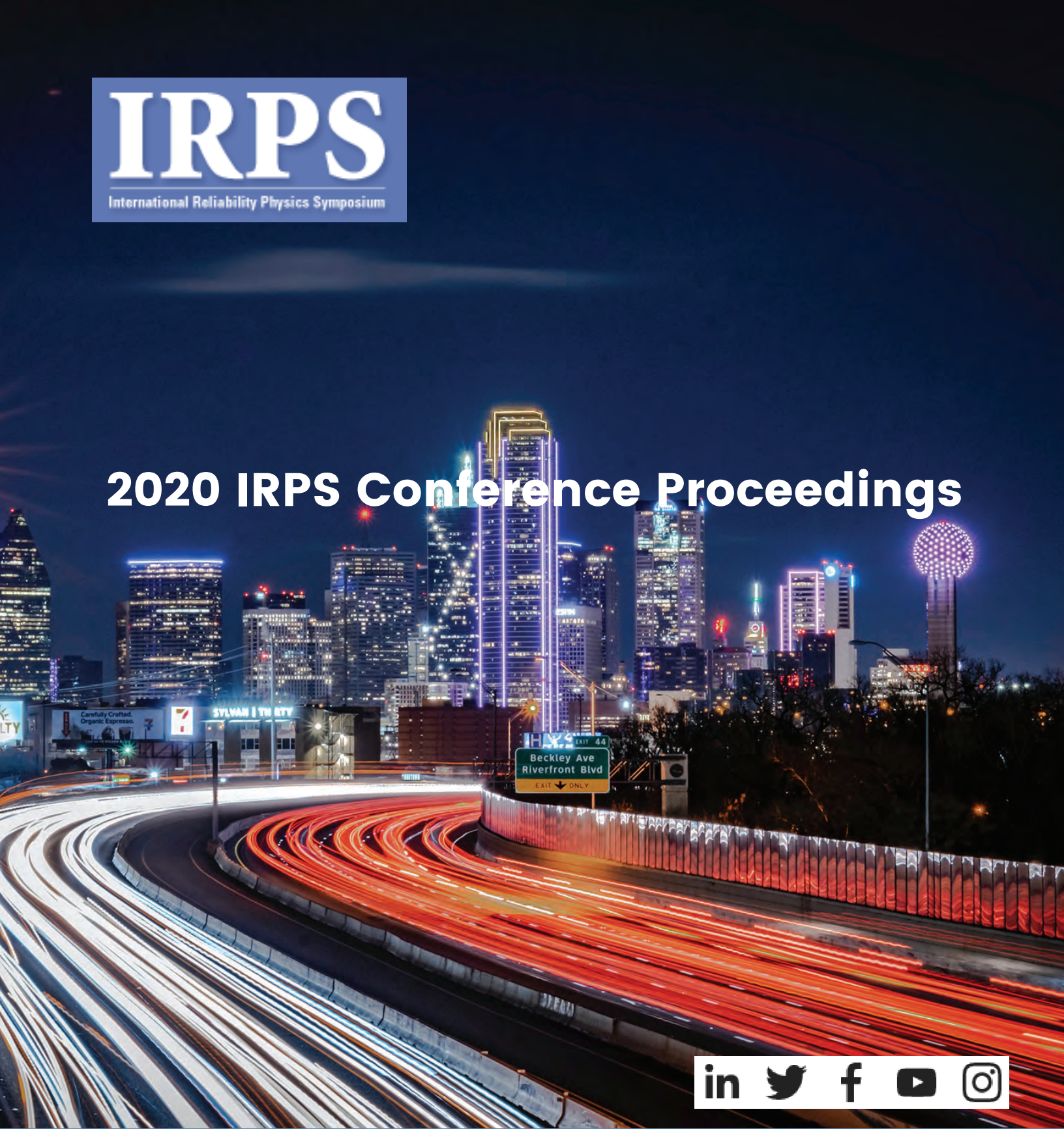




2020 IRPS Conference Proceedings



For More Information
IEDM Online: irps.org

Table of Contents

Intro	3
Committees	3
Topics of Interest	5
Program:	
Keynote Speakers	6
Invited Speakers.....	7
Tutorials	7
Workshops	9
Year in Review.....	9
Exhibits & Exhibit Events	9
Patrons	10
 Abstracts, Bios for Tutorials, Short Courses & Technical Program.....	Appendix

Intro

For 59 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world.



IRPS is Co-Sponsored by IEEE EDS and Reliability Society

Digital & Social Media

- Facebook: @IEEE-IRPS-239965161886
- Twitter: @IEEEIRPS
- LinkedIn: <https://www.linkedin.com/groups/2624656/profile>
- YouTube: @IEEEIRPS
- Instagram: @iee_irps
- Weibo: <http://weibo.com/u/5500677074>

Committees

Executive Committee

General Chair

Gaudenzio Menghesso
University of Padova
gauss@dei.unipd.it

Vice General Chair

Robert Kaplar
Sandia National Labs
rjkapla@sandia.gov

Technical Program Chair

Charles Slayman
Cisco Systems
cslayman@cisco.com

Vice Technical Program Chair

Vincent Huard
Dolphin Integration
vincent.huard@dolphin.fr

Finance Chair

Chris Connor
Intel
chris.connor@intel.com

Arrangements Chair

Jason Ryan
NIST
jason.ryan@nist.gov

AV/Presentations Chair

Cathy Christiansen
GlobalFoundries
cathy.christiansen@globalfoundries.com

Communications Chair

Yen-Hao Shih
Macronix
yhshih@mxic.com.tw

Publications Chair

Koji Eriguchi
Kyoto University
eriguchi.koji.83@kyoto-u.ac.jp

Publicity Chair

Barry Linder
IBM
bplinder@us.ibm.com

Registration Chair

Ben Kaczer
IMEC
kaczer@imec.be

Tutorials Chair

Susumu Shuto
Toshiba
susumu.shuto@toshiba.co.jp

Workshops Chair

Christine Hau-Riege
Qualcomm
chaurieg@qti.qualcomm.com

Exhibits Chair

Tibor Grasser
TU Wien
grasser@iue.tuwien.ac.at

Secretary

Marta Bagatin
University of Padova
marta.bagatin@dei.unipd.it

Conference Manager

Lisa Boyd
IEEE MCE
IRPSplanners@ieee.org

Program Specialist

Tracy Holle
IEEE MCE
IRPSplanners@ieee.org

3D/2.5D/Packaging

Topic Chair Rohit Grover, Intel
Vice Chair CS (Prem) Premachandran, GlobalFoundries
Past Chair Sudarshan Rangaraj, Amazon Lab 126
Ravi Aggarwal, Intel
In-hak Baick, Samsung
Preeti Chauhan, Google
Emmanuel Chery, IMEC
YC Chuang, TSMC
Enamul Kabir, Intel
Kangwook Lee, SK Hynix
John Osenbach, Infinera
Ashok Pachamuthu, Maxim
Richard Rao, InPhi
Kanika Sethi, Intel
Guotao Wang, Futurewei
Gang Yuan, Microsoft

Neuromorphic Computing Reliability

Topic Chair Matthew Marinella, Sandia National Laboratories
Vice Chair Kin Leong Pey, Singapore Univ. of Tech and Design
Past Chair Gennadi Bersuker, The Aerospace Corporation
Stefano Ambrogio, IBM Almaden Research Center
An Chen, SRC
Robin Degraeve, IMEC
Arthur Edwards, Air Force Research Laboratory (AFRL)
Hiroyuki Akinaga, Advanced Industrial Science and Technology (AIST), Japan
Tuo-Hung (Alex) Hou, National Chiao Tung University, Taiwan
Doo Seok Jeong, HANYANG University (Korea)
Roza Kotlyar, Intel Corporation
Gabriel Molas, LETI (France)
Sabina Spiga, CNR-IMM, Italy
John Paul Strachan, Hewlett Packard Enterprise
Eric M. Vogel, Georgia Institute of Technology
Rainer Waser, RWTH Aachen
Bin Gao, Tsinghua University

Circuit Reliability/Aging

Topic Chair James Tschanz, Intel
Vice Chair Florian Cacho, STMicroelectronics
Past Chair Georgios Konstadinidis, Google

Xinfei Guo, Mellanox
Karl Hofmann, Infineon
Kazutoshi Kobayashi, Kyoto Institute of Technology
Tom Kopley, ONSemiconductors
Chris Kim, University of Minnesota
Vijay Reddy, Texas Instruments
Mingoo Seok, Columbia University
Hyewon Shim, Samsung
Sriram Kalpat, Qualcomm
Saibal Mukhopadhyay, Georgia Institute of Technology

IRPS/IEEW ESD and Latchup

Topic Chair Shih-Hung Chen, IMEC
Vice Chair Mototsugu Okushima, Renesas
Past Chair Gianluca Boselli, Texas Instruments
Lorenzo Cerati, ST Microelectronics
Zhong Chen, University of Arkansas
Kai Esmark, Infineon
Nathan Jack, Intel
Junjun Li, ESDA
Dionyz Pogany, TU Wien
Mayank Shrivastava, Indian Institute of Science
Michael Stockinger, NXP
Teruo Suzuki, Socionext Inc.
Michael Khazhinsky, Silicon Labs
Nathaniel Peachey, Qorvo

Failure Analysis

Topic Chair Jane Li, NVidia
Vice Chair Bryan Tracy, EAG Laboratories
Past Chair Baohua Niu, TSMC
Kevin Johnson, Intel
Jayhoon Chung, Texas Instruments
Stephen Fasolino, Raytheon
Branden Foran, The Aerospace Corp.
Eckhard Langer, GlobalFoundries
Paiboon Tangyonyong, Sandia National Laboratories
Nathan DeBardleben, Los Alamos National Laboratory
Jason Wheeler, Raytheon
Michael Gribelyuk, Western Digital

Gate/MOL Dielectrics

Topic Chair Mario Lanza, Soochow University
Vice Chair Francesco Maria, Puglisi University of Modena and Reggio Emilia
Past Chair Nagarajan Raghavan, Singapore U. of Technology and Design

Ravi Achanta, GlobalFoundries
Shih-Chang Chen, TSMC
Fei Hui, Technion
Miaomiao Wang, IBM
Regina Dittman, Forschungszentrum Jülich GmbH
Andrea Padovani, Applied Materials
Mireia Bargallo-Gonzalez, Institute of Microelectronics of Barcelona, CNM-CSIC
Miguel Muñoz-Rojo, University of Twente
Naohito Suzumura, Renesas
Stanislav Tyaginov, IMEC
Eilam Yalon, Technion
Yuanyuan Shi, IMEC

IC Product Reliability

Topic Chair Jae-Gyung Ahn, Xilinx
Vice Chair Souhir Mhira, Mentor Graphics
Past Chair Feng Xia, Intel
Davide Appello, ST
Paolo Bernardi, Politecnico di Torino
Sandhya Chandrashekhar, Cypress
Steven Mittl IBM
Ming-Han Hsieh, Mediatek
Lin Cong, Nvidia
Richard (Shiguo) Rao, Inphi
Daniel Tille, Infineon

Memory

Topic Chair Ming-Yi Lee, Macronix
Vice Chair (MRAM) Tetsuo Endoh, Tohoku University
Vice Chair (ReRAM) Shimeng Yu, Georgia Institute of Technology
Past Chair Andrea Chimenton, Intel
Guohan Hu, IBM
Carlo Cagli, CEA
Joe McCrate, Micron
Jiezhi Chen, Shandong University
SangBum Kim, Seoul National Univ.
Georg Tempel, Infineon
Yuri Tkachev, Microchip
Cristian Zambelli, University of Ferrara
Wen-Hsien Kuo, TSMC
Barry O'Sullivan, imec

Metallization/BEOL Reliability

Topic Chair Baozhen Li, IBM
Vice Chair Rahim Kasim, Intel
Past Chair Valeriy Sukharev, Mentor Graphics
Seungman Choi, GlobalFoundries
Matsuyama Hideya, Socionext

Andrew Kim, Intel
Ki-Don Lee, Samsung
Ming-Hsien Lin, TSMC
Gavin Hall, On-Semi
Kristof Croes, IMEC
Young-Joon Park, TI
Tian Shen, IBM
Cher Ming Tan Chang Gung, Univ
Shinji Yokogawa Univ. E. C.

Process Integration

Topic Chair Mustapha Rafik, ST
Microelectronics
Vice Chair Anisur Rahman, Intel
Past Chair Hiroshi Miki, Hitachi
Adrian Chasin, IMEC
Jen-Hao Lee, TSMC
Xavier Garros, CEA-LETI
Hyun Chul Sagong, Samsung
Guido Sasse, NXP
Motoyuki Sato, Micron
Richard Southwick, IBM
Srinivasan Purushothaman,
GlobalFoundries

Reliability Testing

Topic Chair Jifa Hao, On Semiconductor
Vice Chair Osama O. Awadelkarim,
Penn State Univ.
Past Chair Derek Slotke, Intel
Hosain Farr, Qualitau
Praveen Gunturi, II-VI Inc
Peter Paliwoda, GlobalFoundries
Stéphane Moreau, CEA-Leti
John Ortega, Intel
Fiorella Pozzobon, STMicroelectronics
Bryan Root, Celadon Systems
Dirk Rudolph, GlobalFoundries
Stephen Ramey, Intel
Pascal Salome, SERMA Group
Tim Turner, Xact/Texas Semicon Labs
Durgamadhab Misra, New Jersey
Institute of Technology
Yi Zhao, Zhejiang University
Kevin Manning, Analog Devices
Samia Suliman, Penn State University

Soft Error

Topic Chair Indranil Chatterjee, Airbus
Vice Chair Daisuke Kobayashi, ISAS JAXA
Past Chair Nihaar Mahatme, NXP
Semiconductors
Laurent Artola, Onera
Ethan Cannon, Boeing
Krishna Mohan Chavali, GlobalFoundries
Yi-Pin Fang, TSMC
Yanran Chen, Xilinx

Simone Gerardin, U. Padova
Ruben Garcia Alia, CERN
Nelson Gaspard, NASA
Haibin Wang, Hohai University
Masanori Hashimoto, Osaka Univ.

System Reliability

Topic Chair Jay Sarkar, Western Digital
Vice Chair Flavio Griggio, Microsoft
Past Chair Rob Kwasnick, Intel
Michael Azarian U. Maryland
Sandhya Chandrashekar, Cypress
Jinseok Kim, Samsung
Nikolaos Papandreou, IBM Research
Zurich
Yan Liu, Medtronic
Guneet Sethi, Amazon Lab 126
Amit Marathe, Google
Florian Moliere, Airbus
Yi-Ching Ong, TSMC
David Sunderland, Boeing (Retired)

Transistors

Topic Chair Jacopo Franco, IMEC
Vice Chair Chetan Prasad, Intel
Past Chair Tibor Grasser, TUWien
Goel Nilesh, BITS Pilani Dubai Campus
Kazuki Nomoto, Sony Semiconductor
Solutions
Jason Campbell, NIST
Subhadeep Mukhopadhyay, TSMC
Moonju Cho, Micron
Changze (Chris) Liu, Huawei
Montserrat Nafria, Universitat
Autonoma de Barcelona
Eun-Ae (Grace) Chung, Samsung
Hokyung Park, SK Hynix
Wen Liu, Globalfoundries
Runsheng Wang, Peking University
Bonnie Weir, Broadcom
Alain Bravaix, IM2NP (ST Micro)

Wide Bandgap

Topic Chair Aivars Lelis, US Army
Research Labs
(SiC) Vice Chair Thomas Aichinger,
Infineon
(GaN) Vice Chair Sameh Khalil,
Infineon
Past Chair Sandeep Bahl, TI
Past Chair Matteo Meneghini, U. Padova
Anant Agarwal, Ohio State Univ
Alberto Castellazzi Kyoto, University of
Advanced Science
Charles Cheung, NIST
Ferdinando Iucolano, ST
Mike Uren, U. Bristol

Dan Lichtenwalner, Cree-Wolfspeed
Peter Losee, United SiC
David Sheridan, AOS
Hiroshi Yano, Univ. of Tsukuba
Shuzhen You, IMEC
Hideyuki Okita, Panasonic
Alain Charles, Infineon
Kiran Chatty, Littlefuse
Srabanti Chowdhury, Stanford Univ.
Ulrike Grossner, ETH Zurich
Joshi Kaustubh, TSMC
Josef Lutz, University of Chemnitz
Luca Perniola, CEA, Leti
Junji Senzaki, AIST
Bob Stahlbush, Naval Research
Laboratory
Akin Akturk, CoolCAD Electronics
Shireen Warnock, MIT Lincoln Labs

RF/mmW/5G Reliability

Topic Chair Farid Medjdoub, I.E.M.N
- CNRS
Vice Chair Jose Jimenez, Qorvo
Robert Coffie, RLC solutions
Michael Dammann, Fraunhofer IAF
Krishnanshu Dandu, TI
Fernando Guarin, GlobalFoundries
Sriram kalpat, Qualcomm
Dietmar Kissinger, University of Ulm
Nathalie Malbert, Univ. of Bordeaux
Vijay Reddy, TI
Zuo-Min Tsai, National Chung Cheng
University

Beyond CMOS

Topic Chair Charlie Slayman, Cisco
Systems
Fei Hui, Technion Institute of
Technology, Israel
Jacopo Franco, imec
Mario Lanza, Soochow University
Max Lemme, Aachen University
Nagarajan Raghavan, Singapore
University of Technology and Design
Yury Illarionov, TU Wien

Topics of Interest

SPECIAL FOCUS TOPICS

Circuit Reliability and Aging – RAS, self-healing, aging aware designs, design tools

Emerging memory / Neuromorphic Computing– Reliability for PCM, MRAM, RRAM, ferroelectrics

Reliability of RF/mmW/5G Devices – CMOS, SiGe BiCMOS, SOI, GaAs, GaN

Circuits, Products, and Systems

- Circuit Reliability and Aging
- IC Product Reliability
- System Electronics Reliability
- Soft Errors
- ESD and Latchup
- Packaging and 2.5D/3D Assembly
- Reliability Testing
- Silicon Photonics
- RF/mmW/5G

Materials, Processing, and Devices

- Transistors
- Gate/MOL Dielectrics
- Beyond CMOS Devices
- Neuromorphic Computing Reliability
- Wide-Bandgap Semiconductors
- Compound and Optoelectronic Devices
- Metallization/BEOL Reliability
- Process Integration
- Failure Analysis
- Memory Reliability
- Photovoltaics
- MEMS

Program

NOTE – For full Program, including Abstracts and Speaker information, view Appendix

VIDEOS – <https://www.youtube.com/user/IEEEIRPS/videos>

Keynote Speakers

Plenary Keynote-I

Title: The Future of Compute: Reliability and Resiliency in the era of Data Transformation

Dr. Mike Mayberry - Intel

Plenary Keynote-II

Title: Power Semiconductor Reliability – An Industry Perspective on Status and Challenges

Dr. Oliver Häberlen - Infineon Technologies Austria AG

Plenary Keynote-III

Title: Power scalability challenges in High-Voltage ESD Design

Dr. Gianluca Boselli - Texas Instruments

Invited Speakers

Wide-Bandgap Semiconductors – SiC

- 3B.1 Ruggedness of SiC devices under extreme conditions - Peter Friedrichs - Infineon
- 5B.1 Defect spectroscopy in SiC devices - Michael Waltl - TU Vienna
- 5B.2 Challenges and peculiarities in developing new standards for SiC - Don Gajewski - Cree/Wolfspeed

Neuromorphic Computing Reliability

- 3C.1 Introduction of Non-Volatile Computing In Memory (nvCIM) by 3D NAND Flash for Inference Accelerator of Deep Neural Network (DNN) and the Read Disturb Reliability Evaluation - Hang-Ting Lue - Macronix
- 8B.1 Embracing the Unreliability of Memory Devices for Neuromorphic Computing - Damien Querlioz - U. Paris-Sud
- 8B.5 Neuromorphic computing with Phase Change, Device Reliability and Variability Challenges - Charles Mackin - IBM, Almaden

Circuit Reliability and Aging

- 2A.1 An industry-standard approach toward modeling device aging - Colin ShawRosana - Si2 / Silvaco
- 3A.1 A novel approach to in-field, in-mission reliability monitoring based on deep data - Evelyn Landman - CTO, ProteanTecs
- 3A.2 Voltage Regulator Reliability - Saibal Mukhopadhyay - Georgia Tech
- 3A.3 Experimental monitoring of aging in CMOS RF linear power amplifiers: correlation between device and circuit degradation - Rodriguez Martinez - Universitat Autònoma de Barcelona

RF/mmW/5G Reliability

- 2B.1 Reliability physics of GaN HEMT microwave devices: the age of scaling - Enrico Zanoni - Univ of Padova
- 2B.3 Silicon Based RF Reliability Challenges for 5G Communication - Paul Colestock - GlobalFoundries
- 4B.3 The role of RF operational life testing in evaluating III-V devices addressing RF through millimeter-wave applications - Elias Reese - Qorvo

Transistors I

- 5A.1 FEOL Reliability Issues in Advanced CMOS Nodes - Inanc Meric - Intel

System Electronics Reliability

- 4C.1 Challenges in Prognostics and Health Management of Electronic Systems - Michael Azarian - Univ Maryland/CALCE

Failure Analysis

- 7C.4 Localization of high speed failures with a novel detection method - Ed Cole - Sandia

Tutorials

Basics of Semiconductor Reliability I

TSA.4 (Tutorial) – Basic Reliability Physics: Acceleration Models, Statistical Methods, and Defect

Screening

Mark Porter – Medtronic

TSB.1 (Tutorial) – Bias Temperature Instabilities: Best Practices for Reliability Benchmarking and Optimization Based on Recent Theoretical Insights

Jacopo Franco - IMEC

TSB.2 (Tutorial) – Self-heating: Assessment Methodologies, Impact on Reliability and Prospects for Future Technology Solutions

Erik Bury – IMEC

Basics of Semiconductor Reliability II

TSA.1 (Tutorial) – Terrestrial Radiation and Its Impact on the Reliability Performance of Microelectronics

Robert Baumann - Radiosity Solutions LLC & Southern Methodist University

TSA.2 (Tutorial) – Plasma-induced Damage-modeling, Characterizations, and Design Methodologies

Koji Eriguchi - Kyoto University

TSB.3 (Tutorial) – Electromigration: Physics, Rule, Validation, and Relaxation

Young-Joon Park - Texas Instruments | Sunglyong Kim - Texas Instruments

TMC.3 (Tutorial) – Materials Analysis Techniques in Semiconductor

Ling Pan – Intel

Memory Reliability / Power Devices Reliability

TSA.3 (Tutorial) – SONOS or Charge Trap Memories

Krishnaswamy Ramkumar - Cypress Semiconductor

TMB.1 (Tutorial) – Scaling Impacts on Reliability of p-STT MRAM Cells

Toshio Sunaga - ExIBM

TMB.2 (Tutorial) – Phase Change Memory: Technology Reliability and System-Level Implications

Haralampos Pozidis - IBM Research - Zurich

Nikolaos Papandreou – IBM

TMA.1 (Tutorial) – The Role of Defects on Reliability Aspects in GaN Power Devices

Clemens Ostermaier - Infineon

TMA.3 (Tutorial) – Testing for Wear and Abnormal Conditions of Power IGBT Modules

Francesco Iannuzzo - Aalborg University

Circuit & System Reliability

TSB.4 (Tutorial) – An Introduction to RF and Mixed-Signal Circuit Reliability

Vijay Reddy - Texas Instruments

TMB.3 (Tutorial) – Designing for Analog Reliability: From Components to Circuits

Dhanoop Varghese - Texas Instruments

Sunglyong Kim - Texas Instruments, Inc.

TMD.2 (Tutorial) – TCAD-EDA Assisted BTI-HCD Reliability Framework from Devices to Circuits

Souvik Mahapatra - Indian Institute of Technology Bombay

Workshops

- BEOL Reliability | Ki-Don Lee (Samsung) | Gavin Hall (ON Semiconductor)
- Circuit Reliability and Aging: Measurements and Simulations | Dr. Valeriy Sukharev (Mentor Graphics) | Dr. Georgios Konstadinidis (Google)
- Emerging Memory | Joe McCrate (Micron) and Prof. Tetsuo Endoh (Tohoku University)
- Wide-bandgap Workshop (GaN) | Dr. Shireen Warnock, MIT Lincoln Laboratory | Prof. Matteo Meneghini, University of Padova
- Wide-bandgap Workshop (SiC) | Dr. Aivars Lelis, US Army Research Lab | Dr. Thomas Aichinger, Infineon
- Solid State Drive Workshop | Dr. Jay Sarkar, Western Digital | Dr. Nikolaos Papandreou, IBM Research
- RF/mmW/5G | Fernando Guarin (GlobalFoundries), Si-SiGe | Farid Medjdoub (IEMN CNRS), GaN
- Workshop on BTI and HCD | Xavier Federspiel, ST Microelectronics | Souvik Mahapatra, IIT Bombay

Year In Review

YA1 – Circuit Reliability: Main Review

James Tschanz - Intel Corporation

YA2 – Circuit Reliability: EDA Aspects

Georgios Konstadinidis – Google

YA3 – RF/mmW/5G Reliability: CMOS/SiGe

Fernando Guarin - GLOBALFOUNDRIES

YA4 – RF/mmW/5G Reliability: GaN HEMT

Enrico Zanoni - University of Padova

YA5 – Memory

Chandra Mouli - Micron

Technical Program

NOTE – For full Program, including Abstracts and Speaker information, view Appendix

Exhibits & Exhibit Events

Exhibits are an integral part of the International Reliability Physics Symposium. Don't miss this opportunity to showcase your company's products and services in our VIRTUAL exposition.

For more than 59 years, the International Reliability Physics Symposium (IRPS) has been the premier conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and other parts of the world, IRPS seeks to understand the interplay between the reliability of semiconductor components, integrated circuits, and microelectronic assemblies through an improved understanding of both the physics of failure as well as the application environment.

IRPS Highlights:

- 400+ professionals from the semiconductor reliability field
- 90+ platform presentations and invited talks
- 50+ posters at the evening reception
- 20+ tutorials
- 10+ workshops and panel discussions

For more information or for custom opportunities, contact Lisa Boyd – l.boyd@ieee.org

IRPS gratefully acknowledges the generous support
of our 2020 exhibitors:

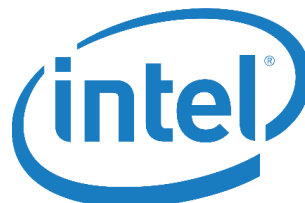


2020 Patrons

Platinum



Gold



Appendix – Abstracts, Bios & Technical Program

2020 IEEE International Reliability Physics Symposium (IRPS)



**Virtual Conference
28 April – 30 May 2020**





Sunday, 29 March

7:30am **Breakfast**
International Foyer

8:30am **TSA1 - Terrestrial Radiation and Its Impact on the Reliability Performance of Microelectronics**
International I & II

TSA.1 (Tutorial) - Terrestrial Radiation and Its Impact on the Reliability Performance of Microelectronics
» [Robert Baumann](#)¹ (1. Radiosity Solutions LLC & Southern Methodist University)

8:30am **Bias Temperature Instabilities: Best Practices for Reliability Benchmarking and Optimization Based on Recent Theoretical Insights**
International III & IV

TSB.1 (Tutorial) - Bias Temperature Instabilities: Best Practices for Reliability Benchmarking and Optimization Based on Recent Theoretical Insights
» [Jacopo Franco](#)¹ (1. IMEC)

10am **Break**
International Foyer

10:30am **Plasma-induced Damage-modeling, Characterizations, and Design Methodologies**
International I & II

TSA.2 (Tutorial) - Plasma-induced Damage-modeling, Characterizations, and Design Methodologies
» [Koji Eriguchi](#)¹ (1. Kyoto University)

10:30am **Self-heating: Assessment Methodologies, Impact on Reliability and Prospects for Future Technology Solutions**
International III & IV

TSB.2 (Tutorial) - Self-heating: Assessment Methodologies, Impact on Reliability and Prospects for Future Technology Solutions
» [Erik Bury](#)¹ (1. IMEC)

12pm **Lunch**
International Foyer

1:30pm **SONOS or Charge Trap Memories**
International I & II

TSA.3 (Tutorial) - SONOS or Charge Trap Memories
» [Krishnaswamy Ramkumar](#)¹ (1. Cypress Semiconductor)

1:30pm **Electromigration: Physics, Rule, Validation, and Relaxation**
International III & IV

TSB.3 (Tutorial) - Electromigration: Physics, Rule, Validation, and Relaxation
» [Young-joon Park](#)¹ (1. Texas Instruments)

1:30pm **Electronic Design Automation (EDA) Solutions for Latch-up Verification in CMOS and HV Technologies**
Spicewood I, II & III

TSC.3 (Tutorial) - Electronic Design Automation (EDA) Solutions for Latch-up Verification in CMOS and HV Technologies
» [Michael Khazhinsky](#)¹ (1. Silicon Labs)

3pm **Break**
International Foyer



Continued from Sunday, 29 March	
3:30pm	Basic Reliability Physics: Acceleration Models, Statistical Methods, and Defect Screening <i>International I & II</i>
	TSA.4 (Tutorial) - Basic Reliability Physics: Acceleration Models, Statistical Methods, and Defect Screening » Mark Porter ¹ (1. Medtronic)
3:30pm	Introduction to RF and Mixed-Signal Circuit Reliability <i>International III & IV</i>
	TSB.4 (Tutorial) - Introduction to Circuit Reliability » Vijay Reddy ¹ (1. Texas Instruments)
3:30pm	EOS, ESD, Transient, AMR, EIPD, Robustness, Aging - Do All of These Pieces go to the Same Puzzle? <i>Spicewood I, II & III</i>
	TSC.4 (Tutorial) - EOS, ESD, Transient, AMR, EIPD, Robustness, Aging —Do all of These Pieces go to the Same Puzzle? » Hans Kunz ¹ (1. Texas Instruments, Inc.)

Monday, 30 March	
7am	Breakfast <i>International Foyer</i>
8am	The Role of Defects on Reliability Aspects in GaN Power Devices <i>Val Verde</i>
	TMA.1 (Tutorial) - The Role of Defects on Reliability Aspects in GaN Power Devices » Clemens Ostermaier ¹ (1. Infineon)

8am	Scaling Impacts on Reliability of p-STT MRAM Cells <i>International I & II</i>
	TMB.1 (Tutorial) - Scaling Impacts on Reliability of p-STT MRAM Cells » Toshio Sunaga ¹ (1. TBD)
8am	Exploring Relation of ESD and EMC: Tests, Events to Damage, Failure Types, and Co-Design Approaches <i>Spicewood I, II & III</i>
	TME.1 (Tutorial) - Exploring Relation of ESD and EMC: Tests, Events to Damage, Failure Types, and Co-Design Approaches » Alan Righter ¹ (1. Analog Devices)
8am	Reliability-aware Energy-efficient Smart-IoT & Cognitive-5G <i>International III & IV</i>
	TMC.1 (Tutorial) - Reliability-aware Energy-efficient Smart-IoT & Cognitive-5G » Sidina Wane ¹ , Vincent Huard ² (1. EV Technology, 2. Dolphin)
8am	Topics: Automotive Title: TBD <i>Cap Rock I, II & III</i>
	TMD.1 (Tutorial) - Automotive Semiconductor Reliability and its Changed Importance for Complex System Engineering - From Changing Mission Profiles to Reliability / Security Co-design » Andreas Aal ¹ , Oliver Aube ² (1. Volkswagen, 2. GLOBALFOUNDRIES)
9:30am	Break <i>International Foyer</i>
10am	System-Focused Reliability of SiC MOSFETs <i>Val Verde</i>



Continued from Monday, 30 March	
	<p>TMA.2 (Tutorial) - System-Focused Reliability of SiC MOSFETs » Mrinal Das¹ (1. Texas Instruments)</p>
10am	<p>Phase Change Memory: Technology Reliability and System-Level Implications <i>International I & II</i></p>
	<p>TMB.2 (Tutorial) - Phase Change Memory: Technology Reliability and System-Level Implications » Haralampos Pozidis¹, Nikolaos Papandreou² (1. IBM Research - Zurich, 2. IBM)</p>
10am	<p>Tests, Events to Damage, Failure Types, and Co-Design Approaches <i>Spicewood I, II & III</i></p>
	<p>TME.2 (Tutorial) - Full chip CDM ESD Verification » Melanie Etherton¹ (1. NXP)</p>
10am	<p>Challenges in Prognostics and Health Management of Electronic Systems <i>International III & IV</i></p>
	<p>TMC.2 (Tutorial) - Prognostics and Health Management of Systems » Michael Azarian¹ (1. University of Maryland)</p>
10am	<p>TCAD-EDA Assisted BTI-HCD Reliability Framework from Devices to Circuits <i>Cap Rock I, II & III</i></p>
	<p>TMD.2 (Tutorial) - TCAD-EDA Assisted BTI-HCD Reliability Framework from Devices to Circuits » Souvik Mahapatra¹ (1. Indian Institute of Technology Bombay)</p>
11:30am	<p>Lunch <i>Vineyard</i></p>
	<p>12:30pm Testing for Wear and Abnormal Conditions of Power IGBT Modules <i>Val Verde</i></p>
	<p>TMA.3 (Tutorial) - Testing for Wear and Abnormal Conditions of Power IGBT Modules » Francesco Iannuzzo¹ (1. Aalborg University)</p>
	<p>12:30pm Designing for Analog Reliability: From Components to Circuits <i>International I & II</i></p>
	<p>TMB.3 (Tutorial) - Designing for Analog Reliability: From Components to Circuits » Dhanoop Varghese¹, Sunglyong Kim² (1. Texas Instruments, 2. Texas Instruments, Inc.)</p>
	<p>12:30pm Materials Analysis Techniques in Semiconductor <i>International III & IV</i></p>
	<p>TMC.3 (Tutorial) - Materials Analysis Techniques in Semiconductor » Ling Pan¹ (1. Intel)</p>
	<p>12:30pm Materials Engineering Challenges for Neuromorphic Computing <i>Cap Rock I, II & III</i></p>
	<p>TMD.3 (Tutorial) - Materials Engineering Challenges for Neuromorphic Computing » Siddarth Krishnan¹ (1. Applied Materials)</p>
	<p>2pm IRPS Break <i>International Foyer</i></p>
	<p>2:20pm Circuit <i>Val Verde</i></p>
	<p>YA1 (IRPS YIR) - Circuit Reliability: Main Review » James Tschanz¹ (1. Intel Corporation)</p>



Continued from **Monday, 30 March**

YA2 (IRPS YIR) - Circuit Reliability: EDA Aspects

» [Georgios Konstadinidis](#)¹ (1. Google)

3:10pm **RF/mmW/5G**
Val Verde

YA3 (IRPS YIR) - RF/mmW/5G Reliability: CMOS/SiGe

» [Fernando Guarin](#)¹ (1. GLOBALFOUNDRIES)

YA4 (IRPS YIR) - RF/mmW/5G Reliability: GaN HEMT

» [Enrico Zanoni](#)¹ (1. University of Padova)

4pm **IRPS Break**

4:10pm **Memory**
Val Verde

YA5 (IRPS YIR) - Memory

» [Chandra Mouli](#)¹ (1. Micron)

Tuesday, 31 March

7am **Breakfast**
Texas Grande

8:30am **IRPS Welcome & Introduction**
Texas Grande

9:05am **Plenary Keynote I**
Texas Grande

PK1 (Plenary Keynote) - The Future of Compute: Reliability and Resiliency in the Era of Data Transformation

» [Michael C. Mayberry](#)¹, Gaudenzio Meneghesso² (1. Intel, 2. UniPD)

9:40am **Plenary Keynote II**
Texas Grande

PK2 (Plenary Keynote) - Power Semiconductor Reliability – An Industry Perspective on Status and Challenges

» [Oliver Häberlen](#)¹, Gaudenzio Meneghesso² (1. Infineon Technologies Austria AG, 2. UniPD)

10:15am **Plenary Keynote III**
Texas Grande

PK3 (Plenary Keynote) - IoT End-node Device: Built to Last

» [Alessandro Piovaccari](#)¹, Gaudenzio Meneghesso² (1. SiLabs, 2. UniPD)

10:50am **Break & Exhibits**
Texas Grande

11:10am **2A - Circuit Reliability and Aging I**
Texas Grande

2A.1 (Invited) - An Industry-Standard Approach Toward Modeling Device Aging

» [Colin Shaw](#)¹ (1. Silvaco)

2A.2 - Fast & Accurate Methodology for Aging Incorporation in Circuits using Adaptive Waveform Splitting (AWS)

» [Subrat Mishra](#)¹, Pieter Weckx¹, Ji-Yung Lin¹, Ben Kaczer², Dimitri Linten², Alessio Spessot¹, Francky Catthoor¹ (1. IMEC, 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium)



Continued from **Tuesday, 31 March**

2A.3 - BTI and HCD Degradation in a Complete 32 x 64 bit SRAM Array – including Sense Amplifiers and Write Drivers – under Processor Activity

» Victor M. van Santen¹, Simon Thomann¹, Chaitanya Pasupuleti², Paul R. Genssler¹, Narendra Gangwar², Uma Sharma², Jörg Henkel¹, Souvik Mahapatra², Hussam Amrouch¹ (1. Karlsruhe Institute of Technology (KIT), 2. Indian Institute of Technology Bombay)

11:10am **2B - RF/mmW/5G Reliability I**
International I & II

2B.1 (Invited) - Reliability Physics of GaN HEMT Microwave Devices: The Age of Scaling

» Enrico Zanoni¹, Matteo Meneghini², Gaudenzio Meneghesso², Fabiana Rampazzo², Daniele Marcon², Veronica Zhan Gao², Francesca Chiochetta², Andreas Graff³, Frank Altmann³, Michel Simon-Najasek³, David Poppitz³ (1. UniPD, 2. University of Padova, 3. IMWS)

2B.2 - Short-term reliability of high performance Q-band AlN/GaN HEMTs

» Riad KABOUCHE¹, Kathia Harrouche¹, Etienne Okada¹, Farid MEDJDOUB¹ (1. IEMN-University of Lille)

2B.3 (Invited) - Silicon Based RF Reliability Challenges for 5G Communication

» Paul Colestock¹, Srinivasan Purushothaman¹, Fernando Guarin¹ (1. GLOBALFOUNDRIES)

11:10am **2C - Reliability Testing I**
International III & IV

2C.1 - A Novel 'I-V Spectroscopy' Technique to Deconvolve Threshold Voltage and Mobility Degradation in LDMOS Transistors

» Yen-Pu Chen¹, Bikram Mahajan¹, Dhanoop Varghese², Srikanth Krishnan², Vijay Reddy², Muhammad Ashraf Alam¹ (1. Purdue University, 2. Texas Instruments)

2C.2 - Studies of Bias Temperature Instabilities in 4H-SiC DMOSFETs

» Amartya Ghosh¹ (1. The Pennsylvania State University)

2C.3 - Surge Energy Robustness of GaN Gate Injection Transistors

» Ruizhe Zhang¹, Joseph P. Kozak¹, Jingcun Liu¹, Ming Xiao¹, Yuhao Zhang¹ (1. Virginia Polytechnic Institute and State University)

12:30pm **Lunch**
Vineyard

1:40pm **3A - Circuit Reliability and Aging II**
Texas Grande

3A.1 (Invited) - A Novel Approach to In-field, In-mission Reliability Monitoring Based on Deep Data

» Evelyn Landman¹, Tamar Naishlos², Noam Brousard³ (1. CTO, ProteanTecs, 2. Director of Marketing, proteanTecs, 3. VP System, proteanTecs)

3A.2 (Invited) - Voltage Regulator Reliability

» Saibal Mukhopadhyay¹, Venkata Chaitanya Krishna Chekuri², Arvind Singh², Nael Mizanur Rahman², Edward Lee² (1. Georgia Tech, 2. Georgia Institute of Technology)

3A.3 (Invited) - Experimental Monitoring of Aging in CMOS RF Linear Power Amplifiers: Correlation Between Device and Circuit Degradation

» Rosana Rodriguez¹, Albert Crespo-Yepes¹, Javier Martin-Martinez¹, Montse Nafria², Xavier Aragones³, Diego Mateo³, Enrique Barajas³ (1. Universitat Autònoma de Barcelona, 2. UAB, 3. Universitat Politècnica de Catalunya)

3A.4 - Hot-Carrier induced Breakdown events from Off to On mode in NEDMOS

» Alain Bravaix¹, Edith KUSSENER¹, David NEY², Xavier Federspiel², Florian Cacho³ (1. ISEN, 2. ST Microelectronics, 3. STMicroelectronics)



Continued from **Tuesday, 31 March**

3A.5 - Statistical Characterization of BTI and RTN using Integrated pMOS Arrays

» [Bernhard Stampfer](#)¹ (1. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria)

1:40pm

3B - Wide-Bandgap Semiconductors I

International I & II

3B.1 (Invited) - Ruggedness of SiC Devices Under Extreme Conditions

» [Peter Friedrichs](#)¹ (1. Infineon)

3B.2 - Physics of Degradation in SiC MOSFETs Stressed by Over-voltage and Over-current Switching

» [Joseph P. Kozak](#)¹, Ruizhe Zhang¹, Jingcun Liu¹, Khai Ngo¹, Yuhao Zhang¹ (1. Virginia Polytechnic Institute and State University)

3B.3 - Non-Isothermal Simulations to Optimize SiC MOSFETs for Enhanced Short-Circuit Ruggedness

» [Dongyoung Kim](#)¹, Adam Morgan¹, Nick Yun¹, Woongje Sung¹, Anant Agarwal², Robert Kaplar³ (1. SUNY Polytechnic Institute, 2. The Ohio State University, 3. Sandia National Labs)

3B.4 - Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs

» [Thomas Aichinger](#)¹, Matthias Schmidt² (1. Infineon Technologies Austria AG, 2. Infineon Technologies AG)

3B.5 - Influence of high-voltage gate-oxide pulses on the BTI behavior of SiC MOSFETs

» [Sebastian Maaß](#)¹, Thomas Aichinger², Gerald Rescher², Hans Reisinger¹ (1. Infineon Technologies AG, 2. Infineon Technologies Austria AG)

1:40pm

3C - Neuromorphic Computing Reliability I

International III & IV

3C.1 (Invited) - Introduction of Non-Volatile Computing In Memory (nvCIM) by 3D NAND Flash for Inference Accelerator of Deep Neural Network (DNN) and the Read Disturb Reliability Evaluation

» [Hang-Ting Lue](#)¹ (1. Macronix)

3C.2 - Device-aware inference operations in SONOS non-volatile memory arrays

» [Christopher Bennett](#)¹, T. Patrick Xiao¹, Ryan Dellana¹, Ben Feinberg¹, Venkatraman Prabhakar², Krishnaswamy Ramkumar², Vineet Agrawal², Long Hinh², Swatilekha Saha², Vijay Raghavan², Ramesh Chetthuvetty², Sapan Agarwal¹, Matt Marinella¹ (1. Sandia National Labs, 2. Cypress Semiconductor)

3C.3 - Superior Data Retention of Programmable Linear RAM (PLRAM) for Compute-in-Memory Application

» [Shifan Gao](#)¹, Cong Yu¹, Zeyu Zhang¹, Xiang Qiu², Choonghyun Lee¹, Yi Zhao¹ (1. Zhejiang University, 2. Flash Billion)

3C.4 - Gate-Oxide Trapping Enabled Synaptic Logic Transistors

» [Xin Ju](#)¹, Diing shenp Ang¹ (1. Nanyang Technological University)

3C.5 - Memory Update Characteristics of Carbon Nanotube Memristors (NRAM) Under Circuitry-relevant Operation Conditions

» [Dmitry Veksler](#)¹, Gennadi Bersuker¹, Pragya Shrestha², Charles Cheung³, Jason Campbell², Adam Bushmaker¹, Maribeth Mason¹, Tom Rueckes⁴, Lee Cleveland⁴, Harry Luan⁴, David Gilmer⁴ (1. The Aerospace Corporation, 2. National Institute of Standards and Technology, 3. NIST, 4. Nantero Inc.)

3:50pm

Break & Exhibits

Texas Grande

4:10pm

4A - Metallization/BEOL Reliability I

Texas Grande

4A.1 - Reliability Characteristics of a High Density Metal-Insulator-Metal Capacitor on Intel's 10+ Process

» [Cheyun Lin](#)¹ (1. Intel Corporation)



Continued from **Tuesday, 31 March**

4A.2 - Impact of Anode-side Defect Generation on Inter-Level TDDB Degradation in Cu/Low-k Damascene Structures

» [Naohito Suzumura](#)¹, Kazuyuki Omori¹, Hideaki Tsuchiya¹, Hideki Aono¹, Tomohiro Yamashita¹ (1. Renesas Electronics Corporation)

4A.3 - Dielectric Reliability Study of 21 nm Pitch Interconnects with Barrierless Ru Fill

» [Alicja Lesniewska](#)¹, Davide Tierno¹, Philippe Roussel¹, Victor Vega Gonzalez¹, Marleen van der Veen¹, Patrick Verdonck², Nicolas Jourdan², Christopher J. Wilson², Kristof Croes³, Zsolt Tokei² (1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 2. IMEC, 3. IMEC, Kapeldreef 75, B-3001 Leuven)

4:10pm

4B - RF/mmW/5G Reliability II

International I & II

4B.1 - A Novel Methodology to Evaluate RF Reliability on SOI CMOS-based Power Amplifier for mmWave Applications

» [Srinivasan Purushothaman](#)¹, Paul Colestock¹, Stephen Moss¹, Thomas Samuels¹, Fernando Guarin¹, Byoung Min¹ (1. GLOBALFOUNDRIES)

4B.2 - Exploring the DC reliability metrics for scaled GaN-on-Si devices targeted for RF/5G applications

» [Vamsi Putcha](#)¹, Erik Bury¹, Jacopo Franco¹, Amey Walke¹, Simeng Zhao², Uthayasankaran Peralagu¹, Ming Zhao¹, AliReza Alian¹, Ben Kaczer¹, Niamh Waldron¹, Dimitri Linten¹, Bertrand Parvais¹, Nadine Collaert¹ (1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 2. vanderbilt university)

4B.3 (Invited) - The Role of RF Operational Life Testing in Evaluating III-V Devices Addressing RF Through Millimeter-wave Applications

» [Elias Reese](#)¹ (1. Qorvo)

4:10pm

4C - System Electronics Reliability

International III & IV

4C.1 (Invited) - Challenges in Prognostics and Health Management of Electronic Systems

» [Michael Azarian](#)¹ (1. Univ Maryland/CALCE)

4C.2 - Use of Silicon-based Sensors for System Reliability Prediction

» [Dmitry Goloubev](#)¹, Shi-Jie Wen¹, Donald Allen¹, Ranjani Ram¹, Firdous Bano¹, Nithin Guruswamy¹, James Turman¹ (1. Cisco Systems)

4C.3 - Early Diagnosis and Prediction of Wafer Quality using Machine Learning on sub-10nm Logic Technology

» [Heungkook Ko](#)¹, Sangwoo Pae¹, Dongjoon Lee¹, Sena Park¹, Sung Ryul Kim¹, Jihyun Ryu¹, Euncheol Lee¹, Seoung Bum Kim², Hyungrok Do², Hyungu Kahng², Yoon Sang Cho², Jiyeon Lee², Dongkyun Kwon¹, Yongsung Ji¹, Hai Jiang¹, Tae-Young Jeong¹, Taiki Uemura¹, Mingu Kwak² (1. SAMSUNG ELECTRONICS, 2. Korea University)

6pm

Workshop Reception

Texas Grande

7pm

HCI/BTI

International I & II

Chaired by: Xavier Federspiel and Souvik Mahapatra

7pm

BEOL

Delaney I & II

Chaired by: Ki-Don Lee and Gavin Hall

BEOL

7pm

Neuromorphic

Cross Timbers I & II

Chaired by: Gennadi Bersuker and Matt Marinella and Kin Leong Pey



Continued from **Tuesday, 31 March**

7pm **Solid State Drive**
International III & IV
Chaired by: Jay Sarkar and Nikolaos Papandreou

7pm **Wide-Bandgap I**
Cap Rock I, II & III
Chaired by: Shireen Warnock and Matteo Meneghini

Wide-Bandgap I

8pm **Circuit Reliability**
International I & II
Chaired by: Valeriy Sukharev and Georgios Konstadinidis

8pm **Automotive**
Delaney I & II
Chaired by: Riccardo Mariani and Udeerna Doppalapudi

Automotive

8pm **RF/mmW/5G**
Cross Timbers I & II
Chaired by: Fernando Guarin and Farid Medjdoub

8pm **Emerging Memory**
International III & IV
Chaired by: Joe McCrate and Tetsuo Endoh

8pm **Wide-Bandgap II**
Cap Rock I, II & III
Chaired by: Aivars J. Lelis

Wednesday, 1 April

7am **Breakfast**
Texas Grande

8:30am **5A - Transistors I**
Texas Grande

5A.1 (Invited) - Modeling Framework for Transistor Aging Playback in Advanced Technology Nodes

» Inanc Meric¹, Stephen Ramey¹, Steven Novak², Jeffrey Hicks¹, Sivakumar P. Mudanai³, Satrajit Gupta³ (1. Intel Corporation, 2. Logic Technology Development Quality and Reliability, Intel Corporation, 3. Intel)

5A.2 - A Compact Physics Analytical Model for Hot-Carrier Degradation

» Stanislav Tyaginov¹, Alexander Grill², Michiel Vandemaele¹, Tibor Grasser³, Geert Hellings¹, Alexander Makarov⁴, Markus Jech⁴, Dimitri Linten², Ben Kaczer² (1. IMEC, 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 3. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria, 4. Vienna Technical University)

5A.3 - The Influence of Gate Bias on the Anneal of Hot-Carrier Degradation

» Michiel Vandemaele¹, Kai-Hsin Chuang¹, Erik Bury², Stanislav Tyaginov², Guido Groeseneken¹, Ben Kaczer³ (1. imec + KU Leuven, 2. IMEC, 3. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium)



Continued from **Wednesday, 1 April**

5A.4 - Analysis of BTI, SHE Induced BTI and HCD Under Full VG/VD Space in GAA Nano-Sheet N and P FETs

» [Nilotpal Choudhury](#)¹, Uma Sharma², Huimei Zhou³, Ricki Southwick³, Miaomiao Wang³, Souvik Mahapatra¹ (1. Indian Institute of Technology Bombay, 2. India, 3. IBM Research)

5A.5 - Comparison of Variability of HCI Induced Drift for SiON and HKMG Devices

» [Xavier Federspiel](#)¹, Cheikh Diouf², Florian Cacho², Emmanuel Vincent² (1. ST Microelectronics, 2. STMicroelectronics)

8:30am **5B - Wide-Bandgap Semiconductors II**
International I & II

5B.1 (Invited) - Defect Spectroscopy in SiC Devices

» [Michael Waltl](#)¹ (1. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria)

5B.2 (Invited) - Challenges and Peculiarities in Developing New Standards for SiC

» [Don Gajewski](#)¹ (1. Cree/Wolfspeed)

5B.3 - Towards a Robust Approach to Threshold Voltage Characterization and High Temperature Gate Bias Qualification

» [Daniel Habersat](#)¹, Aivars J. Lelis², Ronald Green¹ (1. Optical and Power Devices Branch, U.S. Army Combat Capabilities Development Command — Army Research Laboratory, 2. United States Army Research Laboratory)

5B.4 - Similarities and Differences of BTI in SiC and Si Power MOSFETs

» [Judith Berens](#)¹, Magdalena Weger¹, Gregor Pobegen¹, Thomas Aichinger², Gerald Rescher², Christian Schleich³, Tibor Grasser³ (1. KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Europastr. 8, 9524 Villach, Austria, 2. Infineon Technologies Austria AG, 3. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria)

5B.5 - Non-Intrusive Methodologies for Characterization of Bias Temperature Instability in SiC Power MOSFETs

» [Jose Ortiz Gonzalez](#)¹, Olayiwola Alatise¹, Phil Mawby¹ (1. University of Warwick)

8:30am **5C - Reliability Testing II**
International III & IV

5C.1 - In-Situ Monitoring of Self-Heating Effect and Its Quantitative Impact on Hot Carrier Injection in Aggressively Scaled SOI FinFETs Under Dynamic Circuit Operation

» [Yiming Ou](#)¹, Jiwu Lu², Junkang Li¹, Zhuo Chen¹, Jie Zhang¹, Chunlong Li³, Shih-Wuu Lee¹, Yi Zhao¹ (1. Zhejiang University, 2. Hunan University, 3. Institute of Microelectronics, Chinese Academy of Sciences, Beijing)

5C.2 - A fast and test-proven methodology of assessing RTN/fluctuation on deeply scaled nano pMOSFETs

» [Rui Gao](#)¹, Mehzabeen Mehedi², Haibao Chen³, Xinsheng Wang⁴, Jianfu Zhang², Xiaoling Lin¹, Zhiyuan He¹, Yiqiang Chen¹, Dengyun Lei¹, Yun Huang¹, ZHIGANG JI⁵, Yunfei En¹, Runsheng Wang⁶ (1. China Electronic Product Reliability and Environment Research Institute, 2. School of Engineering, Liverpool John Moores University, 3. School of Microelectronics, Shanghai Jiaotong University, 4. Department of Electronics & Electrical Engineering, Harbin Institute of Technology at Weihai, 5. National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiaotong University, 6. Institute of Microelectronics, Peking University)

5C.3 - Reliability and Variability of Advanced CMOS Devices at Cryogenic Temperatures

» [Alexander Grill](#)¹, Erik Bury², Jakob Michl³, Stanislav Tyaginov², Dimitri Linten¹, Tibor Grasser⁴, Bertrand Parvais¹, Ben Kaczer¹, Michael Waltl⁴, Iuliana Radu¹ (1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 2. IMEC, 3. Institute for Microelectronics, TU Wien, Vienna, Austria, 4. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria)



Continued from **Wednesday, 1 April**

5C.4 - Quantum Mechanical Charge Trap Modeling to Explain BTI at Cryogenic Temperatures

» [Jakob Michl](#)¹, Alexander Grill², Dieter Claes², Gerhard Rzepa³, Ben Kaczer², Dimitri Linten², Iuliana Radu², Tibor Grasser¹, Michael Walt¹ (1. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria, 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 3. Global TCAD Solutions GmbH, Vienna, Austria)

5C.5 - Nanoindentation to investigate IC stability using ring oscillator circuits as a CPI sensor

» [Simon Schlipf](#)¹, André Clausner¹, Jens Paul², Simone Capecci², Laura Wambera³, Karsten Meier³, Ehrenfried Zschech¹ (1. Fraunhofer Institute for Ceramic Technologies and Systems IKTS, 2. GLOBALFOUNDRIES, 3. Technische Universität Dresden)

10:50am **Break & Exhibits**
Texas Grande

11:35am **Lunch**
Vineyard

12:35pm **6A - ESD and Latchup**
Texas Grande

6A.1 - How to Achieve Moving Current Filament in High Voltage LDMOS Devices: Physical Insights & Design Guidelines for Self-Protected Concepts

» [kranthi Nagothu](#)¹, Sampath Kumar Boeila¹, Chirag Garg¹, Akram Salman², Gianluca Boselli², Mayank Shrivastava¹ (1. Indian Institute of Science, 2. Texas Instruments)

6A.2 - Over-Voltage Protection on the CC Pin of USB Type-C Interface against Electrical Overstress Events

» Chao-Yang Ke¹, [Ming-Dou Ker](#)¹ (1. Institute of Electronics, National Chiao-Tung University)

6A.3 - Design Insights to Address Low Current ESD Failure and Power Scalability Issues in High Voltage LDMOS-SCR Devices

» [kranthi Nagothu](#)¹, Sampath Kumar Boeila¹, Gianluca Boselli², Akram Salman², Mayank Shrivastava¹ (1. Indian Institute of Science, 2. Texas Instruments)

6A.4 - Threshold Voltage Shift in a-Si:H Thin film Transistors under ESD stress Conditions

» [Rajat Sinha](#)¹, Prasenjit Bhattacharya¹, Sanjiv Sambandan¹, Mayank Shrivastava¹ (1. Indian Institute of Science)

6A.5 - Sub-nanosecond Reverse Recovery Measurement for ESD Devices

» [Alex Ayling](#)¹, Shudong Huang¹, Elyse Rosenbaum¹ (1. University of Illinois - Urbana Champaign)

6A.6 - Improved Turn-on Uniformity & Failure Current Density by n- & p-Tap Engineering in Fin Based SCRs

» [Monishmurali M](#)¹, Milova Paul¹, Mayank Shrivastava¹ (1. Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, Karnataka, 560012, India)

12:35pm **6B - Wide-Bandgap Semiconductors III**
International I & II

6B.1 - A Generalized Approach to Determine the Switching Lifetime of A GaN FET

» [Sandeep Bahi](#)¹, Francisco Baltazar¹, Yong Xie¹ (1. Texas Instruments)

6B.2 - Charge Trapping and Stability of E-Mode p-gate GaN HEMTs Under Soft- and Hard- Switching Conditions

» [Fabrizio Masin](#)¹, Matteo Meneghini¹, Eleonora Canato¹, Alessandro Barbato¹, Carlo De Santi¹, Arno Stockman², Abhishek Banerjee², Peter Moens², Enrico Zanoni¹, Gaudenzio Meneghesso¹ (1. UniPD, 2. ON Semiconductor)



Continued from **Wednesday, 1 April**

6B.3 - Trap Dynamics Model Explaining the RON Stress/Recovery Behavior in Carbon-Doped Power AlGaIn/GaN MOS-HEMTs

» [Nicolò Zagni](#)¹, Alessandro Chini¹, Francesco Maria Puglisi¹, Paolo Pavan¹, Matteo Meneghini², Gaudenzio Meneghesso³, Enrico Zanoni³, Giovanni Verzellesi¹ (1. University of Modena and Reggio Emilia, 2. University of Padova, 3. UniPD)

6B.4 - Demonstration of Bilayer Gate Insulator for Improved Reliability in GaN-on-Si Vertical Transistors

» [Kalparupa Mukherjee](#)¹, Carlo De Santi¹, Matteo Borga¹, Shuzhen You², Karen Geens², Benoit Bakeroot³, Stefaan Decoutere², Gaudenzio Meneghesso¹, Enrico Zanoni¹, Matteo Meneghini¹ (1. UniPD, 2. IMEC, 3. University of Ghent)

6B.5 - Robust avalanche in GaN leading to record performance in Avalanche Photo Diode

» [Dong Ji](#)¹, Burcu Ercan², Garrett Benson³, AKM Newaz³, Srabanti Chowdhury¹ (1. Stanford University, 2. University of California at Davis, 3. San Francisco State University)

6B.6 - Failure Analysis of 100 nm AlGaIn/GaN HEMTs Stressed under On- and Off-State Stress

» [Tobias Kemmer](#)¹, Michael Dammann¹, Martina Baeumler¹, Vladimir Polyakov¹, Peter Brückner¹, Helmer Konstanzer¹, Rüdiger Quay¹, Oliver Ambacher¹ (1. Fraunhofer IAF, Fraunhofer Institute for Applied Solid State Physics)

6C.1 - Study of the Walk-Out Effect of Junction Breakdown Instability of the High-Voltage Depletion-Mode N-Channel MOSFET for NAND Flash Peripheral Circuit and an Effective Layout Solution

» [Chieh Lo](#)¹, Teng-Hao Yeh¹, Yung-Hsiang Chen², Wei-Chen Chen¹, Hang-Ting Lue¹, Chu-Yung Liu², Yao-Wen Chang², Keh-Chung Wang¹, Chih-Yuan Lu³ (1. Macronix Emerging Central Lab., Macronix International Co., Ltd., 2. Technology Development Center, Macronix International Co., Ltd., 3. Macronix Emerging Central Lab., Technology Development Center, Macronix International Co., Ltd.)

6C.2 - Relevance of fin dimensions and high-pressure anneals on hot-carrier degradation

» [Adrian Chasin](#)¹, Jacopo Franco², Erik Bury³, Romain Ritzenthaler², Eugenio Dentoni Litta², Alessio Spessot², Naoto Horiguchi¹, Dimitri Linten², Ben Kaczer² (1. IMEC, Kapeldreef 75, B-3001 Leuven, 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 3. IMEC)

6C.3 - A new technique for evaluating stacked nanosheet inner spacer TDDDB reliability

» [Tian Shen](#)¹, Koji Watanabe¹, Huimei Zhou¹, Michael Belyansky¹, Erin Stuckert¹, Jingyun Zhang¹, Andrew Greene¹, Baskar Veeraraghavan¹, Miaomiao Wang¹ (1. IBM Research)

6C.4 - Trap Density Modulation for IO FinFET NBTI Improvement

» [Rakesh Ranjan](#)¹, Charles Larow¹, Ki-Don Lee¹ (1. samsung Austin Semiconductor, LLC)

6C.5 - A New Implementation Approach for Reliability Design Rules against Plasma Induced Charging Damage from Well Configurations of Complex ICs

» [Andreas Martin](#)¹, Angelika Kamp¹ (1. Infineon Technologies AG)

6C.6 - First Insights into Electro-Thermal Stress Driven Time-Dependent Permanent Degradation & Failure of CVD Monolayer MoS2 Channel

» [Ansh](#)¹, Gaurav Sheoran¹, Jeevesh Kumar¹, Mayank Shrivastava¹ (1. Indian Institute of Science)

12:35pm **6C - Process Integration**

International III & IV

3:10pm **Break & Exhibits**

Texas Grande



Continued from **Wednesday, 1 April**

3:30pm **7A - Memory Reliability I**
Texas Grande

7A.1 - Origins and Signatures of Tail Bit Failures in Ultrathin MgO Based STT-MRAM

» [Jia Hao Lim](#)¹, Nagarajan Raghavan², Jae Hyun Kwon¹, Tae Young Lee¹, Robin Chao¹, Nyuk Leong Chung¹, Kazutaka Yamane¹, Naganivetha Thiyagarajah¹, Vinayak Bharat Naik¹, Kin Leong Pey² (1. GLOBALFOUNDRIES Singapore Pte. Ltd, 2. Singapore University of Technology and Design)

7A.2 - Magnetic Immunity Guideline for Embedded MRAM Reliability to Realize Mass Production

» Tae Young Lee¹, Kazutaka Yamane¹, LEE YONG HAU¹, Robin Chao¹, Nyuk Leong Chung¹, Vinayak Bharat Naik¹, SIVABALAN K¹, Jae Hyun Kwon¹, [Jia Hao Lim](#)¹, Wah Peng NEO¹, Kevin KHUA¹, Naganivetha Thiyagarajah¹, Suk Hee JANG¹, Behtash Behin-Aein¹, Eng Huat TOH¹, YUICHI OTANI¹, DINGGUI ZENG¹, NIVETHA BALASANKARAN¹, Lian Choo GOH¹, Timothy LING¹, Jay HWANG¹, LEI ZHANG¹, Rachel LOW¹, Soon Leng TAN¹, Chim Seng SEET¹, Jia Wen TING¹, Stanley ONG¹, Young Seon YOU¹, Swee Tuck WOO¹, Elgin QUEK¹, Soh Yun SIAH¹ (1. GLOBALFOUNDRIES)

7A.3 - Understanding and empirical fitting the breakdown of MgO in end-of-line annealed MTJs

» [Simon Van Beek](#)¹, Barry O'Sullivan¹, Sebastien Couet¹, Dimitri Linten¹, Davide Crotti², Gouri Kar¹ (1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 2. IMEC)

7A.4 - Impact of Ferroelectric Wakeup on Reliability of Laminate based Si-doped Hafnium Oxide (HSO) FeFET Memory Cells

» [Tarek Ali](#)¹, Kati Kühnel², Malte Czernohorsky², Matthias Rudolph², Björn Pätzold², Ricardo Olivo², David Lehninger², Konstantin Mertens², Franz Müller², Maximilian Lederer², Raik Hoffmann², Clemens Mart², Mahsa Kalkani², Philipp Steinke², Thomas Kämpfe², Johannes Müller³, Jan Van Houdt⁴, Konrad Seidel², Lukas M. Eng⁵ (1. Fraunhofer IPMS-Center Nanoelectronic Technologies (CNT), 2. Fraunhofer IPMS Center Nanoelectronic Technologies (CNT), 3. GLOBALFOUNDRIES Fab1 LLC and Co. KG, 4. imec, ESAT-Katholieke Universiteit Leuven, 5. Institut für Angewandte Physik, Technische Universität Dresden)

3:30pm **7B - IC Product Reliability I**
International I & II

7B.1 - Estimation of Product Reliability using TDDB Simulation and Statistical EM Method

» [Jae-Gyung Ahn](#)¹, Ping-Chin Yeh¹, Jonathan Chang¹ (1. Xilinx, Inc.)

7B.2 - Thermal Characterization and TCAD Modeling of a Power Amplifier in 45RFSOI for 5G mmWave Applications

» [Peter Paliwoda](#)¹, Mohamed Rabie¹, Oscar Restrepo¹, Eduardo Silva¹, Erdem Kaltalioglu², Fernando Guarin¹, Kenneth Barnett¹, Jeffrey Johnson¹, William Taylor¹, Myra Boenke¹, Byoung Min¹ (1. GLOBALFOUNDRIES, 2. Globalfoundries US Inc)

7B.3 - Impact of X-Ray Radiation on the Reliability of Logic Integrated Circuits

» [Somayyeh Rahimi](#)¹, Christian Schmidt¹, Joy Liao¹, Howard Lee Marks¹, Kyung Mo Shin¹ (1. NVIDIA Corp.)

7B.4 - Stability and degradation of isolation and surface in Ga2O3 devices

» [Carlo De Santi](#)¹, Arianna Nardo¹, Man Hoi Wong², Ken Goto³, Akito Kuramata⁴, Shigenobu Yamakoshi⁵, Hisashi Murakami³, Yoshinao Kumagai³, Masataka Higashiwaki⁶, Gaudenzio Meneghesso¹, Enrico Zanoni¹, Matteo Meneghini¹ (1. University of Padova, 2. University of Massachusetts Lowell, 3. Tokyo University of Agriculture and Technology, 4. Novel Crystal Technology, 5. Tamura Corporation, 6. National Institute of Information and Communications Technology)



Continued from **Wednesday, 1 April**

3:30pm **7C - Failure Analysis**
International III & IV

7C.1 - STEM EBIC for High-Resolution Electronic Characterization

» [William Hubbard](#)¹, Zachary Lingley¹, Jesse Theiss¹, Miles Brodie¹, Brendan Foran¹ (1. The Aerospace Corporation)

7C.2 - High-Current State triggered by Operating-Frequency Change

» [Lyu Xu](#)¹, Jingchen Cao², Shi-Jie Wen³, Rita Fung³, James Markevitch³, Dennis Ball², [Bharat Bhuvra](#)² (1. vanderbilt, 2. vanderbilt university, 3. Cisco Systems)

7C.4 (Invited) - At-Speed Defect Localization by Combining Laser Scanning Microscopy and Power Spectrum Analysis

» [Edward Cole](#)¹, Mary Miller², Garth Kraus², Perry Robertson² (1. Sandia, 2. Sandia National Labs)

5:25pm **Break & Exhibits**
Texas Grande

6pm **Joint Poster Session & Reception**
Austin Ranch

P1 - Analysis of Hot Carrier Degradation in Cryo-CMOS

» [Wriddhi Chakraborty](#)¹, Uma Sharma², Souvik Mahapatra³, Suman Datta⁴ (1. UNIVERSITY OF NOTREDAME, 2. India, 3. Indian Institute of Technology Bombay, 4. University of Notre Dame)

P2 - Inverse Design of FinFET SRAM Cells

» [Rui Zhang](#)¹, Zhaocheng Liu¹, Kexin Yang¹, Taizhi Liu¹, Wenshan Cai¹, Linda Milor¹ (1. Georgia Institute of Technology)

P3 - Degradation Detection of Power Switches in a Three Phase Inverter using SSTDR Signal Embedded PWM Sequence

» [Roy Sourav](#)¹, Abu Hanif¹, Faisal Khan¹ (1. University of Missouri-Kansas City)

P4 - Novel Re-Configurable Circuits for Aging Characterization: Connecting Devices to Circuits

» [Ketul Sutaria](#)¹, Jihan Standfest¹, Inanc Meric¹, Amirhossein Davoody¹, Swaroop Kumar Namalapur¹, Trinadh Mutyala¹, Supriya P¹, Balkaran Gill¹, Stephen Ramey¹, Jeffrey Hicks¹ (1. Intel Corporation)

P5 - Evolution of Defect in AlGaIn-based Deep Ultraviolet Light Emitting Diodes During Electrical Stress

» [Yingzhe Wang](#)¹, Xuefeng Zheng¹, Jiaduo Zhu¹, Linlin Xu², Shengrui Xu¹, Jiangnan Dai², Xiaohua Ma¹, Peixian Li¹, Jincheng Zhang¹, Yue Hao¹ (1. Xidian University, 2. Huazhong University of Science and Technology)

P6 - Impact of Intrinsic Series Resistance on the Reversible Dielectric Breakdown Kinetics in HfO2 Memristors

» [Mireia Bargallo-Gonzalez](#)¹, Samuel Aldana², Marcos Maestro-Izquierdo¹, Francisco Jiménez-Molinós², Juan Bautista Roldán², Francesca Campabadal¹ (1. Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), 2. Universidad de Granada)

P7 - Reversible dielectric breakdown in h-BN stacks: a statistical study of the switching voltages

» Juan Bautista Roldán¹, D. Maldonado¹, Francisco Jiménez-Molinós¹, C. Acal¹, J.E. Ruiz-Castro¹, A.M. Aguilera¹, [Fei Hui](#)², J. Kong³, Y. Shi⁴, X. Jing², C Wen², M. A. Villena², [Mario Lanza](#)² (1. Universidad de Granada, 2. Soochow University, 3. Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, 4. imec, Kapeldreef 75, B-3001 Leuven)

P8 - Influence of the magnetic field on dielectric breakdown in memristors based on h-BN stacks

» David Maldonado¹, [Juan Bautista Roldán](#)¹, Andres Roldán¹, Francisco Jiménez-Molinós¹, Fei Hui², Y. Shi³, X. Jing², C Wen², [Mario Lanza](#)² (1. Universidad de Granada, 2. Soochow University, 3. imec, Kapeldreef 75, B-3001 Leuven)

P9 - Two-Regime Drift in Electrolytically Gated FETs and BioFETs

» Robin Wuytens¹, [Sybren Santermans](#)², Mihir Gupta¹, Bert Du Bois³, Simone Severi³, Liesbet Lagae¹, Wim Van Roy³, Koen Martens³ (1. imec + KU Leuven, 2. imec, 3. imec, Kapeldreef 75, B-3001 Leuven, Belgium)



Continued from Wednesday, 1 April

P11 - No Trouble Found (NTF) Customer Return Analysis

» [Thong Tran](#)¹, Sudheer Gundala¹, Komal Soni¹, Aaron Baker¹, Adam Fogle¹, Sandhya Chandrashekhar¹ (1. Cypress Semiconductor)

P12 - High Frequency TDDB of Reinforced Isolation Dielectric Systems

» [Tom Bonifield](#)¹, Jeff West¹, Honglin Guo¹, Hisashi Shichijo², Talha Tahir² (1. Texas Instruments, Inc., 2. University of Texas at Dallas)

P13 - Dynamic vs Static Burn-in for 16nm Production

» [Jeffrey Zhang](#)¹, Antai Xu¹, Daniel Gitlin¹, Desmond Yeo¹ (1. Xilinx Inc.)

P14 - Physical Insights into Phosphorene Transistor Degradation Under Exposure to Atmospheric Conditions and Electrical Stress

» [Jeevesh Kumar](#)¹, [Ansh](#)¹, Asha Yadav¹, Anant Singh¹, Andrew Naclerio², Dmitri Zakharov³, Piran Kidambi², Mayank Shrivastava¹ (1. Indian Institute of Science, 2. vanderbilt university, 3. Brookhaven National Laboratory)

P15 - Impact of Extrinsic Variation Sources on the Device-to-Device Variation in Ferroelectric FET

» [Kai Ni](#)¹, Aniket Gupta², Om Prakash², Simon Thomann², X. Sharon Hu³, [Hussam Amrouch](#)² (1. Rochester Institute of Technology, 2. Karlsruhe Institute of Technology, 3. University of Notre Dame)

P16 - Temperature Dependence and Temperature-Aware Sensing in Ferroelectric FET

» Aniket Gupta¹, [Kai Ni](#)², Om Prakash¹, X. Sharon Hu³, [Hussam Amrouch](#)¹ (1. Karlsruhe Institute of Technology, 2. Rochester Institute of Technology, 3. University of Notre Dame)

P17 - A Pulsed RTN Transient Measurement Technique: Demonstration on the understanding of the Switching in Resistance memory

» E R Hsieh¹, H. W. Cheng¹, Z. H. Huang¹, C. H. Chuang², S. P. Yang², [Steve Chung](#)² (1. Institute of Electronics, National Chiao-Tung University, 2. Institute of Electronics, National Chiao Tung University)

P18 - Reliability Analysis by Charge Migration of 3D SONOS Flash Memory

» [Jun Kyo Jeong](#)¹, gawon lee¹, Heehun Yang¹, Jaeyoung Sung¹, Hi-Deok Lee¹ (1. Chungnam National University)

P19 - Reliability of Industrial grade Embedded-STT-MRAM

» [Yongsung Ji](#)¹, Hyunjae Goo¹, Jungman Lim¹, Tae-Young Jeong¹, Taiki Uemura¹, Gun Rae Kim¹, Boil Seo¹, Seungbae Lee¹, Goeun Park¹, Jeongmin Jo¹, Sang Il Han¹, Kilho Lee¹, Junghyuk Lee¹, Sohee Hwang¹, Daesop Lee¹, Suksoo Pyo¹, Hyun Taek Jung¹, Shinhee Han¹, Seungmo Noh¹, Kiseok Suh¹, Sungyoung Yoon¹, Hyeonwoo Nam¹, Hyewon Hwang¹, Hai Jiang¹, Jinwoo Kim¹, Dongkyun Kwon¹, Yoonjong Song¹, Gwan-Hyeob Koh¹, Hwasung Rhee¹, Sangwoo Pae¹, Brandon Lee¹ (1. SAMSUNG ELECTRONICS)

P20 - Accelerated Temperature and Voltage Life Test on DRAM Cell Capacitor

» [KyungWoo Lee](#)¹ (1. SAMSUNG ELECTRONICS)

P21 - Double Layers Omega FETs with Ferroelectric HfZrO2 for One-Transistor Memory

» Kuan-Ting Chen¹, Shu-Tong Chang², Jessie Tseng³, [Min-Hung Lee](#)¹ (1. National Taiwan Normal University, 2. National Chung Hsing University, 3. synopsis)

P22 - Statistical Analysis of Bit-Errors Distribution for Reliability of 3-D NAND Flash Memories

» Nian-Jia Wang¹, KUANYI LEE¹, Hsin-Yi Lin¹, Wei-Hao Hsiao¹, [Ming-Yi Lee](#)¹, Li-Kuang Kuo¹, Ding-Jhang Lin¹, Yen-Hai Chao¹, Chih-Yuan Lu¹ (1. Macronix International Co. Ltd.)

P23 - Physical Origin of RESET Failure in TaO2 RRAM

» [Yuanzhi Ma](#)¹, Phoebe Yeoh¹, Liting Shen¹, Jonathan Goodwill¹, James Bain¹, Marek Skowronski¹ (1. Carnegie Mellon University)



Continued from **Wednesday, 1 April**

P24 - ON-state retention of Atom Switch eNVM for IoT/AI Inference Solution

» [Koichiro Okamoto](#)¹, Ryusuke Nebashi¹, Naoki Banno¹, Xu Bai¹, Hideaki Numata¹, Noriyuki Iguchi¹, Makoto Miyamura¹, Hiromitsu Hada¹, Kazunori Funahashi¹, Tadahiko Sugibayashi¹, Toshitsugu Sakamoto¹, Munehiro Tada¹ (1. NEC)

P25 - Open Block Characterization and Read Voltage Calibration of 3D QLC NAND Flash

» [Nikolaos Papandreou](#)¹, Haralampos Pozidis¹, Nikolas Ioannou¹, Thomas Parnell¹, Roman Pletka¹, Milos Stanisavljevic¹, Radu Stoica¹, Sasa Tomic¹, Patrick Breen², Gary Tressler², Aaron Fry², Timothy Fisher², Andrew Walls² (1. IBM Research - Zurich, 2. IBM Systems)

P26 - Stress Induced Voiding Behavior of Electroplated Copper Thin Films in Highly Scaled Cu/low-k interconnects

» [Clement Huang](#)¹ (1. Reliability Technology & Assurance Division, UMC Inc.)

P27 - Physics based modeling of bimodal electromigration failure distributions and variation analysis for VLSI interconnects

» [Sarath Mohanachandran Nair](#)¹, Rajendra Bishnoi¹, Mehdi Tahoori¹, Houman Zahedmanesh², Kristof Croes², Kevin Garello², Gouri Kar², Francky Catthoor² (1. Karlsruhe Institute of Technology (KIT), 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium)

P28 - BEoL Reliability, XPS and REELS Study on low-k Dielectrics to understand Breakdown Mechanisms

» [Bettina Wehring](#)¹, Raik Hoffmann¹, Lukas Gerlich¹, Malte Czernohorsky¹, Benjamin Uhlig¹, Robert Seidel², Tobias Barchewitz², Frank Schlaphof², Lutz Meinshausen², Christoph Leyens³ (1. Fraunhofer IPMS Center Nanoelectronic Technologies (CNT), 2. GLOBALFOUNDRIES, 3. Technical University of Dresden)

P29 - Reliability Characterization of Logic-Compatible NAND Flash Memory based Synapses with 3-bit per Cell Weights and 1uA Current Steps

» [Minsu Kim](#)¹, Jeehwan Song¹, Chris Kim¹ (1. University of Minnesota)

P30 - Reliability Aspects of SONOS Based Analog Memory for Neuromorphic Computing

» Venkatraman Prabhakar¹, [Krishnaswamy Ramkumar](#)¹, Vineet Agrawal¹, Long Hinh¹, Swatilekha Saha¹, Santanu Samanta¹, Ravindra Kapre¹ (1. Cypress Semiconductor)

P31 - Radiation Tolerance of 3-D NAND Flash Based Neuromorphic Computing System

» MD MEHEDI HASAN¹, Md Raquibuzzaman¹, Indranil Chatterjee², [Biswajit Ray](#)¹ (1. The University of Alabama in Huntsville, 2. Airbus)

P32 - Effects of Wiring Density and Pillar Structure on Chip Package Interaction for Advanced Cu Low-k Chips

» [Weishen Chu](#)¹, Laura Spinella¹, Dwayne R. Shirley², Mark Patterson³, Paul Ho¹ (1. The University of Texas at Austin, 2. Inphi Corporation, 3. inphi)

P33 - Effect of Residual TiN on Reliability of Au Wire Bonds during High Temperature Storage

» [John McGlone](#)¹, Guy Brizar¹, Daniel Vanderstraeten¹, Dorai Iyer¹, Sallie Hose¹, Jeff Gambino¹ (1. ON Semiconductor)

P34 - Backside Die-Edge and Underfill Fillet Cracks Induced by Additional Tensile Stress from Increasing Die-to-Package Ratio in Bare-Die FCBGA

» [Khai Nguyen](#)¹, Ernie Opiniano¹, Randolph Mah¹ (1. NVIDIA Corp.)

P36 - Study of Lower Voltage Protection against Plasma Process Induced Damage by Quantitative Prediction Technique

» [Yohei Hiura](#)¹, Shinichi Miyake¹, Shigetaka Mori¹, Koichi Matsumoto¹, Hidetoshi Ohnuma¹ (1. Sony Semiconductor Solutions Corporation)



Continued from Wednesday, 1 April

P37 - Reliability Characterization for 12V Application Using the 22FFL FinFET Technology

» [Chen-Yi Su](#)¹, Mark Armstrong¹, Sunny Chugh¹, Mohammed El-tanani¹, Hannes Greve¹, Hai Li¹, Mahjabin Maksud¹, Benjamin Orr¹, Christopher Perini¹, James Palmer¹, Leif Paulson¹, Stephen Ramey¹, James Waldemer¹, Yang Yang¹, Dave Young¹ (1. Intel Corporation)

P38 - Facile Route for Low-temperature Eco-friendly Solution Processed ZnSnO Thin-film Transistors

» [Tianshi Zhao](#)¹, Chun Zhao¹, Ivona Mitrovic², Enggee Lim¹, Li Yang¹, Chenghu Qiu¹, Cezhou Zhao¹ (1. Xi'an Jiaotong-Liverpool University, 2. University of Liverpool)

P39 - Investigation of VT Shift Extraction Techniques with Fast Measurement in NBTI

» [Yu-Hsing Cheng](#)¹, Michael Cook¹, Chris Kendrick¹ (1. ON Semiconductor)

P40 - A Novel Calculation Method of Activation Energy for Accelerated Life Test

» [youjin jeon](#)¹, haedong no¹, jongtaek seong¹, daewon kim¹, kirock kwon¹, kihwan choi¹ (1. SAMSUNG ELECTRONICS)

P41 - A test method for MOSFET Voltage derating design verification in switching power supply circuit

» [Wei Li](#)¹, ZeYa Peng¹, Jiahui Li¹ (1. China CEPREI Laboratory)

P43 - Reliability Stressing Control Using Jacobian Feedback Kelvin Measurement on Intel Technologies

» [Peng Xiao](#)¹, Haris Hadziosmanovic¹, Rong Jiang¹, Misagh Rostami-asrabad¹, Stephen Ramey¹, Ilan Tsameret¹ (1. Intel Corporation)

P44 - Hybrid HCI Degradation in Sub-micron NMOSFET due to Mixed Back-end Process Damages

» [Kuifong Yu](#)¹, Xiaojuan Zhu¹, Rui Fang¹, Tingting Ma¹, Kun Han¹, Zhongyi Xia¹ (1. Yangtze Memory Technologies Co., Ltd.)

P45 - Impact of Radiation on Negative Capacitance FinFET

» Govind Bajpai¹, Aniket Gupta¹, Om Prakash¹, Girish Pahwa², Jörg Henkel¹, Yogesh Chauhan², [Hussam Amrouch](#)¹ (1. Karlsruhe Institute of Technology, 2. Indian Institute of Technology Kanpur)

P46 - Large-tilt Heavy Ions Induced SEU in Multiple Radiation Hardened 22 nm FDSOI SRAMs

» [Chang Cai](#)¹, Luchang Ding², Kai Zhao², Bingxu Ning², Mingjie Shen², Tianqi Liu¹, Jie Liu¹, Gengsheng Chen² (1. Institute of Modern Physics, Chinese Academy of Sciences, 2. State Key Laboratory of ASIC and System, Fudan University)

P47 - Temperature Dependence of Single Event Transient Pulse Widths for 7-nm Bulk FinFET Technology

» [Jingchen Cao](#)¹, Lyuan Xu¹, Shi-Jie Wen², Rita Fung², Balaji Narasimham³, Lloyd Massengill¹, Bharat Bhuvu¹ (1. vanderbilt university, 2. Cisco Systems, 3. Broadcom Inc.)

P48 - Using Partial Duplication With Compare to Detect Radiation-Induced Failure in a Commercial FPGA-Based Networking System

» Andrew Keller¹, [Jared Anderson](#)¹, Michael Wirthlin¹, Shi-Jie Wen², Rita Fung², Conner Chambers² (1. Brigham Young University, 2. Cisco Systems)

P49 - Characterizing Energetic Dependence of Low-Energy Neutron-induced MCUs in 65 nm bulk SRAMs

» [Wang LIAO](#)¹, Kojiro Ito², Yukio MITSUYAMA¹, Masanori Hashimoto² (1. Kochi University of Technology, 2. Osaka University)

P50 - Comparing Variation-tolerance and SEU/TID-Resilience of Three SRAM Cells in 28nm FD-SOI Technology: 6T, Quatro, and we-Quatro

» Le Dang Trang¹, [Dinh Trinh Linh](#)¹, Thanh Nguyen Dat¹, Chang Hong Min², Jinsang Kim¹, Jin-Woo Han³, Ik-Joon Chang¹ (1. Kyunghee Univeristy, 2. Kyu, 3. NASA)

P51 - Trends and Functional Safety Certification Strategies for Advanced Railway Automation Systems

» [Jyotika Athavale](#)¹, Andrea Baldovin¹, Michael Paulitsch¹ (1. Intel Corporation)



Continued from Wednesday, 1 April

P52 - An Interpretable Predictive Model for Early Detection of Hardware Failure

» [Artsiom Balakir](#)¹, Alan Yang¹, Elyse Rosenbaum² (1. University of Illinois - Urbana Champaign, 2. University of Illinois -)

P53 - A Novel HCI Reliability Model for RF/mmWave Applications in FDSOI Technology

» [Wafa Arfaoui](#)¹ (1. Mrs.)

P54 - Anomalous accelerated negative-bias- instability (NBI) at low drain bias

» [Charles Cheung](#)¹ (1. NIST)

P55 - Analysis of The Hole Trapping Detrapping Component of NBTI Over Extended Temperature Range

» [Nilotpal Choudhury](#)¹, Narendra Parihar¹, Souvik Mahapatra¹ (1. Indian Institute of Technology Bombay)

P56 - Effect of Different Ambients on the Recovery of Hot-Carrier Degraded Devices

» [Maurits de Jong](#)¹, Cora Salm¹, Jurriaan Schmitz¹ (1. University of Twente)

P57 - "shift and match" (s&m) method for channel mobility correction in degraded mosfets

» Linglin Jing¹, [Rui Gao](#)², ZHIGANG JI¹, Runsheng Wang³ (1. National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiaotong University, 2. China Electronic Product Reliability and Environment Research Institute, 3. Institute of Microelectronics, Peking University)

P58 - Self-healing LDMOSFET for high-voltage application on high-k/metal gate CMOS process

» [Jing-Chyi Liao](#)¹, Paul Ko², [M. H. Hsieh](#)³, zheng zeng⁴ (1. jc.liao@mediatek.com, 2. paul.ko@mediatek.com, 3. hank.hsieh@mediatek.com, 4. zheng.zeng@mediatek.com)

P59 - AC stress reliability study of a new high voltage transistor for logic memory circuits

» [Jordan Locati](#)¹, Vincenzo Della-Marca², Christian Rivero³, Arnaud Regnier³, Stephan Niel³, Karine Coulie² (1. STMicroelectronics, 190 avenue Célestin Coq, 13106 Rousset, France, 2. Aix-Marseille University, CNRS, IM2NP UMR 7334-F, 13997 Marseille, France, 3. STMicroelectronics, 190 avenue Célestin Coq, 13106 Rousset, France)

P60 - Analysis of charge-to-hot-carrier degradation in Ge pFinFETs

» [Wataru Mizubayashi](#)¹, Hiroshi Oka¹, Koichi Fukuda¹, Yuki Ishikawa¹, Kazuhiko Endo¹ (1. AIST)

P61 - Investigation of Random Telegraph Noise Characteristics with Intentional Hot Carrier Aging

» [Hyeong-Sub Song](#)¹, Sunil babu Eadi¹, Hyung-dong Song¹, Hyungwoong Choi¹, gawon lee¹, Hi-Deok Lee¹ (1. Chungnam National University)

P62 - Full Understanding of Hot Electrons and Hot/Cold Holes in the Degradation of p-channel Power LDMOS Transistors

» [Andrea Natale Tallarico](#)¹ (1. University of Bologna)

P63 - Front-plane and Back-plane Bias Temperature Instability of 22 nm Gate-last FDSOI MOSFETs

» [Yang Wang](#)¹, Qingqing Sun¹, Chen Wang¹, Tao Chen¹, Hao Liu¹, Chinte Kuo², Ke Zhou², Bin Feng Yin², Lin Chen¹ (1. State Key Laboratory of ASIC and System, Fudan University, 2. Shanghai Huali Microelectronics Corporation)

P64 - Comparative Study on the Energy Profile of NBTI-Related Defects in Si and Ferroelectric p-FinFETs

» [Longda Zhou](#)¹, Qingzhu Zhang², HONG YANG², ZHIGANG JI³, Zhaohao Zhang², Renren Xu², Huaxiang Yin², Wenwu Wang² (1. Institute of Microelectronics of the Chinese Academy of Sciences, 2. Institute of Microelectronics of Chinese Academy of Sciences, 3. School of Microelectronics, Shanghai Jiaotong University)



Continued from **Wednesday, 1 April**

P65 - Oxide Leakage Currents and E' Centers in 4H-SiC MOSFETs with Barium Passivation

» [James P. Ashton](#)¹, Patrick M. Lenahan¹, Daniel J. Lichtenwalner², Aivars J. Lelis³ (1. The Pennsylvania State University, 2. Wolfspeed, a Cree Company, 3. United States Army Research Laboratory)

P68 - Measurement of the Pre-Breakdown Characteristics in Silicon Carbide Power Devices by the Use of Radioactive Gamma Sources

» [Mauro Ciappa](#)¹, Marco Pocaterra¹ (1. ETH Zurich, Integrated Systems Laboratory)

P69 - Constant-Gate-Charge Scaling for Increased Short-Circuit Withstand Time in SiC Power Devices

» Madan Sampath¹, Dallas Morissette¹, [James Cooper](#)² (1. Purdue University, 2. Sonrisa Research, Inc. and Purdue University)

P70 - On the Root Cause of Dynamic ON Resistance Behavior in AlGaIn/GaN HEMTs

» [Sayak Dutta Gupta](#)¹, Vipin Joshi¹, RAJARSHI ROY CHAUDHURI¹, Anant Singh¹, Sirsha Guha¹, Mayank Shrivastava¹ (1. Indian Institute of Science)

P71 - Effects of Thermal Boundary Resistance on the Thermal Performance of GaN HEMT on Diamond

» [Assaad El Helou](#)¹, Marko Tadjer², Karl Hobart², Peter Raad¹ (1. Southern Methodist University, 2. Naval Research Laboratory)

P72 - Specific aspects regarding evaluation of power cycling tests with SiC devices

» [Martina Gerlach](#)¹, Peter Seidel¹, Josef Lutz² (1. Technische Universität Chemnitz, 2. Technische Universität Chemnit)

P74 - Gate Oxide Reliability Studies of Commercial 1.2 kV SiC Power MOSFETs

» [Tianshi Liu](#)¹, Shengnan Zhu¹, Susanna Yu¹, Diang Xing¹, Arash Salemi¹, Minseok Kang¹, Kristen Booth¹, Marvin White¹, Anant Agarwal¹ (1. The Ohio State University)

P76 - Thermomechanical behaviour of inverse diode in SiC MOSFETs under surge current stress

» [Shanmuganathan Palanisamy](#)¹, Roman Boldyrjew¹, Thomas Basler², Josef Lutz³ (1. Technische Universität Chemnitz, 2. Infineon Technologies AG, 3. Technische Universität Chemnit)

P77 - Analysis of Transient HTRB Leakage in a SiC Field Ring Termination

» [Rahul Potera](#)¹, Tony Witt¹, Yongju Zheng¹ (1. SemiQ Inc.)

P78 - Fast Neutron Irradiation Effects on Multiple Gallium Nitride (GaN) Device Reliability in Presence of Ambient Variations

» [Luis Soriano](#)¹, Hector Valencia¹, Ronald Nelson², Ke-Xun Sun¹ (1. University of Nevada, Las Vegas, 2. Los Alamos National Laboratory)

P79 - Enhanced Threshold Voltage Stability in ZnO Thin-Film-Transistors by Excess Oxygen in Atomic Layer Deposited Al₂O₃

» Rodolfo A. Rodriguez-Davila¹, Richard A. Chapman¹, Massimo Catalano¹, Manuel Quevedo-Lopez¹, [Chadwin Young](#)¹ (1. University of Texas at Dallas)

P80 - Reliability and Robustness Performance of 1200 V SiC DMOSFETs

» [Siddarth Sundaresan](#)¹, Vamsi Mulpuri¹, Jaehoon Park¹, Ranbir Singh¹ (1. GeneSiC Semiconductor)

P81 - Substrate Bias Effect on Dynamic Characteristics of Monolithic Integration GaN Half-Bridge

» [Wen Yang](#)¹, Jiann-Shiun Yuan¹, Balakrishnan Krishnan², An-Jye Tzou³, Wen-Kuan Yeh³ (1. University of Central Florida, 2. BRIDG, 3. Taiwan semiconductor research institutue)

P82 - ESD Robustness of GaN-on-Si Power Devices under Substrate Biases by means of TLP/VFTLP Tests

» [Wen Yang](#)¹, Nicholas Stoll¹, Jiann-Shiun Yuan¹ (1. University of Central Florida)



Continued from **Wednesday, 1 April**

P83 - Threshold Voltage Instability of Commercial 1.2 kV SiC Power MOSFETs

» [Susanna Yu](#)¹, [Minseok Kang](#)¹, [Tianshi Liu](#)¹, [Shengnan Zhu](#)¹, [Diang Xing](#)¹, [Arash Salemi](#)¹, [Kristen Booth](#)¹, [Marvin White](#)¹, [Anant Agarwal](#)¹ (1. The ohio state University)

P84 - Reliability of 200mm E-mode GaN-on-Si Power HEMTs

» [David Zhou](#)¹ (1. Innoscience Technology)

P85 - Design Optimization of MV-NMOS for ESD Self-protection in 28nm CMOS technology

» [Kyeongjin Hwang](#)¹, [Sagarpremnath Karalkar](#)¹, [Vishal Ganesan](#)¹, [Sevashanmugam Marimuthu](#)¹, [Alban Zaka](#)¹, [Tom Herrmann](#)², [Bhoopendra Singh](#)¹, [Robert Gauthier jr](#)¹ (1. GLOBALFOUNDRIES, 2. GI)

P86 - Triggering Optimization on NAND ESD Clamp and Its ESD Protection IO Scheme for CMOS Designs

» [Jian Liu](#)¹, [Divya Acharya](#)¹, [Nathaniel Peachey](#)¹ (1. Qorvo Inc.)

P87 - A Method to Analyze Aging Effect on ESD Protection Design

» [Kuo-Hsuan Meng](#)¹ (1. NXP Semiconductors)

P88 - Understanding ESD Induced Thermal Mechanism in FinFETs Through Predictive TCAD Simulation

» [Zhiqing Li](#)¹, [Baofu Zhu](#)¹, [Anindya Nath](#)¹, [Meng Miao](#)¹, [Alain Loiseau](#)¹, [You Li](#)¹, [Jeffrey Johnson](#)¹, [Souvick Mitra](#)¹, [Robert Gauthier jr](#)¹ (1. GLOBALFOUNDRIES)

Thursday, 2 April

7am

Breakfast

Texas Grande

8am

8A Gate/MOL Dielectrics

Texas Grande

8A.1 - The Mysterious Bipolar Bias Temperature Stress from the Perspective of Gate-Sided Hydrogen Release

» [Tibor Grasser](#)¹, [Ben Kaczer](#)², [Barry O'Sullivan](#)², [Gerhard Rzepa](#)³, [Bernhard Stampfer](#)¹, [Michael Waltl](#)¹ (1. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria, 2. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 3. Global TCAD Solutions)

8A.2 - Conduction and Breakdown Mechanisms in Low-k Spacer and Nitride Spacer Dielectric Stacks in Middle of Line Interconnects

» [Chen Wu](#)¹, [Adrian Chasin](#)¹, [Steven Demuynck](#)¹, [Naoto Horiguchi](#)¹, [Kristof Croes](#)¹ (1. IMEC, Kapeldreef 75, B-3001 Leuven)

8A.3 - Generation of Hot-Carrier Induced Border and Interface Traps, Investigated by Spectroscopic Charge Pumping

» [Bernhard Ruch](#)¹, [Gregor Pobegen](#)¹, [Christian Schleich](#)², [Tibor Grasser](#)² (1. KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Europastr. 8, 9524 Villach, Austria, 2. Institute for Microelectronics, TU Wien, Gußhausstr. 27-29, 1040 Vienna, Austria)

8A.4 - Reliability and Breakdown Study of Erase Gate Oxide in Split-Gate Non-Volatile Memory Device

» [Luo Laiqiang](#)¹, [Shubhakar Kalva](#)², [Sen Mei](#)², [Nagarajan Raghavan](#)², [Fan Zhang](#)¹, [Danny Shum](#)¹, [Kin Leong Pey](#)² (1. GLOBALFOUNDRIES, 2. Singapore University of Technology and Design)

8A.5 - Correlation of Dielectric Breakdown and Nanoscale Adhesion in SiO2 Thin Films

» [Alok Ranjan](#)¹, [Sean O'Shea](#)², [Michel Bosman](#)³, [Joel Molina](#)⁴, [Nagarajan Raghavan](#)¹, [Kin Leong Pey](#)¹ (1. Singapore University of Technology and Design, 2. Institute of Materials Research and Engineering, 3. National University of Singapore, 4. National Institute of Astrophysics, Optics and Electronics)

8am

8B - Neuromorphic Computing Reliability II

International I & II



Continued from Thursday, 2 April

8B.1 (Invited) - Embracing the Unreliability of Memory Devices for Neuromorphic Computing

» Marc Bocquet¹, Tifenn Hirtzlin², Jacques-Olivier Klein², Etienne Nowak³, Elisa Vianello³, Jean-Michel Portal¹, [Damien Querlioz](#)² (1. Aix-Marseille Université, CNRS, 2. Université Paris-Saclay, CNRS, 3. Université Grenoble-Alpes, CEA, LETI)

8B.2 - Impact of Read Disturb on Multilevel RRAM based Inference Engine: Experiments and Model Prediction

» [WONBO SHIM](#)¹, YANDONG LUO¹, JAE-SUN SEO², Shimeng Yu¹ (1. Georgia Tech, 2. Arizona State University)

8B.3 - Circuit Reliability Analysis of RRAM-based Logic-in-Memory Crossbar Architectures Including Line Parasitic Effects, Variability, and Random Telegraph Noise

» [Tommaso Zanotti](#)¹, Francesco Maria Puglisi¹, Paolo Pavan¹ (1. University of Modena and Reggio Emilia)

8B.4 - Breakdown Lifetime Analysis of HfO₂-based Ferroelectric Tunnel Junction (FTJ) Memory for In-Memory Reinforcement Learning

» [Marina Yamaguchi](#)¹, Shosuke Fujii¹, Kensuke Ota¹, Masumi Saitoh¹ (1. Kioxia Corporation)

8B.5 (Invited) - Neuromorphic Computing with Phase Change, Device Reliability, and Variability Challenges

» [Charles Mackin](#)¹, Pritish Narayanan¹, Stefano Ambrogio¹, Hsinyu Tsai¹, Katie Spoon¹, Andrea Fasoli¹, An Chen¹, Alexander Friz¹, Robert Shelby¹, Geoffrey Burr¹ (1. IBM Research)

8D.1 - Silicon Reliability Characterization of Intel's Foveros 3D Integration Technology for Logic-on-Logic Die Stacking

» [Chetan Prasad](#)¹, Emre Armagan², Peng Bai³, Sunny Chugh¹, Hannes Greve¹, Lance Hibbeler⁴, I-Chen Ho¹, Doug Ingerly³, Enamul Kabir¹, Cheyun Lin¹, Mahjabin Maksud¹, Steven Novak¹, Michael O'Day⁴, Benjamin Orr¹, Daniel Pantuso⁴, Keun Woo Park¹, Anthony Schmitz¹, Patrick Stover⁵, Hsinwei Wu², Zhizheng Zhang¹ (1. Logic Technology Development Quality and Reliability, Intel Corporation, 2. Assembly and Test Technology Development Quality and Reliability, Intel Corporation, 3. Logic Technology Development, Intel Corporation, 4. Technology Computer Aided Design, Logic Technology Development, Intel Corporation, 5. Assembly and Test Technology Development, Intel Corporation)

8D.3 - Effects of UBM Thickness and Current Flow Configuration on Electromigration Failure Mechanisms in Solder Interconnects

» [Yi Ram Kim](#)¹, Allison Osmanson¹, Hossein Madanipour¹, Choong-Un Kim¹, Patrick Thompson², Qiao Chen² (1. University of Texas at Arlington, 2. Texas Instruments, Inc.)

8D.4 - Efficient Bidirectional protection structure for Plasma induced damage (PID) and Electrostatic discharge (ESD) for 3D IC Integration

» [CS \(Prem\) Premachandran](#)¹, Salvatore Cimino¹, Manjunatha Prabhu¹ (1. GLOBALFOUNDRIES)

8am

8C - Soft Error

International III & IV

8C.1 - Investigating of SER in 28 nm FDSOI-Planar Technology and Comparing with SER in Bulk-FinFET Technology

» [Taiki Uemura](#)¹, Byungjin Chung¹, Jeongmin Jo¹, Hai Jiang¹, Yongsung Ji¹, Tae-Young Jeong¹, Rakesh Ranjan¹, Youngin Park¹, Kiil Hong¹, Seungbae Lee¹, Hwasung Rhee¹, Sangwoo Pae¹, Euncheol Lee¹, Jaehee Choi¹, Shota Ohnishi¹, Ken Machida¹ (1. SAMSUNG ELECTRONICS)

8am

8D - Packaging and 2.5/3D Assembly

Val Verde



Continued from Thursday, 2 April

8C.2 - Thermal Neutron Induced Soft Errors in 7-nm Bulk FinFET Node

» [Lyu Xu](#)¹, Jingchen Cao¹, John Brockman², Carlo Cazzaniga³, Christopher Frost³, Shi-Jie Wen⁴, Rita Fung⁴, [Bharat Bhuvu](#)¹ (1. vanderbilt university, 2. University of Missouri Research Reactor, 3. Rutherford Appleton Laboratory, 4. Cisco Systems)

8C.3 - Backside Alpha-Irradiation Test in Flip-Chip Package in EUV 7 nm FinFET SRAM

» [Taiki Uemura](#)¹, Byungjin Chung¹, Jeongmin Jo¹, Hai Jiang¹, Yongsung Ji¹, Tae-Young Jeong¹, Rakesh Ranjan¹, Seungbae Lee¹, Hwasung Rhee¹, Sangwoo Pae¹, Euncheol Lee¹, Jaehee Choi¹, Shota Ohnishi¹, Ken Machida¹ (1. SAMSUNG ELECTRONICS)

8C.4 - On the Correlation of Laser-induced and High-Energy Proton Beam-induced Single Event Latchup

» Norbert Seifert¹, Bahar Ajdari¹, Samwel Sekwao¹, [Ricardo Ascazubi](#)¹, Adam Neale¹ (1. Intel Corporation)

8C.5 - Impact of Hydrided and Non-Hydrided Materials Near Transistors on Neutron-Induced Single Event Upsets

» [Shinichiro Abe](#)¹, Tatsuhiko Sato¹, Junya Kuroda², Seiya Manabe², Yukinobu Watanabe², Wang LIAO³, Kojiro Ito⁴, Masanori Hashimoto⁴, Masahide Harada⁵, Kenichi Oikawa⁵, Yasuhiro Miyake⁶ (1. Japan Atomic Energy Agency, 2. Kyushu University, 3. Kochi University of Technology, 4. Osaka University, 5. J-PARC Center, 6. High Energy Accelerator Research Organization)

9A.1 - Advanced self-heating model and methodology for layout proximity effect in FinFET technology

» [Hai Jiang](#)¹, Hyun-Chul Sagong¹, Jinju Kim¹, Hyewon Shim¹, Yoohwan Kim¹, Junekyun Park¹, [Taiki Uemura](#)¹, Yongsung Ji¹, Tae-Young Jeong¹, Dongkyun Kwon¹, Hwasung Rhee¹, Sangwoo Pae¹, Brandon Lee¹ (1. SAMSUNG ELECTRONICS)

9A.2 - Effect of Drain-to-Source Voltage on Random Telegraph Noise Based on Statistical Analysis of MOSFETs with Various Gate Shapes

» [Ryo Akimoto](#)¹, Rihito Kuroda¹, Akinobu Teramoto², Takezo Mawaki¹, Shinya Ichino¹, Tomoyuki Suwa¹, Shigetoshi Sugawa¹ (1. Tohoku University, 2. Hiroshima University)

9A.3 - On the impact of mechanical stress on gate oxide trapping

» [Anastasiia Krav](#)¹, Ben Kaczer¹, Alexander Grill¹, Mario Gonzalez¹, Jacopo Franco¹, Dimitri Linten¹, Wolfgang Goes², Tibor Grasser³, Ingrid De Wolf¹ (1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 2. TU Wien, 3. Institute for Microelectronics, TU Wien, GuBhausstr. 27-29, 1040 Vienna, Austria)

9A.4 - NBTI Impact of Surface Orientation in Stacked Gate-All-Around Nanosheet Transistor

» [Huimei Zhou](#)¹, Miaomiao Wang¹, Jingyun Zhang¹, Koji Watanabe¹, Curtis Durfee¹, SHOGO MOCHIZUKI¹, Ruqiang Bao¹, Ricki Southwick¹, Maruf Bhuiyan¹, Basker Veeraraghavan¹ (1. IBM Research)

11:10am **9B - Memory Reliability II**
International I & II

9B.1 - eNVM RRAM reliability performance and modeling in 22FFL FinFET technology

» [Yao-Feng Chang](#)¹, James A. O'Donnell¹, Tony Acosta¹, Roza Kotlyar¹, Albert Chen¹, Pedro A Quintero¹, Nathan Strutt¹, Oleg Golonzka¹, Chris Connor¹, Jeffrey Hicks¹ (1. Intel Corporation)

10:20am **Break & Exhibits**
Texas Grande

11:10am **9A - Transistors II**
Texas Grande



Continued from Thursday, 2 April

9B.2 - Modeling of Charge Failure Mechanisms during the Short Term Retention Depending on Program/Erase Cycle Counts in 3-D NAND Flash Memories

» [Changbeom Woo](#)¹, Shinkeun Kim¹, Jaeyeol Park¹, Haesoo Kim², Gil-Bok Choi², Moon-Sik Seo², Keum Hwan Noh², Hyungcheol Shin¹ (1. Seoul National University, 2. SK hynix Inc.)

9B.3 - Write Disturb Mechanism in Embedded SuperFlash Technology

» [Clyde Dunn](#)¹, Alex Microchip² (1. Texas Instruments, 2. Microchip)

9B.4 - Further Investigation on Mechanism of Trap Level Modulation in Silicon Nitride Films by Fluorine Incorporation

» [Harumi Seki](#)¹, Yasushi Nakasaki¹, Yuichiro Mitani¹ (1. Kioxia Corporation)

11:10am **9D - IC Product Reliability II**
Val Verde

9D.1 - Comprehensive Quality and Reliability Management for Automotive Product

» [M. H. Hsieh](#)¹ (1. Mediatek.inc)

9D.2 - Advanced methods for CPU product reliability modeling and enhancement

» [Oren Zonensain](#)¹, Roman Rechter¹, Rob Kwasnick¹, Keun Woo Park¹, Anisur Rahman¹, Almog Reshef¹, Tal Raz¹, Maxim Levit¹ (1. Intel Corporation)

9D.3 - A Reliability Overview of Intel's 10+ Logic Technology

» [Rohit Grover](#)¹, Tony Acosta¹, Craig AnDyke¹, Emre Armagan¹, Chris Auth¹, Sunny Chugh¹, Katherine Downes¹, Michael Hattendorf¹, Nathan Jack¹, Subhash Joshi¹, Rahim Kasim¹, Gerald Leatherman¹, Se-hoon Lee¹, Cheyun Lin², Atul Madhavan¹, Haijing Mao¹, Anthony Lowrie¹, Gregory Martin¹, Gray McPherson¹, Pinakpani Nayak¹, Adam Neale¹, David Nminibapiel¹, Benjamin Orr¹, James Palmer¹, Christopher Pelto¹, Steven Poon¹, Ian Post¹, Tanmoy Pramanik¹, Anisur Rahman¹, Stephen Ramey¹, Norbert Seifert¹, Kanika Sethi¹, Anthony Schmitz¹, Hsinwei Wu¹, Andrew Yeoh¹ (1. Intel Corporation, 2. Intel)

11:10am **9C - Metallization/BEOL Reliability II**
International III & IV

9C.1 - Reliability on EUV Interconnect Technology for 7 nm and beyond

» [Tae-Young Jeong](#)¹, Miji Lee¹, Yunkyung Jo¹, Jinwoo Kim¹, Min Kim¹, Myungsoo Yeo¹, Jinseok Kim¹, Hyunjun Choi¹, Joosung Kim¹, Yoojin Jo¹, Yongsung Ji¹, Taiki Uemura¹, Hai Jiang¹, Dongkyun Kwon¹, Hwasung Rhee¹, Sangwoo Pae¹, Brandon Lee¹ (1. SAMSUNG ELECTRONICS)

9C.2 - Metal reliability mechanisms in Ruthenium interconnects

» [Olalla Varela Pedreira](#)¹, Michele Stucchi¹, Anshul Gupta¹, Victor Vega Gonzalez¹, Marleen van der Veen¹, Stephane Lariviere¹, Christopher J. Wilson¹, Zsolt Tokei¹, Kristof Croes² (1. IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, 2. IMEC, Kapeldreef 75, B-3001 Leuven)

9C.3 - Reliability of Metal-Dielectric Structures Under Intermittent Current Pulsing

» [Chung-Shuo Lee](#)¹, Pavan Kumar Vaitheeswaran¹, Ganesh Subbarayan¹, Young-Joon Park², Jayhoon Chung², Srikanth Krishnan² (1. Purdue University, 2. Texas Instruments)

1:05pm **Break & Exhibits**
Texas Grande

1:15pm **IRPS Closing & 2021 Introduction**
Texas Grande



Continued from **Thursday, 2 April**

1:25pm **Lunch**
Vineyard

Tuesday, 28 April

8am **Welcome & Introduction**



Plenary Keynote-I

Dr. Mike Mayberry - Intel

Title: The Future of Compute: Reliability and Resiliency in the era of Data Transformation

Abstract: The digital transformation continues to gain momentum and is changing the shape of business, industry and consumers around the world. This transformation is characterized by continued strong demand for compute at all points in the network – at the core, the edge, and at the endpoints. Data continues to grow at an exponential rate and not only drives the compute requirements, but also requires efficient solutions for movement and storage of data that is critical for overall performance. From device to cloud, new applications and use cases are continuously emerging. This transformation demands that we adapt our thinking and move from a hardware/program centric to a data/information centric approach, and to embrace new ways to compute. To keep pace in this dynamic environment, Moore's Law and its impact have become more relevant than ever. The continued dimensional, materials and device scaling drives a renewed focus on the fundamental reliability physics of devices and materials, while novel architecture integration schemes and large-scale system design innovation motivates a more comprehensive understanding of resiliency at all levels of the system.

Biography:

Dr. Michael (Mike) C. Mayberry is the chief technology officer at Intel Corporation. He is a senior vice president and general manager of Technology Development, where he is responsible for the research, development and deployment of next-generation silicon logic, packaging and test technologies that will produce future Intel products.

Since joining Intel in 1984 as a process integration engineer, Mayberry has held a variety of positions. As part of the California Technology Development team, he developed EPROM, flash and logic wafer fabrication processes. In 1994, he moved to Sort Test Technology Development, responsible for roadmaps and development of test processes for Intel microprocessors. In 2005, he moved to Components Research and was responsible for research to enable future process options for Intel's technology development organizations. In 2015, he moved to Intel Labs and became responsible for Intel's product-driven research. In 2018, he moved to the Technology Development group at Intel.

Mayberry received his bachelor's degree in chemistry and mathematics from Midland College and his Ph.D. in physical chemistry from the University of California, Berkeley.



Plenary Keynote-II

Dr. Oliver Häberlen - Infineon Technologies Austria AG

Title: Power Semiconductor Reliability – An Industry Perspective on Status and Challenges

Abstract: Power transistors are an inevitable key component of nearly every power electronic system enabling the path to a greener environment through increased conversion efficiency. Silicon based power transistors are established on the market since more than half a century and the reliability and quality of those devices has matured to failure levels in the sub ppm range. The base for this achievement was a deep understanding of all the failure modes and their corresponding lifetime models.

The new wide band gap power semiconductor materials SiC and GaN that have entered the market during the past respective this decade are on much earlier points along a similar learning curve. It will be shown that the methodology how to qualify a power semiconductor technology remains essentially unchanged for the new devices, but of course all the new material and device specific failure modes need to be understood and modelled. The most important past learnings will be shown in this talk.

So everything is solved for the established silicon technologies? Also here we face new challenges due to the ever continuing pressure for cheaper devices mostly addressed by device shrinks. Pushing the devices closer and closer to their physical limits of course also requires refining and improving the established models in order to tailor the exactly right amount of safety margin. Additionally increasing power and current densities on die level require new package concepts leading to potential new failure modes.

Finally, we will conclude with some examples on a general trend observed: Fitting the devices as good as possible to the target applications and their respective requirements is leading to the need for an increased focus on application reliability testing.

Biography:

Dr. Oliver Häberlen received his M.S. and Ph.D. degree in physics from the University of Munich and Technical University of Munich respectively.

He is currently employed with Infineon Technologies Austria AG as a Senior Principal for Power Transistor Technology and heading the group for advanced technology concepts evaluating future silicon and wide band gap (SiC, GaN) power device concepts for improved energy conversion solutions. His research areas include low and medium voltage trench power MOSFETs, high voltage super junction devices, GaN power devices and power device reliability.

He is a senior member of IEEE and member of the IEEE EDS Power Devices and ICs Technical Committee. He also served as Technical Committee member for IEDM (International Electron Devices Meeting) and ISPSD (International Symposium on Power Semiconductor Devices and ICs) and is the General Chair of the ISPSD conference in 2020. He is author and co-author of over 100 international patents and patent applications in the field of power semiconductors.



Dr. Gianluca Boselli - Texas Instruments

Title: Power scalability challenges in High-Voltage ESD Design

Abstract: The criticality of Analog Technologies has significantly increased over the last decade, due to the phenomenal success of portable consumer electronics, which require multiple analog functions to be implemented in the same chip. The relatively recent push towards society “electrification” (electric cars, smart power grids, IoT) is driving the need for higher and higher voltage applications together with a plethora of functional and safety requirements, which pose significant challenges in terms of ESD Design. This paper discusses these challenges, with special emphasis on the perspective of power scalability.

Biography:

Gianluca Boselli completed his master’s in EE at the University of Parma, Italy, in 1996. In 2001, he completed his PhD at the University of Twente, The Netherlands; where he worked on high current phenomena in CMOS technologies. In 2001, he joined Texas Instruments, Inc., Dallas, Texas; where he focused on ESD and latch-up development for advanced CMOS technologies, with particular emphasis on process and modeling aspects. In 2007, his responsibilities extended into ESD development of Texas Instruments’ analog technologies portfolio. He is currently managing both ESD and Spice Modeling Teams.

He authored several papers in the area of ESD and latch-up. He presented his work at major conferences, including EOS/ESD Symposium, IEDM, and IRPS. He has also presented many invited tutorials and papers at various conferences, including EOS/ESD Symposium, IRPS, IEDM, ESREF, IEW, and RCJ.

Dr. Boselli has been the recipient of the best paper award on behalf of Microelectronics Reliability Journal in 2000. He received the best paper award at the EOS/ESD Symposium 2002. He also received the Outstanding Symposium award at the EOS/ESD Symposium in 2002, 2006, and 2010.

Dr. Boselli served multiple times as sub-committee chair for technical program committees (TPC) of EOS/ESD Symposium, IEDM, IRPS, IEW, and ESREF. He served as moderator and panelist in many workshops in ESD and latch-up area.

Dr. Boselli has served as TPC chair at the EOS/ESD Symposium 2006, vice-general chair at the EOS/ESD Symposium 2007, and general chair at the EOS/ESD Symposium 2008.

He is currently a member of the board of directors of EOS/ESD Association, Inc

Dr. Boselli is an IEEE senior member and holds over twenty patents with several pending.

Dr. Boselli serves in the editorial board of the IEEE Transactions on Device and Materials Reliability (T-DMR).

YA1 (IRPS YIR) - Main Review

Authors

James Tschanz - Intel Corporation

Abstract

TBD

BIO

YA2 (IRPS YIR) - EDA Aspects

Authors

Georgios Konstadinidis – Google

Abstract

Achieving high level of performance, time to market and high quality as required by automotive, mission critical and cloud computing applications demands accurate analysis scalable to the billion devices in today's chips. In this EDA focused YIR session of Circuit Reliability we will review papers that cover compact reliability models that take into account recovery effects, self-heating, workload, process, voltage and temperature variations, and also combine accuracy and scalability based on a hierarchical analysis approach. The workload choice to get good coverage is tricky, and ML methods are being employed to help with this problem. These however require training and in situ measurements are used to form the baseline training set. This knowledge can be used to make changes in the microArchitecture to minimize the chip wearout by proper load balancing and more uniform wearout. This session will review some key papers that cover this complex task and help define the future direction of the EDA circuit reliability analysis.

BIO

Georgios K. Konstadinidis is a Technology and Chip Implementation Lead at Google focusing on the R&D of Machine Learning Accelerators. He received a Ph.D degree in electrical engineering from the Technical University of Berlin, Germany and a B.Sc. Degree in Physics, M.Sc. in electronics from the Aristoteles University Thessaloniki Greece. From 2010 to 2017 he was a Senior Hardware Architect at Oracle and prior to that a Distinguished Engineer at Sun Microsystems, focused on high performance microprocessor physical design. He has been involved in the technology, design porting, physical design, reliability, optimization, circuit methodology, signal integrity, timing, and CAD tools for several projects. From 1991 to 1995 he was the leader of the high performance bipolar ICs design team at the R&D Center of SGS Thomson in England and in Catania, Italy. He was involved in the design of several ICs for telecommunications, in device modeling and process optimization.

Dr. Konstadinidis holds 13 patents and has several IEEE publications. He served as a member of the ISSCC Digital Program Committee from 2002 to 2007, and as Guest Editor for the IEEE Journal of Solid State Circuits. He is a co-author of the book "Clocking in Modern VLSI Systems", Springer, 2009. He currently serving as TPC member of the IRPS Digital Circuit Reliability sub-committee and IEDM Systems & Circuit Reliability

YA3 (IRPS YIR) - Si and SiGe Reliability

Author



Fernando Guarín - GLOBALFOUNDRIES

Abstract

In 2019 the world was getting ready for the unstoppable transition from 4G to 5G. There was a large amount of activity throughout the year in the area of Si/SiGe (CMOS/Bi-CMOS). Academia, RF companies and semiconductor foundries were very active developing and refining the best suited technologies capable of meeting the stringent requirements needed for RF/mmW 5G solutions. Most key players realize that there is a sizable opportunity for Si and SiGe technology solutions as we transition from the few antennas required in 4G to the multi element antenna array solutions incorporating “Massive MIMO” (Multiple Input Multiple Output) the power requirements have been reduced to a range that is well suited for Silicon and Silicon Germanium technology offerings. To be competitive in this arena RF circuit designers must try to squeeze every bit of performance from the technologies that they are using in their designs. Reliability gates the maximum amount of power/performance that can be safely achieved in a given technology. We will summarize the most significant papers of 2019 dealing with the achievements and reliability of Si and SiGe in this mmW/5G year in review session.

BIO

Dr. Fernando Guarín is a Distinguished Member of Technical Staff at Global Foundries in East Fishkill New York where he is currently leading the reliability team involved in the qualification of GlobalFoundries 5G mmW technology offerings, particularly 45RFSOI. From 1980 until 1988 he worked in the Military and Aerospace Operations division of National Semiconductor Corporation. In 1988 he joined IBM’s microelectronics division where he worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies. He retired from the IBM Semiconductor Research Development Center SRDC in 2016 after 27 years with the reliability group where he was a

Senior Member of Technical Staff. He earned his BSEE from the “Pontificia Universidad Javeriana”, in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University, NY. He has been actively working in semiconductor reliability for over 38 years. He has authored 15 patents, one trade secret, five book chapters and over 2000 citation for his publications. Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Device Society EDS, where he has served in many capacities including; member of the IEEE’s EDS Board of governors, chair of the EDS Education Committee, Secretary for EDS. He was the EDS President 2018-2019 and is currently the Jr. Past president of EDS.

YA5 (IRPS YIR) - Memory

Authors

Chandra Mouli - Micron

Abstract

I will present highlights from key recent papers specifically focused on reliability topics. Evolutionary memory technologies will be covered along with few papers from Emerging Memory areas. Since memory systems are increasingly becoming complex, there is significant focus in the community to understand not only component-level reliability challenges but at the system and product-levels as well. Therefore, I will focus on couple of key papers in these areas in addition to those at the device-level.

BIO

Chandra Mouli is with Micron Technology Inc., Boise, ID, USA. He is currently Senior Director of Device Technology with responsibilities in the areas of advanced CMOS logic technology for memory products, device characterization, reliability analysis, compact models, test structure design, process & device modeling for all technologies under development in R&D. He received his undergraduate degree in Physics and MSEE from the Indian Institute of Science (IISc), Bangalore, India and Ph.D (EE) from the University of Texas at Austin. He was with Texas Instruments for couple of years before joining UT/Austin. His interests include semiconductor devices and process technology for advanced memory, opto-electronic devices, exploratory research in the area of new materials and device structures. He has >200 issued patents and several pending in various areas of semiconductor devices and process – in advanced memory, novel devices and image sensor technology. He has served in the technical committees for various conferences, including IEDM, IRPS and SISPAD. He has also served in the review committees for NSF and SRC. He is currently an editor for IEEE Electron Device Letters (EDL).

YA4 (IRPS YIR) - Compound

Author



Enrico Zanoni - University of Padova

Abstract

TBD

BIO

YA6 (IEW/IRPS YIR) - ESD Industry Council Roadmap (I asked Gianluca for this)

Authors

Charvaka Duvvury - ESD Consulting

Abstract

TBD

BIO

TSB.1 (Tutorial) - Bias Temperature Instabilities: Best Practices for Reliability Benchmarking and Optimization Based on Recent Theoretical Insights

Authors

Jacopo Franco - imec

Abstract

In high-k/metal gate stacks, charge trapping in pre-existing oxide defects plays a crucial role in Bias Temperature Instabilities and complicates reliability benchmarking and gate stack optimization. In the first part of the tutorial, we will review the Non-Radiative Multi-Phonon theory, which has been shown to accurately describe the charge trapping kinetics, discussing the practical implications of the microscopic physics. Based on these theoretical insights, we will then review a range of BTI extrapolation methodologies, from the simplest and most commonly used empirical power-law approach, to a variety of semi-empirical/semi-physical models with increasing complexity and accuracy, ending with a quick review of the imec-T.U. Wien BTI modeling framework Comphy designed to maximize the modelling accuracy/complexity ratio.

In the second part, we will discuss practical BTI case studies in a variety of advanced technologies, including finFET and nanowire architectures, SiGe, Ge and III-V channels, sequential 3D-stacked transistors, back-gated fully-depleted SOI, and junctionless transistors, focusing on BTI benchmarking and gate stack optimization practices. Finally, we will discuss how the charging of individual oxide defects induces time-dependent variability in nanoscale devices, which can be statistically projected from the BTI characterization of large area test structures.

TSB.2 (Tutorial) - Self-heating: Assessment Methodologies, Impact on Reliability and Prospects for Future Technology Solutions

Authors

Erik Bury - imec

Abstract

In modern VLSI devices, multiple degradation mechanisms dictate limits of the acceptable bias conditions to guarantee reliable operation for extended times. Reliability qualification of a technology typically focusses on the usual degradation mechanisms, such as Bias Temperature instabilities (BTI), Hot-Carrier Degradation (HCD) or Time-Dependent-Dielectric-Breakdown (TDDB), each occurring in specific operating regimes of the MOSFET, determined by the gate (VG) and drain (VD) bias conditions. However, the thermal aspects during both testing and operation are becoming more important in technology nodes with confined channels such as FinFETs, fully-depleted SOI and Gate-all-around nanowire (GAA-NW) devices, and thus needs to be taken into account in the reliability measurements and projections.

In this tutorial, we will discuss the thermal aspects of FEOL degradation mechanisms. Dedicated methodologies for device-level DC and AC self-heating evaluation will be discussed and applied to contemporary and future device architectures and materials (such as high-mobility GAA-NW). Also the relevance of device-level thermal simulations, utilizing either classical Fourier or Boltzmann-Transport Equation for phonons will be discussed.

Finally, we will show how the active degradation mechanisms in the bias space can be deconvoluted and the safe-operating area for an anticipated lifetime quantified, while accounting for self-heating effects. Guidelines for thermal-aware test-structure design and overstress measurements will be also provided.

Bio

Erik Bury received the B.Sc., M.Sc. and PhD degrees in Electronic Engineering from the Katholieke Universiteit Leuven - Belgium, in 2009, 2011 and 2016 respectively. He is currently full-time researcher in the device characterization and reliability group of imec. His main research interests involve device self-heating effects, channel hot carrier degradation and bias temperature instabilities. He received the IPFA Best Paper award (in reliability) in 2014 and is serving or served as a technical program committee member for ESSDERC, IPFA and IRPS.

TSB.3 (Tutorial) - Electromigration: Physics, Rule, Validation, and Relaxation

Authors

Young-Joon Park - Texas Instruments

Abstract

This tutorial reviews the overall aspects of electromigration (EM), including physics, rule, design validation, and layout-sensitive EM check methods. The process impact on the EM performance is not the main focus of this presentation. The contents are not limited to advanced Cu interconnects, but also include conventional Al interconnects, which are still the main stream in analog applications, especially in power devices. The layout-sensitive EM check part explains the via node vector EM interaction, local current crowding impact on EM, and multi-finger impact on EM, which will help to maximize the entitlement for advanced interconnect designs.

Bio

Young-Joon joined Texas Instruments (TI) in 2002 and has worked in numerous semiconductor technology nodes for both digital and analog applications. He has researched back end of line (BEOL) reliability, especially focusing on the electromigration reliability. Since 2011, Young-Joon has been TI's Distinguished Member of the Technical Staff (DMTS). Prior to TI, he had carried out comprehensive researches on the BEOL semiconductor process and reliability, microstructure and fabrication of bulk and thin films, laser processing of hard films, and simulations of electromigration reliability in Korea Institute of Science and Technology (KIST) and Massachusetts Institute of Technology (MIT).

TSB.4 (Tutorial) - An Introduction to RF and Mixed-Signal Circuit Reliability

Authors

Vijay Reddy - Texas Instruments

Abstract

An introduction is provided to some of the reliability challenges encountered during the design of radio frequency (RF) and mixed-signal circuits. RF circuits can operate at voltages greater than twice the nominal supply voltage and thus hot-carrier and off-state aging are key considerations. Examples are given involving RF oscillators and power amplifier circuits along with a demonstration of an RF reliability FOM circuit. Mixed-signal circuits also present a reliability challenge due to their stringent matching and offset requirements and the aging impact on switch linearity, current mirror mismatch, and op-amp voltage offset is demonstrated. The impact of transient charge trapping on circuits such as SAR ADCs is also illustrated. The reliability issues present in power management circuits such as DCDC converters and LDOs along with the potential of bias runaway issue are also presented.

Bio

Vijay Reddy is currently a Distinguished Member Technical Staff in Texas Instruments' Analog Technology Development organization. He has worked on several topics concerning transistor, circuit reliability and product qualification methodologies for analog, digital, and RF products. He has served on the IRPS/IEDM program committees and has presented papers at IRPS/IEDM and invited tutorials at IRPS/ICTMS/VLSI Test. Symposium. He has received IRPS Outstanding Paper Awards and the ESD/EOS Symposium Best Paper/Best Presentation Awards. He has received nineteen patents with several pending along with more than thirty publications.

TSA.1 (Tutorial) - Terrestrial Radiation and Its Impact on the Reliability Performance of Microelectronics

Authors

Robert Baumann - Radiosity Solutions LLC & Southern Methodist University

Abstract

With the new focus on autonomous vehicles and Internet-of-Things (power, transportation and traffic infrastructure, etc.) ensuring high-reliability operation of microelectronics is critical for ensuring safety. With few exceptions, radiation-induced failures in qualified microelectronics typically occur at higher levels than all other "hard" reliability failure mechanisms combined. As motivation, we commence with a couple of real-world examples where random sub-atomic events induced human-scale reliability failures. We then examine the terrestrial environment, dominated by cosmic-ray high-energy and thermal neutrons, and by alpha-particles from trace impurities in manufacturing processes and materials. We look at how radiation impacts microelectronics by creating Single-Event Effects (including soft errors) that can induce transient and permanent reliability failures in microelectronics and conclude with a brief discussion of real-time and accelerated testing methods to determine failure rates and mechanisms.

Bio

Robert earned his Ph.D. in ECE from Rice U. He joined Texas Instruments in 1989 working on transistor and soft error reliability. He moved to Japan in 1993 to work on DRAM/CPU reliability and created a failure analysis team providing solutions for production-stop issues. From 1998 Robert drove company radiation effects and modeling activities, interacting regularly with major customers. He joined the High-Reliability Product group in 2012 improving radiation effects characterization, modeling, and developing new aerospace products. After retiring from TI in 2018, Robert is now a technology consultant (Radiosity Solutions) and research professor at SMU. He is an IEEE Fellow, has coauthored more than 90 papers, 1 book, 2 chapters, and 16 patents.

TSA.2 (Tutorial) - Plasma-induced Damage-modeling, Characterizations, and Design Methodologies

Authors

Koji Eriguchi - Kyoto University

Abstract

The increasing demand for higher performance of ULSI circuits requires aggressive shrinkage of device feature sizes in accordance with the scaling law. Plasma processing plays an important role in manufacturing advanced MOSFETs. This lecture will discuss the negative aspects of plasma processing, i.e., plasma process-induced damage (PID). During the last three decades, tremendous efforts have been devoted to clarify the mechanisms and effects of PID on MOSFETs. Firstly, an overview of three fundamental mechanisms of PID—charging damage, radiation damage, and physical damage—will be provided, in terms of modeling, characterization techniques, and experimental evidence reported so far. In particular, the effects of charging damage on the performance and reliability degradation of MOSFETs will briefly be reviewed so that tutorial attendees can understand the representative and principal mechanisms of PID extensively studied in the device reliability field. Then, this lecture will focus on physical damage, i.e., one of the emerging topics in ultimately scaled MOSFET regimes such as FinFETs and atomic layer etching technologies. The damage monitoring and characterization methods will also be presented to manage the productivity of device fabrications. Finally, device and process design methodologies for controlling PID (e.g. design rule, recovery, optimization, etc.) will be discussed as future perspectives.

Bio

Koji Eriguchi has been a professor of Kyoto University since 2016 after joining Kyoto University in 2005, working on plasma–solid surface interaction, optical characterization techniques of Si surfaces, and the modeling of plasma process-induced damage (PID) and the related defect creation in crystalline Si substrates and dielectric films, particularly, the degradation of materials and devices in harsh environments. Prior to joining Kyoto University, he had been a senior engineer at Panasonic from 1991 responsible for the research of plasma etch processes, thin gate dielectric wear-out phenomena under electrical stress and plasma irradiation (charging), CMOS process integration, and reliability of electronic devices. He has published more than 100 journal papers and delivered many invited talks at major international conferences. He received the Best Paper Award from the 32nd Dry Process Symposium in 2009, the APEX/JJAP Paper Award, the Plasma-Electronics Award from the Japan Society of Applied Physics (JSAP) in 2010, and 2015 Dry Process Symposium, Paper Award.

TSA.3 (Tutorial) - SONOS or Charge Trap Memories

Authors

Krishnaswamy Ramkumar - Cypress Semiconductor

Abstract

Silicon Nitride based charge trap (CT) devices have been studied for more than four decades for applications in non-volatile memories. Although the initial studies were reported on devices with metal gate, the Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) stack as the non-volatile memory gate stack has been the focus since the 1990s. Several enhancements in SONOS layer materials have been invented to reduce the programming voltage and improve the reliability of the SONOS memory cell. Some of the key enhancements include band gap engineered SONOS (BE-SONOS) stack and scaling down of layer thicknesses without sacrificing uniformity. With these enhancements, SONOS memories which can be programmed at voltages as low as 7.5V and can meet the 10 year retention at 100°C ambient temperature are now commercially available. With the advent of high K – metal gate technology for CMOS transistors, it was logical that high K dielectrics would be evaluated for the charge trap layer or blocking layer of the SONOS stack. The same is true for FinFETs which has led to research on SONOS based FinFETs. Furthermore, with the advent of 3D non-volatile memories, SONOS devices have been invented for 3D memory cells and these are now in manufacturing. SONOS has also been very successful in embedded memories where the cost of integration into an existing CMOS baseline process is most critical. Here the embedded SONOS has proven to be much more economical than the traditional Floating Gate technology for many applications. SONOS memory, which is also referred to as Charge Trap memory, is now being evaluated for analog multi-level memories for in-memory computing in AI edge applications.

While the ONO stack has been the CT memory stack of choice for all these years, new materials are now being explored and developed for the memory stack to improve the performance and reliability. All the layers of a CT stack, namely, tunneling oxide, trapping nitride and blocking oxide can be replaced by other dielectric materials. While there many dielectric material options, novel metal oxides such as high K dielectrics are strong candidates for all the layers. The availability of novel deposition tools and processes has enabled many studies on CT stacks with metal oxides. Widely studied oxides for the different layers of the CT stack are Al₂O₃, HfO₂ and HfAlON.

This tutorial will highlight the various innovations that have enhanced SONOS memory performance, reliability and low cost of manufacture. Topics that will be covered include various improvements in the ONO stack such as Band gap engineering, High K – Metal Gate for SONOS, 3D SONOS, SONOS FinFETs and embedded SONOS. The key features of the various CT memory stacks containing metal oxides and their dependence on material characteristics are also discussed

Bio

Current Title: VP Fellow at Cypress Semiconductor

Educational Background: Ph.D in Electrical Engineering, Indian Institute of Science, Bangalore, India

Professional Career Background

1993 to date: Process / Technology Development Engineer at Cypress Semiconductor, San Jose, engaged in Process / Module / Integration development and transfer to volume manufacturing of many SRAM technology and SONOS technology generations

Since 2007 involved in licensing / transferring of SONOS process IP to foundries; defining and developing embedded SONOS into foundry process flow on 130nm, 65nm, 55nm, 40nm and 28nm technology nodes.

Prior experience: Visiting Research Associate at Rensselaer Polytechnic Institute; Faculty at Indian Institute of Science

Publications and Patents

Over 75 publications in reputed journals and conferences; Over 140 US patents

Books

One textbook on “Electronic Devices” published by Wiley Eastern Ltd (India) in 1992.

Chapter on “Material and Device Reliability in SONOS Memories” in the book “Charge-Trapping Non-Volatile Memories - Emerging Materials and Structures” published by Springer 2017

Chapter on “Charge Trapping NVMs with Metal Oxides in the Memory Stack” in the book “Metal oxides for Non-Volatile Memories: Materials, Technology and Applications” to be published by Elsevier

TSA.4 (Tutorial) - Basic Reliability Physics: Acceleration Models, Statistical Methods, and Defect Screening

Author

Mark Porter - Medtronic

Abstract

This tutorial will give students a basic understanding of the reliability discipline as it is practiced in the semiconductor industry. We will cover statistical methods of fitting reliability data and show how this is done using modern software tools. We will then move on to acceleration models, including a review of important semiconductor failure mechanisms. Finally, we will dive into the difference between infant mortality and wearout, and how these two types of failures need to be treated differently in order to achieve robust product performance.

Bio

Mark Porter received a BS in Physics from the University of New Hampshire, USA, and is currently a Senior Engineering Manager and Technical Fellow with the Medtronic Tempe Campus in Arizona. He leads a diverse team of scientists, engineers, and technicians with responsibility for ensuring the microelectronics systems used in Medtronic implantable medical devices meet the demanding reliability requirements of this important industry.

Mark is a member of IEEE and holds two certifications, as a Quality Engineer and a Reliability Engineer, from the American Society for Quality. He was a member of the Management Committee of the IEEE International Reliability Physics Symposium starting in 2008, and served as Technical Program Chair in 2017 and General Chair in 2019. Prior to joining Medtronic, Mark held positions at the Massachusetts Institute of Technology in Cambridge, Massachusetts, TRW Space Systems in Redondo Beach, California, and Motorola in Phoenix, Arizona.

TSC.3 (Tutorial) - Electronic Design Automation (EDA) Solutions for Latch-up Verification in CMOS and HV Technologies

Authors

Michael Khazhinsky - Silicon Labs

Abstract

The verification of latch-up protection networks in CMOS and HV technologies is a difficult challenge. There are several factors including increasing design and process complexity, higher-pin counts, wide operating voltage ranges, and the overall computational difficulties in dealing with large data sets. Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification. These checks are typically focused on layout topology. However electrical information for latch-up risk areas throughout the chip is not readily available. While DRC checks are still useful at early design stages, relying on conventional DRC latch-up checking exclusively, poses a significant risk of missing hidden latch-up pitfalls. Consequently, a fully automated latch-up rule checking approach analyzing electrical information is highly desired.

In this tutorial we will review the essential requirements of the latch-up electronic design automation (EDA) verification flow. Then an overview of existing latch-up EDA solutions across the industry will be given. We will introduce generic rules that can be used as basis for a typical latch-up EDA verification flow in CMOS and HV technologies. Finally, recommendations for future EDA tool development and standardization will be provided.

Bio

Michael G. Khazhinsky is currently a Principal ESD engineer/designer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he worked at Motorola and Freescale Semiconductors where he was in charge of the TCAD development and ESD/latch-up protection solutions for emerging process technologies, with a focus on ESD-EDA. Michael has M.S.E.E. and M.S. Physics from the Moscow State Institute of Electronic Engineering, and Ph.D. in Physics from Western Michigan University. Michael is the Chair of ESDA Working Group 18 on EDA. Michael has served as a member of the IRPS, IEW, ESREF, EMC and EOS/ESD Symposium Technical Program Committees, as well as a Workshop Chair, Technical Program Chair, Vice General Chair and General Chair of EOS/ESD Symposium. He currently serves on the Technical Program Committees of 2020 International Reliability Physics Symposium, 2020 International ESD Workshop, and 2020 EOS/ESD Symposium. Michael co-authored over 30 papers and gave a number of invited talks on ESD, EDA, process/device TCAD, and photonic crystals. He was a recipient of seven EOS/ESD Symposium and SOI Symposium “Best Paper” and “Best Presentation” awards as well as Industry Pioneer Recognition Award. Michael currently holds eighteen patents on ESD design, with additional patents pending. Michael is a Senior Member of IEEE and the Director of the ESD Association.

TSC.4 (Tutorial) - EOS, ESD, Transient, AMR, EIPD, Robustness, Aging —Do all of These Pieces go to the Same Puzzle?

Authors

Hans Kunz - Texas Instruments, Inc.

Abstract

TBD

TMA.1 (Tutorial) - The Role of Defects on Reliability Aspects in GaN Power Devices

Authors

Clemens Ostermaier - Infineon

Abstract

Gallium nitride (GaN) offers fundamental advantages over silicon. In particular the higher critical electrical field makes it very attractive for power semiconductor devices with outstanding specific dynamic on-state resistance and smaller capacitances compared to silicon switches, which makes GaN HEMTs great for high speed switching. However, defects in GaN epitaxial layers grown on silicon substrate have been a long standing topic going hand-in-hand with the understanding of reliability aspects of such devices.

After some introduction on device and material basics and the benefits of GaN devices in typical applications, this talk summarizes the current understanding of the most relevant defects in GaN power HEMTs:

Interface defects controlling the electron concentration in the device channel, the lateral 2-dimensional electron gas, and buffer defects required to establish a vertically insulating GaN buffer. The latter is typically achieved by introducing Carbon atoms during the buffer growth acting dominantly as acceptor-like defect states. Finally, the knowns and unknowns of the key reliability aspects, III-N TDDB and dynamic drift and lifetime effects, will be discussed in respect to those defects.

Bio

Clemens Ostermaier has received his master's degree in semiconductor engineering from Kyungpook National University in South Korea in 2008 and his doctoral degree in electrical engineering from Vienna University of Technology in 2011, where he rejoined in 2019 as university lecturer. Since 2010 he is working at Infineon Technologies Austria on GaN power devices with special interest and passion on the technology, design, and reliability aspects. He has supervised several Ph.D. and master students and co-authored over 30 peer-reviewed scientific journal publications, more than 50 conference contributions and over 20 international patent and patent applications in power semiconductors.

TMA.2 (Tutorial) - System-Focused Reliability of SiC MOSFETs

Authors

Mrinal Das - Texas Instruments

Abstract

Silicon carbide MOSFETs are becoming an accepted semiconductor device technology for advanced power conversion systems, supplanting existing Si IGBT/MOSFETs while also creating new semiconductor application areas. Fundamental studies of the gate and drain terminals have established the intrinsic reliability from a device perspective. However, the emerging focus is the stability of the device within the context of its usage in various systems. In this tutorial, we will review the device data in terms of historical time dependent dielectric breakdown and ramped high temperature reverse bias. This will be followed by a study of the challenges imposed by the applications valuing the SiC MOSFETs and subsequent progress made by the SiC industry. Notable system-focused areas to be covered are negative bias temperature instability of the gate, outdoor ruggedness against humidity under high drain voltage, susceptibility to cosmic ray induced failures, overshoots/undershoots driven by system parasitics, fault handling capability, stability of the body pn junction diode in lieu of external Schottky diodes, to name a few. The goal of the tutorial is to arm the device and system reliability audience with the current status and requirements of SiC MOSFETs thereby enabling them to drive the next generation of reliability breakthroughs.

Bio

Dr. Mrinal K. Das has enjoyed a professional career at the forefront of SiC power device technology. After completing electrical engineering and Plan II liberal arts dual honors at The University of Texas at Austin, he pursued graduate studies at Purdue University where his doctoral research involved the fundamental understanding of the SiC MOS structure to enable advanced power MOSFETs. In his first 13 years at Cree Inc., Dr. Das worked on the process and design development to enable the evolution of many SiC power devices. In his final 5 years at Cree, his focus shifted to marketing where he worked with customers and partners to catalyze market acceptance. With the SiC MOSFET rapidly becoming a mature and accepted technology in power electronics, Dr. Das has moved on to his current role as the SiC technology lead in Texas Instruments' Kilby Labs R&D where he is addressing the next phase of SiC MOSFET evolution—optimizing the surrounding eco-system. Dr. Das has authored 60+ publications, presented 12 invited seminars, and received 25+ US patents.

TMA.3 (Tutorial) - Testing for Wear and Abnormal Conditions of Power IGBT Modules

Authors

Francesco Iannuzzo - Aalborg University

Abstract

The tutorial introduces the modern principles of testing for the reliability of power IGBT modules, both against wear and abnormal conditions. After a short introduction about CORPE – the Center of Reliable Power Electronics at Aalborg University, where expectations from power electronics industries will be presented as well, some reliability theory fundamentals will be given, along with practical details about common testing protocols. Wear/life testing types will be then presented and classified, each with its specific aim. The last part will be about the original test approach at Aalborg University, in particular for Silicon IGBTs, which are nowadays the most-used components by far in medium-voltage power electronics. Some insights into failure mechanisms will conclude the tutorial. The expected audience includes students and industry engineers who want to get basic-intermediate information about the reliability testing of Silicon IGBT power modules and its current challenges.

Bio

Francesco Iannuzzo is currently a professor at Aalborg University, Denmark. His research interests are in the reliability of power devices, including condition monitoring, failure theory and testing up to megawatts under extreme conditions. He is the co-author of more than 200 peer-reviewed publications, three book chapters and four patents. He has been contributing 15 technical seminars at first conferences as ISPSD, EPE, ECCE, PCIM and APEC. Prof. Iannuzzo currently serves as Associate Editor for Transactions on Industry Applications and is secretary elect of IAS Power Electronic Devices and Components Committee. In 2018 he was the general chair of the 29th ESREF, the first European conference on the reliability of electronics.

TMB.1 (Tutorial) - Scaling Impacts on Reliability of p-STT MRAM Cells

Authors

Toshio Sunaga - ExIBM

Abstract

Scalability is one of the major requirements for all viable memory products. STT MRAM cell scaling has been studied extensively, because it reduces the write current substantially. However, it also has various impacts, both advantageous and disadvantageous, on other device parameters and memory circuit operating features. Thus, the scaling method itself is very important and it needs careful considerations to keep the MTJ designs as practical memory cells. Using an example p-STT (perpendicular Spin-Transfer Torque) MTJ design with write and read functionalities as constraint factors, a scaling methodology is provided to demonstrate how it impacts on cell operating parameters and reliability items such as endurance and read disturb. For STT MRAM with on-chip ECC (error-correcting code), each memory product tolerates a certain amount of error rates. In endurance case, there are two facets of tolerable error rates, one is a write error rate, WER, ensured from write conditions and the other an endurance failure rate, EFR, as criterion of endurance lifetime, ELT, in number of write cycles. For desired ELT, a guideline to assess how scaling affects EFR for given write conditions with particular WERs is also shown.

Bio

Toshio Sunaga is a technical consultant of memory architecture/circuit design and characterization. He was Senior Adviser of MagIC Technologies Inc., and Principal Fellow of Etron Technology Inc. after retiring from IBM Japan Ltd. as Distinguish Engineer. His experience includes the design and characterization of DRAMs, eFlash, and Field/STT MRAMs. He received PhD from Kyoto University, MSE from Princeton University, both in electrical engineering, and BS in applied physics from Tokyo University of Science.

TMB.2 (Tutorial) - Phase Change Memory: Technology Reliability and System-Level Implications

Authors

Haralampos Pozidis - IBM Research - Zurich

Nikolaos Papandreou - IBM

Abstract

Phase change memory (PCM) has seen many decades of research and development and is considered as the most advanced resistive memory technology. Its universal properties in terms of endurance, retention, scalability and multi-level capability, span the broad space between storage and memory, thus making PCM an excellent candidate for Storage Class Memory (SCM). Today, PCM has entered the market of both standard and embedded memory applications. In addition, PCM has been successfully used in large-scale demonstrations of non-von Neumann computing applications such as neuromorphic and in-memory computing. This tutorial is organized in two parts.

The first part covers the most prominent reliability challenges of PCM from a technology and circuit-level perspective. We will discuss the recent advancements in terms of materials and cell design. Particular emphasis will be given to the reliability challenges of multi-level storage (MLC PCM), which is a key aspect for reducing the cost-per-bit in memory applications. At the same time, multi-level storage (or analog storage) is a key property for neuromorphic and in-memory computing applications.

The second part will cover system-level exploitation of PCM technology and will discuss key applications which would either be enabled or significantly enhanced from this technology. Emphasis will be given first on memory controller design, and central aspects of it such as error correction and media management. Subsequently, we will focus on important applications that a byte-addressable, persistent main memory promises to revolutionize, notably in-memory databases, but also computing in general, with a much larger main memory capacity than what DRAM offers today.

Bio

Haralampos Pozidis manages the Cloud Storage and Analytics group at IBM Research in Zurich, Switzerland. He received a Ph.D. degree in electrical engineering from Drexel University, Philadelphia, USA, in 1998, and was with Philips Research, Eindhoven, The Netherlands, before joining IBM. He has worked on read channel design for DVD and Blu-ray Disc at Philips, and played a key role in developing the first scanning probe-based data storage system at IBM, the "Millipede". His current focus is on the development of Flash memory controllers for all-flash arrays, on phase change memory technology and system solutions, and on accelerated software libraries for machine learning. Haralampos holds over 120 US patents, has co-authored more than 100 publications, is an IBM Principal Research Scientist, an IBM Master Inventor, and a Senior Member of the IEEE.

TMB.3 (Tutorial) - Designing for Analog Reliability: From Components to Circuits

Authors

Dhanoop Varghese - Texas Instruments

Sunglyong Kim - Texas Instruments, Inc.

Abstract

Analog circuits and systems find wide range of applications in today's semiconductor products including voltage regulators, audio and RF amplifiers, comparators and data converters. Analog functionality often demands high voltage or high precision operation leading to unique reliability challenges that are not encountered in digital designs. In this tutorial we will discuss some of the unique reliability challenges for analog circuit design like Positive Bias Temperature Instability (PBTI) of PMOS transistors in comparators, Negative Bias Temperature Instability (NBTI) of PMOS transistors during sub-VDD operation in current mirrors, Channel Hot Carrier (CHC) degradation and hot hole driven gate dielectric breakdown in power FETs used in voltage regulators and polysilicon resistor drifts in high precision circuits. In addition, we will also cover reliability characteristics caused by very high electric field on high voltage lateral power devices such as electric field crowding and charge spreading phenomenon after High Temperature Reverse Bias stress.

Bio

Dhanoop Varghese received the B.Tech. degree in electronics and communication engineering from REC Calicut, India in 2002, M.Tech degree in electrical engineering from Indian Institute of Technology (IIT), Bombay, India in 2005 and Ph.D. in electrical engineering from Purdue University, IN, in 2009. Since 2009 he is with Texas Instruments, Dallas working on the reliability of high voltage analog components. His research interests are in the field of semiconductor device physics, simulation, modeling and characterization of various transistor degradation mechanisms. He has worked on bias temperature, and hot carrier reliability issues in MOSFETs and high-k gate dielectrics. He has served as technical program committee member for IRPS and IEDM and has authored or co-authored more than 25 papers.

Sunglyong Kim received his bachelor's, master's and Ph.D. degree in Electrical Engineering from Ajou University, South Korea. He joined Fairchild Semiconductor as a new technology development engineer in 2000. He had worked on the development of wide voltage range process from 40V to 1200V for mixed signal, power management, automotive, and high side gate driver IC products for his 14 years work life in Fairchild. He joined TI in 2014 and has led HV BCDMOS and discrete MOSFET technology development as a technology development engineer and a technology development manager since 2018. He holds 16 issued and 8 filed US patents, and 24 published papers in international journals and conferences in the areas of power devices and power ICs' architecture and process.

TMC.1 (Tutorial) - Reliability-aware Energy-efficient Smart-IoT & Cognitive-5G

Authors

Sidina Wane - EV Technology

Vincent Huard - Dolphin

Abstract

TBD

TMC.2 (Tutorial) - Challenges in Prognostics and Health Management of Electronic Systems

Authors

Michael Azarian - University of Maryland

Abstract

TBD

TMC.3 (Tutorial) - Materials Analysis Techniques in Semiconductor

Authors

Ling Pan - Intel

Abstract

Materials analysis techniques have been playing important roles in semiconductor technology development, process quality control and failure analysis. In the last 15 years, transistors have evolved beyond traditional poly-Si technology, new and more complicated materials have been introduced into the process as well as the non-planar FinFET transistors, which have brought new requirements and challenges in the characterization techniques. This tutorial gives an overview of a series of materials analysis techniques that are critical to semiconductor technology development and production. The techniques covered in the tutorial include electron microscopy based analysis in nano scale such as electron diffraction, Energy-Dispersive X-ray Spectroscopy (EDS) and Electron Energy Loss Spectroscopy (EELS), Atom Probe Tomography (APT), other structural characterization and chemical analysis techniques in larger scale such as Secondary Ion Mass Spectrometry (SIMS), Time-of-Flight SIMS, X-ray Photoelectron Spectroscopy (XPS), X-ray Diffraction (XRD), Atomic Force Microscopy (AFM), Raman Spectroscopy. Application examples are provided alongside to illustrate the value of individual technique as well as integrated problem solving using multiple techniques.

Bio

Dr. Ling Pan manages the transmission electron microscopy lab in Intel's Corporate Quality and Reliability labs and has supported the development of the 45nm through 7nm process technologies. She received her M.S. and Ph.D. in Materials Science and Engineering from University of Pennsylvania, B.S. in Physics from Beijing Normal University. She has authored/coauthored more than 20 publications in physics, materials, process development and characterization.

TMD.1 (Tutorial) - TBD - Aal

Authors

Andreas Aal - Volkswagen

Oliver Aubel - GLOBALFOUNDRIES

Abstract

The complexity increase of electronic functions in vehicles forces car manufacturers to adapt the electrical system's architecture in order to reduce historically grown and architecture based complexity as well as to optimize complexity management (processes, methods, tools).

Being part of an IoT ecosystem, a car itself becomes a connected entity where data streams enable various new functions and corresponding business models.

However, with respect to reliability this implies two urgent fields of actions. First, automotive electronic systems become strongly software dependent which not only affects the hardware (generation, technology) needed (i.e. AI acceleration), it also causes hardware mission profiles to change over lifetime with central importance to the design-for-reliability process. Second, the increased amount of software algorithm optimized hardware also increases the vulnerability of software based attack windows that focus explicitly on cell-aware aging. Hardware and software based security measures can slow down data processing. To compensate where needed, performance will increase – what is the effect on reliability? The upcoming amount of hardware trojans shows that a much stronger and aligned engagement model along the supply chain is necessary.

This tutorial will discuss the above mentioned challenges and also approaches how to deal with them. As reliability aware design for advanced nodes goes down to process design kits, activities regarding standardized mission profiles based on new automotive load categories and classes and their effect on library cell development will also be discussed.

Bio

Andreas Aal (SM) drives the semiconductor strategy and reliability assurance activities within the electric-/electronic development department at Volkswagen, Germany, which he joined in 2011. His activities concentrate on technology capability enhancement (component construction & system architecture) of most advanced nodes as well as optimization of power electronics integration for automotive applications. He was involved in semiconductor related European projects and is a strong representative of the through-the-supply-chain-joint-development approach.

Andreas (certified reliability professional) published and co-authored various papers, has given tutorials at IRPS and IIRW as well as invited and keynote speeches during various conferences and conventions. He serves as reviewer for different journals and has served in the technical and management committee for IEEE IIRW. He is a member of the IEEE Electron Devices, CPMT, Nuclear and Plasma Sciences, Reliability and Solid-State Circuits Societies and also a frequent participant / contributor of the JEDEC subcommittee 14.2. Since 2007 he is chair of the German VDE ITG group MN 5.6 on (f)WLR, reliability simulations and qualification. He is chair of the European chapter of the SEMI Global Automotive Advisory Council (GAAC) Kick-Off coordinator of the corresponding "European platform for automotive semiconductor requirements along the supply chain" hosted by the VDE ITG, he strongly tries to drive the disruptive automotive transformation process on a collaborative supply chain basis.

Dr. Oliver Aubel leads the automotive program in Globalfoundries (Dresden) with main focus on technical and organizational changes to reflect stricter automotive requirements in advanced manufacturing environments. Before moving into program management he led several global quality projects and beforehand the reliability team in Fab1.

He has earned his diploma (M.S.) in electrical engineering in 2000 and his PhD with focus on microelectronics. After that he joined the reliability team at GLOBALFOUNDRIES (formerly AMD) (Germany).

He authored/coauthored over 80 publications on reliability and is an active member of several reliability or automotive consortia.

TMD.2 (Tutorial) - TCAD-EDA Assisted BTI-HCD Reliability Framework from Devices to Circuits

Authors

Souvik Mahapatra - Indian Institute of Technology Bombay

Abstract

Bias Temperature Instability (BTI) and Hot Carrier Degradation (HCD) are serious reliability concerns in HKMG FinFETs / GAA NSFETs and impact the long term performance of CMOS circuits. It is therefore important to develop a modelling framework to estimate end of life degradation in devices and the corresponding degradation in circuits for various mission profiles. Such a framework can be added to the existing Design Technology Co-Optimization (DTCO) flows for concurrent optimization of performance, power, area and reliability (PPAR) of advanced CMOS chips. This tutorial will address the following:

- (1) A physical BTI model (PMOS NBTI) enabled TCAD framework that can explain measured data across different material / process and architecture (FinFET / NSFET) changes.
- (2) A physical HCD model (N and P MOS) enabled TCAD framework that can explain measured data across bias (VG/VD) space. This includes co-contribution of Self Heat Effect (SHE) activated BTI, especially for PMOS.
- (3) A TCAD based isolation framework for BTI and HCD contribution during device test, to aid development of compact models for cycle-by-cycle AC simulation of circuits.
- (4) A modeling framework for BTI and HCD impact on any (digital / analog mixed-signal) circuits under actual operation (activity awareness), and explore impact of DVFS.
- (5) Estimation of degradation of different circuit benchmarks.

Bio

Souvik Mahapatra is a professor of electrical engineering at IIT Bombay, India. His research interest is primarily on device (logic and memory) and circuit reliability, with focus on electrical characterization, modeling and simulation. He has published over 150 papers in peer reviewed journals and conferences, has given invited talks and tutorials in major international conferences including IEEE IEDM and IRPS. He is a Fellow of IEEE, INAE (Indian National Academy of Engineering) and IASc (Indian Academy of Sciences).

TMD.3 (Tutorial) - Materials Engineering Challenges for Neuromorphic Computing

Authors

Siddarth Krishnan - Applied Materials

Abstract

As CMOS technology scaling slows down and cost goes up quicker than transistor density, alternative computing architectures, such as neuromorphic computing, have been introduced that help speed up computing. While these new computing paradigms eschew the traditional "memory wall" bottlenecks, the materials engineering required for creating robust, reliable, scalable products is still infantile in its lifecycle. This, in turn, has spawned tremendous interest in several non-volatile memories such as Phase Change Memory, Conductive Bridge Memory, Oxygen Vacancy mediated RAM(ReRAM) and Magnetic RAM (MRAM). This tutorial will focus on some of the fundamentals of one of the most promising of these technologies – ReRAM and the device/material co-design requirements thereof, with specific reference to neuromorphic computing technologies.

Bio

Siddarth Krishnan is ideally suited to be in Silicon Valley, having done a bachelors in Metallurgical Engineering from IIT Madras, a Masters in Materials Engineering and a Phd in Electrical and Computer Engineering, both from the University of Texas at Austin. After dabbling a tiny bit in digital design, Siddarth joined IBM SRDC (Semiconductor R&D coop) as a module device and reliability engineer and spent the better part of a decade engineering the gatestack and its reliability for introduction into IBM's 32nm, 22nm and 14nm product lines. During Siddarth's time there, he also helped introduce HfO₂ and metal fill for use in an embedded DRAM and decoupling capacitor that are also used in IBM's server products.

Siddarth moved from New York to California to work in Applied Materials, where he has spent the last 4 years. After spending a few years developing Atomic Layer Deposition (ALD) products for AMAT's MDP business unit, he has spent the last couple of years working on engineering materials for emerging technologies in advanced memory and power devices.

TME.1 (Tutorial) - Exploring Relation of ESD and EMC: Tests, Events to Damage, Failure Types, and Co-Design Approaches

Authors

Alan Righter - Analog Devices

Abstract

This tutorial will explore the events of EMC and ESD as they relate to test methods, damage signatures from the different tests in ICs, and co-design approaches addressing EMC and ESD. First, the various tests will be described and compared to one another. Next common damage signatures for each type of event will be described. With this information, the concept of co-design can be explored to relate to the type of event and the damage signature the co-design is designed to protect. Some co-design tradeoffs may be needed in the consideration of what events are most likely / important in a particular application, but could conflict in co-design, and these will be described.

Bio

Alan Righter has been with Analog Devices since 1997 and currently a Senior Staff ESD Engineer in Santa Clara, CA, involved in customer ESD and EOS (EIPD) return resolution, manufacturing ESD control, and IC design / consulting. From 1984 to 1997, Alan worked at Sandia National Laboratories, Albuquerque, NM and received his PhD in Electrical Engineering from the University of New Mexico in 1996. Alan has been with the EOS/ESD Association also since 1997 and currently is their 2020-21 Association President, and also is ESDA co-chair of the Joint ESDA/JEDEC CDM (Charged Device Model) Standard Working Group responsible for the ANSI/ESDA/JEDEC JS-002 CDM testing standard.

TME.2 (Tutorial) - Exploring Relation of ESD and EMC: Tests, Events to Damage, Failure Types, and Co-Design Approaches

Authors

Melanie Etherton - NXP

Abstract

While the basic principle of protecting integrated circuits (ICs) from damage caused by electrostatic discharge (ESD) events is pretty simple, the details of implementing a full chip protection strategy that has minimal impact on area and leakage, does not limit the functionality or performance of the circuit it is protecting, and prevents any damage from ESD events that ICs are exposed to can be very challenging. The nature of Charged Device Model (CDM) ESD events, where charges are distributed over the complete IC and package and discharge currents flows through internal circuitry, significantly increases the challenge for designing an ESD robust product. For CDM ESD, every aspect of the IC integration can have an impact on the overall product robustness, including the placement of local CDM protection for domain crossings, the primary ESD protection for power and ground domains and seemingly small details in the power and ground grid implementation. This tutorial provides insight to a complete set of verification strategies that will ensure predictive capabilities for CDM ESD robustness, including complex products with billions of transistors, sensitive analog circuitry and multiple power and ground domains.

Bio

Melanie Etherton is a principal engineer at NXP Semiconductors in Austin, Texas where she designs ESD protection for automotive products in advanced CMOS technologies and develops methodologies to ensure full-chip ESD robustness, including new EDA tools. She has almost 20 years of experience in the field of ESD, including her doctoral research work at Robert Bosch GmbH, Germany for her PhD from the Swiss Federal Institute of Technology

(ETH Zurich). She has authored and co-authored numerous papers in the field of ESD and holds several patents in that area. Dr. Melanie Etherton has served as TPC Chair, Vice and General Chair of the EOS/ESD Symposium from 2014 through 2016.

BEOL Reliability

Moderators:

- Ki-Don Lee (Samsung)
- Gavin Hall (ON Semiconductor)

Background

Since the introduction of dual-damascene Cu and low-k dielectric materials, there has been continuous device scaling from 130nm down to 7nm (and beyond) during the last two decades. Numerous innovations in materials, processes, and models have enabled the new technology node successful and reliable, thanks to the efforts of our fellow scientists and engineers. In this year's IRPS, more innovations are happening, as we have seen papers on Ru interconnects and 7nm EUV Co-liner Cu interconnects.

Today, BEOL reliability evaluation includes electromigration (EM), stress-induced voiding (SV/SIV/SM) and time-dependent dielectric breakdown (TDDB). Looking forward, we must also include environmental factors and more extreme use cases of current and thermally induced inelastic behavior of interconnects under various loadings. How do we incorporate these into an accelerated test framework, in both modeling and verification?

Regarding materials, it is key to understand intrinsic and extrinsic size effects – e.g. linewidths, networks, grain boundaries, twins, and texture - and how these relate to stress and the inelastic response. How do we measure and understand these effects and what technological impact do they have? What are the impacts of mechanical response of next generation materials - Ru, Co, alloys, and barrier integrations, etc. – on the reliability, and how do we measure these?

Attendants are invited to discuss their experiences and experiments in metallization, as well as diagnostic and physical/electrical failure analysis techniques that have helped develop their understanding. Additionally, we would like to discuss the pros and cons of fast test methods available, like wafer-level EM, TVS, isothermal EM, and others for rapid learning cycles in development.

Discussion Topics

- Ru Interconnect / 7nm EUV Co-liner Cu interconnects.
- BEOL challenges for 5nm and beyond (Roadmap for RC delay)
- EM Short Length effect (Blech) in 7nm and below.
- Model selection for BEOL TDDB.
- BEOL reliability of power devices, and heterogeneously integrated solutions
- Metal fatigue in microelectronics
- Physical and electrical evaluations
- Reliability methodology & test

IRPS 2020 Workshops– Circuit Reliability and Aging: Measurements and Simulations

Brief summary: In order to determine the chip performance for a given set of design rules, operating voltage and switching speeds, the reliability must be accounted for specific operating conditions. The question is how to account it in right and most effective way. Should we employ the formal approach treating the circuitry as a sequence of elements characterized by known rates of failures, which are traditionally based on the lab data? Or, should we employ more physics-based description of the failure mechanism of the circuitry as a system in the specific environment?

This workshop focuses on the hot topics in the field of circuit reliability:

1. What has been accomplished so far and what should be the path moving forward?
2. ML based approaches are being explored to establish that. Is this the right approach?
3. Are in situ measurements more appropriate to calibrate the models and close the loop?
4. What is the best approach in addressing the extra challenges coming with 3D integration like thermal and mechanical CPI issues to the whole complexity?
5. How to design a chip with a required functionality and performance while satisfying the intended lifetime of the product?

Workshop organizers

Dr. Valeriy Sukharev (Mentor Graphics)



Valeriy Sukharev is a Technical Lead with the Design to Silicon Division (Calibre), Mentor, a Siemens Business, Fremont, CA, USA. He has received the Engineer-Physicist Diploma degree in microelectronics from the National Research University of Electronic Technology (MIET), Moscow, Russia and Ph.D.

degree in Physical Chemistry from the Russian Academy of Sciences. Prior to Mentor Graphics, Dr. Sukharev was a Chief Scientist with Ponte Solutions, Inc., a Visiting Professor with Brown University, and a Guest Researcher with NIST, Gaithersburg, MD. He also held senior technical positions with LSI Logic Advanced Development Lab. He was a recipient of the 2017 and 2019 Best Paper Awards from the International Conference on Computer-Aided Design (ICCAD) and the 2016 & 2018 Mahboob Khan Outstanding Industry Liaison/Associate Awards (SRC). His current research interests include development of new full-chip modeling and simulation capabilities for the electronic design automation, semiconductor processing and reliability management. He coauthored the book "Semiconductor Sensors for Physico-Chemical Studies" (Elsevier Science) and edited a number of Proceeding of the series "Stress induced phenomena in metallization" (AIP). He serves on the editorial boards and technical/steering committees of a number of profiling journals and conferences.

Dr. Georgios Konstadinidis (Google)



Georgios K. Konstadinidis is a Technology and Chip Implementation Lead at Google focusing on the R&D of Machine Learning Accelerators. He received a Ph.D degree in electrical engineering from the Technical University of Berlin, Germany and a B.Sc. Degree in Physics, M.Sc. in electronics from the Aristoteles

University Thessaloniki Greece. From 2010 to 2017 he was a Senior Hardware Architect at Oracle and prior to that a Distinguished Engineer at Sun Microsystems, focused on high performance microprocessor physical design. He has been involved in the technology, design porting, physical design, reliability, optimization, circuit methodology, signal integrity, timing, and CAD tools for several projects. From 1991 to 1995 he was the leader of the high performance bipolar ICs design team at the R&D Center of SGS Thomson in England and in Catania, Italy. He was involved in the design of several ICs for telecommunications, in device modeling and process optimization. Dr. Konstadinidis holds 13 patents and has several IEEE publications. He served as a member of the ISSCC Digital Program Committee from 2002 to 2007, and as Guest Editor for the IEEE Journal of Solid State Circuits. He is a co-author of the book "Clocking in Modern VLSI Systems", Springer, 2009. He currently serves as TPC member of the IRPS Digital Circuit Reliability and IEDM Systems & Circuit Reliability sub-committees

IRPS 2020 – Emerging Memory

Brief summary: Emerging memories have yet to challenge SRAM, eFlash, DRAM, Storage Class Memory (SCM) and NAND/3D-NAND for a large share of the memory market, but continued improvements in performance, cost and reliability of several technologies has brought them closer to the marketplace. Which emerging technologies are most mature and what is gating their widespread adoption? Are reliability challenges a key roadblock for any contending technologies or are performance, cost, or integration the primary challenges? We shall also consider how the potential location of a technology in the memory hierarchy (embedded memory, main memory, storage, or in between such as SCM) dictates reliability requirements

Workshop organizers

Joe McCrate (Micron) and Prof. Tetsuo Endoh (Tohoku University)

IRPS 2020 – Wide-bandgap Workshop (GaN)

Brief summary: GaN is an excellent material for the fabrication of power transistors. These devices are now rapidly finding applications in next-generation power conversion systems with 600-650V transistors already commercially available. Higher voltages are currently targeted (up to 1.2 kV). The success of GaN depends on the understanding of key failure modes and mechanisms. A market transformation is now underway, and the next step is to demonstrate and qualify high reliability.

This workshop focuses on the hot topics in the field of GaN reliability:

1. What are the largest remaining barriers to widespread commercial adoption?
2. Soft vs. Hard switching: What's new? How do you qualify devices in a dynamic regime?
3. GaN devices do not have avalanche capability—Is this a problem or an opportunity?
4. Extrinsic vs. Intrinsic reliability: What are the biggest challenges?

This workshop will address these questions by stimulating discussion on the issues that presently limit the reliability and performance of GaN-based HEMTs. It will be a natural lead-in for the subsequent workshop on SiC reliability.

Workshop organizers

Dr. Shireen Warnock, MIT Lincoln Laboratory

Dr. Shireen Warnock is a technical staff member in the RF Technology Group. Her research interests include III-V materials systems, device characterization, and reliability.

Prior to joining the Laboratory, Dr. Warnock was a graduate student at the Massachusetts Institute of Technology (MIT), where her research focused on the dielectric reliability of gallium nitride metal-insulator-semiconductor high electron mobility transistors for power applications.

Dr. Warnock has authored or co-authored a number of journal and conference publications in the areas of gallium nitride device reliability. She currently serves on the Wide Bandgap sub-committee for the IEEE International Reliability Physics Symposium.

Dr. Warnock received BS, MEng, and PhD degrees in electrical engineering from the Massachusetts Institute of Technology.



Prof. Matteo Meneghini, University of Padova

Matteo Meneghini is associate professor at the Department of Information Engineering at the University of Padova. His main interest is the characterization, reliability and simulation of compound semiconductor devices (LEDs, Laser diodes, HEMTs).



Within these activities, he has published more than 300 journal and conference proceedings papers.

During his activity, he has cooperated and/or co-published with a number of semiconductor companies and research centers including OSRAM-OptoSemiconductor, Panasonic Corporation, Universal Display Corporation, NXP, ON Semiconductor, IMEC, Infineon, Fraunhofer IAF, MIT, UCSB.

Meneghini is a Senior Member of IEEE and a member of the SPIE. He has served as vice- and sub-committee chair for IEEE-IRPS, and as a committee member for several other conferences (including IEDM and WIPDA).

IRPS 2020 – Wide-bandgap Workshop (SiC)

Brief summary: The strong push to maximize performance to demonstrate the superiority of SiC technology vis-à-vis Si has in some cases increased the significance of potential reliability issues. One particular case where this has occurred is in the short-circuit rating of SiC power MOSFETs. Continual decreases in on-state resistance by varying design parameters such as channel length make these devices more susceptible to failure during a short-circuit event since the saturation current, along with the bus voltage, determines the power dissipation that occurs, which in turn determines how quickly the internal temperature rises to a critical value at which Al begins to melt, or other failure mechanisms begin to engage. This workshop will focus on short-circuit reliability in SiC MOSFETs. A list of topics includes failure mechanisms, test methods, trade-offs between performance and reliability, and where the burden for short-circuit protection should lie.

Discussion topics include:

- Brief overview of failure mechanisms.
- Difference in short-circuit behavior between silicon and SiC power devices.
- Brief overview of test methods used.
- Existing trade-offs between on-state resistance, cost, and short-circuit performance.
- Proposals on how to improve device design to reduce susceptibility to short-circuit fault conditions.
- What is an appropriate short-circuit withstand time for industry acceptance?
- Should the burden be on the device designer or the circuit designer?
- Is short-circuit withstand capability required by the circuit designer; or are device designers trying to match the inherent short-circuit performance of Si devices?
- Need for different trade-off points between performance and reliability, depending on the application.

SiC Workshop Organizers

Dr. Aivars Lelis, US Army Research Lab

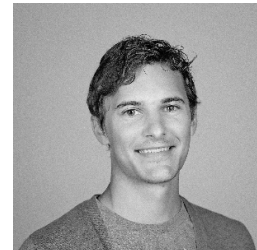
Aivars Lelis leads the Wide Bandgap Device Reliability Team of the Optical and Power Devices Branch in the Advanced Electronics Division at the U.S. Army Research Laboratory in Adelphi, MD, with a focus on the device reliability physics of SiC and GaN MIS-based power devices, for high-temperature, high-voltage, high-efficiency power conversion and conditioning for advanced Army systems.

Dr. Lelis has co-authored over 100 journal publications. He currently serves as the technical chair for Wide Bandgap for the IEEE International Reliability Physics Symposium.



Dr. Thomas Aichinger, Infineon

Thomas Aichinger received his Ph.D. degree in electrical engineering from the technical university of Vienna in 2010. In 2011 and 2012 he was a Postdoctoral researcher at Penn State University, PA, USA. He is currently in the SiC MOSFET technology development of Infineon. His research interests include point defects as well as MOSFET reliability issues such as bias temperature instabilities and gate oxide reliability. He currently serves on the SiC Wide Bandgap sub-committee for the IEEE International Reliability Physics Symposium and in the JEDEC sub-committee focusing on semiconductor standards for SiC power electronic conversion.



IRPS 2020 – Solid State Drive Workshop

Brief summary: Advances in 3D NAND enable endurance gains, capacity increase, lower power consumption and cost reduction, thus making SSD technology attractive for new applications such as AI and cloud computing. At the same time, 3D NAND exhibits new reliability challenges that affect both the resiliency and performance at the system level, e.g., increased number of bit errors, threshold voltage instabilities, frequent read retries, higher read latency, etc. To cope with these issues, modern NAND controller architectures become complex. Resilient FW/HW co-design is critical to ensure the reliability and performance requirements of modern SSDs. Machine learning can aid by offering a valuable tool for prediction and anomaly detection. Analytics together with domain knowledge can provide valuable insights of failure modes and error events relevant to system reliability. On the other hand, blind application of machine learning algorithms can lead to pitfalls. Representative datasets for training, models that provide interpretability and repeatability of the results are key enablers in this quest.

This workshop will discuss the reliability challenges of modern SSDs and the requirements for new applications such as AI, cloud or edge computing. Another intent is to discuss the role of machine learning and analytics in improving the resiliency of modern SSDs through accurate prognostics and prediction.

Moderators

Dr. Jay Sarkar, Western Digital



Jay Sarkar is a Technologist at Western Digital Corporation, San Jose, USA. He received his PhD in Electrical and Computer Engineering from the University of Texas at Austin in 2007, M.S. in Applied Physics from Rice University, Houston in 2004, and B.S.

in Physics from Indian Institute of Technology, Kharagpur in 2001.

He is currently focused on research and development on solid-state storage (SSD) analytics, prognostics, design-aligned machine learning and associated robustness modeling methodologies. He has authored/co-authored over 20 peer-reviewed international conference and journal papers, along with filed/issued patents spanning modeling of system and device designs, analytics and robustness relevant to SSD, Phase Change Memory and 3-D NAND memory. He is a Senior Member of the IEEE and serving the IRPS 2020 System Electronics Reliability Committee as Chair.

Dr. Nikolaos Papandreou, IBM Research



Nikolaos Papandreou is a Research Staff Member at IBM Research – Zurich, Switzerland. He received his Diploma and Ph.D. degree in Electrical and Computer Engineering from the University of Patras, Greece, in 1998 and 2004, respectively.

His current research interests include solid-state memory technologies, in particular phase-change memory and 3D NAND flash, memory controller development with a focus on performance and reliability, signal processing and machine learning with emphasis in algorithmic design and optimization.

Nikolaos has published more than 60 articles in journals and conference proceedings and holds over 50 granted patents in the area of solid-state memory. He is a Senior Member of the IEEE and he currently serves in the IRPS 2020 System Electronics Reliability Committee.

RF/mmW/5G Workshop

RF/mmW devices; GaN, SiGe or Si? Which will offer the best solution for 5G?
(Power/Reliability/Cost)

Moderators:

- Fernando Guarin (GlobalFoundries), Si-SiGe
- Farid Medjdoub (IEMN CNRS), GaN

Background

Given the power, cost structure and integration required for mmW 5G deployment, what gaps remain for Silicon and SiGe to be viable solutions? The market for cellphones, Base Stations and IoT solutions is predicted to explode in the near future. Many companies are in the process of designing their mmW solutions for 5G. In this session we will review the most likely technologies that will dominate the sizable 5G market. Most key players in the industry realize that there is a sizable opportunity for Si and SiGe technology solutions as we transition from the few antennas required in 4G to the multi element antenna array solutions, hence the power requirements have been reduced to a range that is well suited for Silicon and Silicon Germanium technology offerings. Will this be sufficient to displace the proven and well-entrenched RF mmW solutions offered by III-V?

Which solution will win in the market from the perspective of?

- Power
- Cost / Integration
- Reliability

Discussion Topics

- Operating lifetime requirements
 - EOL, should it be 10 years, 3 years, X years?
 - Duty cycle 100%?
- Power requirements for 5G (Linearity/Efficiency) (Handsets and Basestations)
- Translating reliability behavior from device to circuit level – what matters to the end users?
 - Reliability simulator requirements
- Appropriate methods for testing and characterizing RF reliability?
 - Circuit benchmarks, PA, LNA, and Switches
 - Scaled DC measurements
 - Setting up device level tests to accurately reflect circuit level benchmarks
 - Associated impact for various classes of circuits/IP blocks.
- Thermal
 - TCAD modeling
 - Self-heating
 - simulation vs. practical usage

Workshop on BTI and HCD

Xavier Federspiel, ST Microelectronics
Souvik Mahapatra, IIT Bombay

Bias Temperature Instability (BTI) continues to remain as a crucial reliability concern in CMOS devices. Although it comes in two variants – Negative BTI (NBTI) in PMOS and Positive BTI (PBTI) in NMOS, modern devices with Replacement Metal Gate (RMG) based High-K Metal Gate (HKMG) processes primarily suffers from NBTI while PBTI is negligible.

The physics of NBTI has remained debated, although any model should be able to explain different experiments (as follows) in order to qualify as something meaningful:

- Time kinetics of NBTI during (stress) and after (recovery) DC and AC stress at multiple gate bias (V_G) and temperature (T) – preferably T range covering space to automotive applications, and AC stress at multiple duty cycle and frequency.
- Impact of different processes, such as Nitrogen in gate stack, Germanium in channel, device dimension (e.g. fin length/width), layout, etc., on the time kinetics, V_G and T dependence.

However, from a qualification viewpoint, simple empirical models are sufficient to benchmark foundries or process recipes, although care should be taken that the stress and use conditions are not much different to project to operating conditions. Physical models can provide better estimation of end-of-life NBTI.

Hot Carrier Degradation (HCD) depends on channel length (L_{CH}), drain bias (V_D) and ratio of drain to gate bias (V_D/V_G). Classical worst-case projections approaches, such as mid V_G (I/O devices or nodes >90nm) or $V_G=V_D$ (node <90nm) might be sufficient for foundries or process benchmark. However, accurate aging model dedicated to circuit simulation might require refined models taking into account complex V_G dependencies, HCD-BTI interaction as well as self-heating effects. As a matter of fact, the BTI-HCD interaction can become a crucial issue especially for PMOS devices, if qualification is done at $V_G=V_D$ condition, and the situation can get exacerbated due to self-heating effect in modern devices (FDSOI, FinFET, GAA NSFET) with confined channels.

This workshop would focus on the following:

- Overview of BTI mechanism (~15 mins)
- Overview of HCD mechanism in high and low voltage devices (~20 mins)
- Qualification / test methodologies for HCD and BTI (~ 25 mins)
 - Choice of stress bias (V_G/V_D condition) and AC-DC factor
 - Decoupling of BTI and HCD
 - Impact of self-heating effect (DC vs. AC stress)