IRPS
International Reliability Physics Symposium

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- **In-person discussions on the hottest reliability topics**

- **Cultivate networking and collaboration**
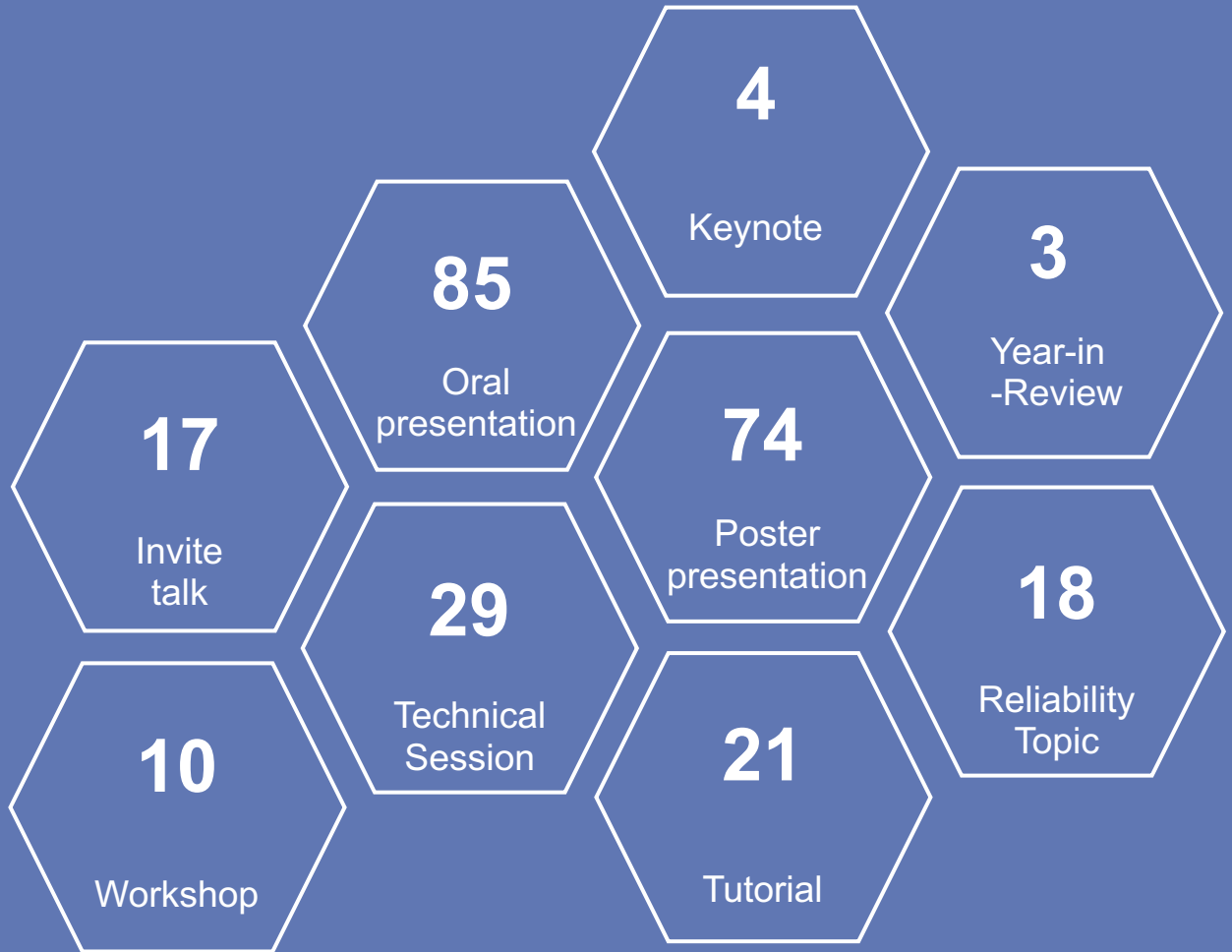
4 Keynote

85 Oral presentation

3 Year-in-Review

17 Invite talk

74 Poster presentation

29 Technical Session

18 Reliability Topic

10 Workshop

21 Tutorial

All of these (except Workshops and Posters) will be available via real-time streaming in the US Central time zone with virtual attendees having Q&A access opportunities. For those virtual attendees who cannot watch the live presentations, the material will be available on demand to all attendees after the symposium with the ability to communicate with the authors.

IRPS
## International Reliability Physics Symposium

Welcome to IRPS

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Join us at IRPS 2024 from April 14-18, 2024, in Dallas, TX!
On behalf of the management committee and board of directors, it gives me great pleasure to extend a warm welcome to all attendees, with sincere gratitude to our patrons and exhibitors. You can attend the symposium both IN-PERSON and VIRTUALLY. IRPS 2024 will offer a two-day tutorial, and a three-day technical program containing a poster and workshop session. Be sure to visit the IRPS homepage and complete your registration. We certainly look forward to your participation!
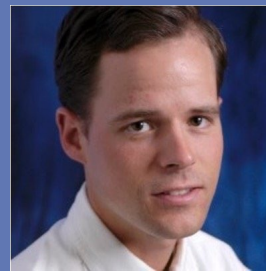
IRPS 2024 General Chair, Koji Eriguchi (Kyoto Univ.)
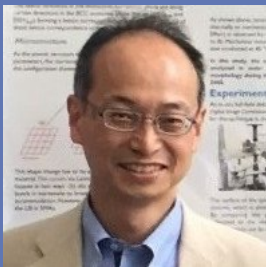
Vice General Chair
Susumu Shuto (Toshiba)

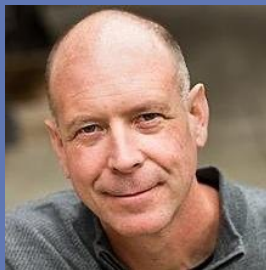**Technical Program Chair**
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Overview

For 62 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment. IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world. The IRPS2024 and the International ESD Workshop (IEW) will be co-hosted with IEW registrants participating in both IRPS and IEW programs.

For 2024, we are face to face but have adopted a hybrid format allowing virtual access to live oral presentations. The Technical Program consists of 4 keynote speakers, 17 invited speakers, 85 oral presentations organized in 29 technical sessions on 18 reliability topics, 10 Workshops, 74 Posters, 21 tutorials and 3 Year in Reviews, which serves as a summary of research in the past year. All of these (except Workshops and Posters) will be available via real-time streaming in the US Central time zone with virtual attendees having Q&A access opportunities. For those virtual attendees who cannot watch the live presentations, the material will be available on demand to all attendees after the symposium with the ability to communicate with the authors.

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Keynote Speakers

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"Hafnium-Oxide-Based Ferroelectric Devices for Low-Power Memory and AI Applications: Promises and Reliability Challenges"

東京大学
THE UNIVERSITY OF TOKYO

Shinichi Takagi (Professor, The University of Tokyo, Japan)

"Innovative Technologies for Sustainable Future of Semiconductor Industry"

SAMSUNG

Su Jin Ahn, EVP, Advanced Technology Development Office at Samsung Semiconductor R&D Center, Samsung)

"Utility-scale Quantum Computing - Advances and Future Challenges"

IBM

Rajeev Malik, Program Director, Systems Development & Deployment at IBM Quantum)

"Analog Technology Scaling and Reliability Implications"

TEXAS INSTRUMENTS

Sameer Pendharkar (VP of Advanced Technology Development, Texas Instruments)

Detail of keynote talk: https://www.irps.org/keynote-speakers

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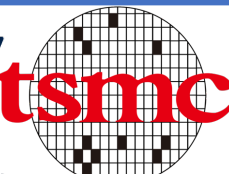
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Year-in-Review
in Tutorial Session

The IRPS Reliability Year-in-Review (YiR) session consists of three presentations reviewing the past year's reliability work by experts in the field for areas of high interest. It is an excellent augmentation to the tutorial sessions immediately preceding, and attendees may obtain keen reliability insights in a short amount of time

"From the Mathematical Foundations to the Physical Models: A Year in Review of Neuromorphic Reliability"

NIST

Brian Hoskins Physicist in NIST

"Dielectric Breakdown: Advances in Characterization Techniques and Extrapolation to Use Conditions for Low and High-Voltage FETs"

BROADCOM

Bonnie Weir, Master Engineer at Broadcom Inc.

"The exciting era of compact electronics with Gallium Nitride technology"

Stanford University

Srabanti Chowdhury, Associate Professor of Electrical Engineering, Senior Fellow at the Precourt Institute for Energy

Detail of Year-in-Review: https://www.irps.org/year-in-review
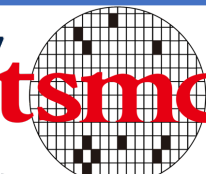
IRPS
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Tutorial Session

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- In-person at IRPS and on-demand later
- Over 30 hours of crash course with Q&A on 20 focused reliability topics (over 2 days)
- Experience sharing from academic and industrial leaders
- Summary on current best-known methods (BKM), reliability challenges, and future trends

Speakers from:

BROADCOM · Infineon · imec · NIST · M2D · PURDUE UNIVERSITY · Stanford University · Qorvo all around you · ST · TU WIEN · transphorm · Wolfspeed

Circuit & System

Space Application
Neuromorphic
Automotive
Data center
5G, 6G

Device

Nanosheet
Forksheet
PRAM
GaN
SiC
NAND
DRAM

Yield
Statistics
Modeling
2.5D/3D Package
TCAD
Plasma Damage

Process

FEOL & MOL & BEOL
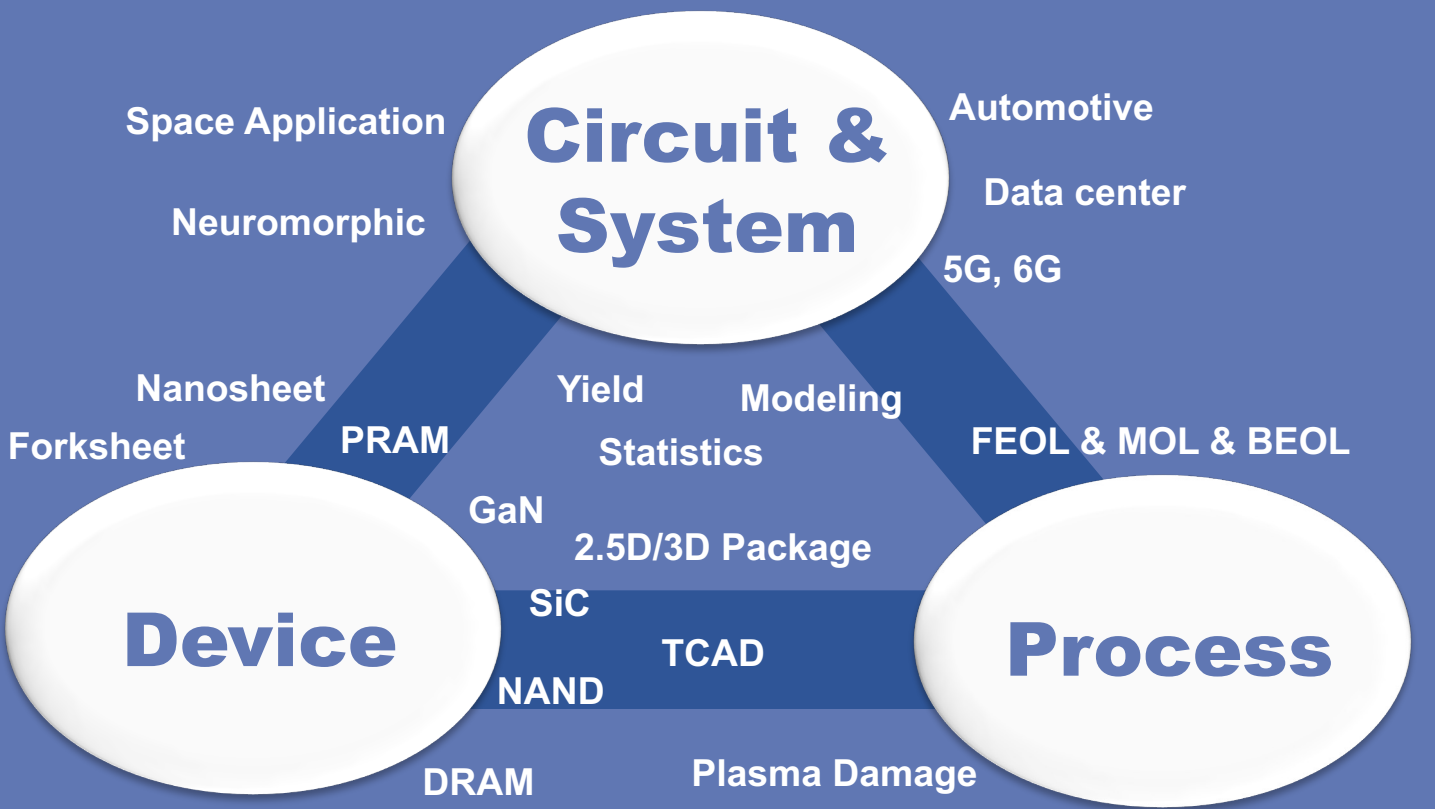
Detail of Tutorial Session: https://www.irps.org/tutorial2024

Don't miss the Exhibition of IRPS 2024.

- **Date and time:** Apr. 16th–18th
- **Location:** the front of the conference room (International I-IV)
- **Why Visit Exhibition:**
  - **Discovering:** Cutting-edge products and solutions.
  - **Expert Guidance:** Engage with our expert team
  - **Networking:** Connect with global professionals
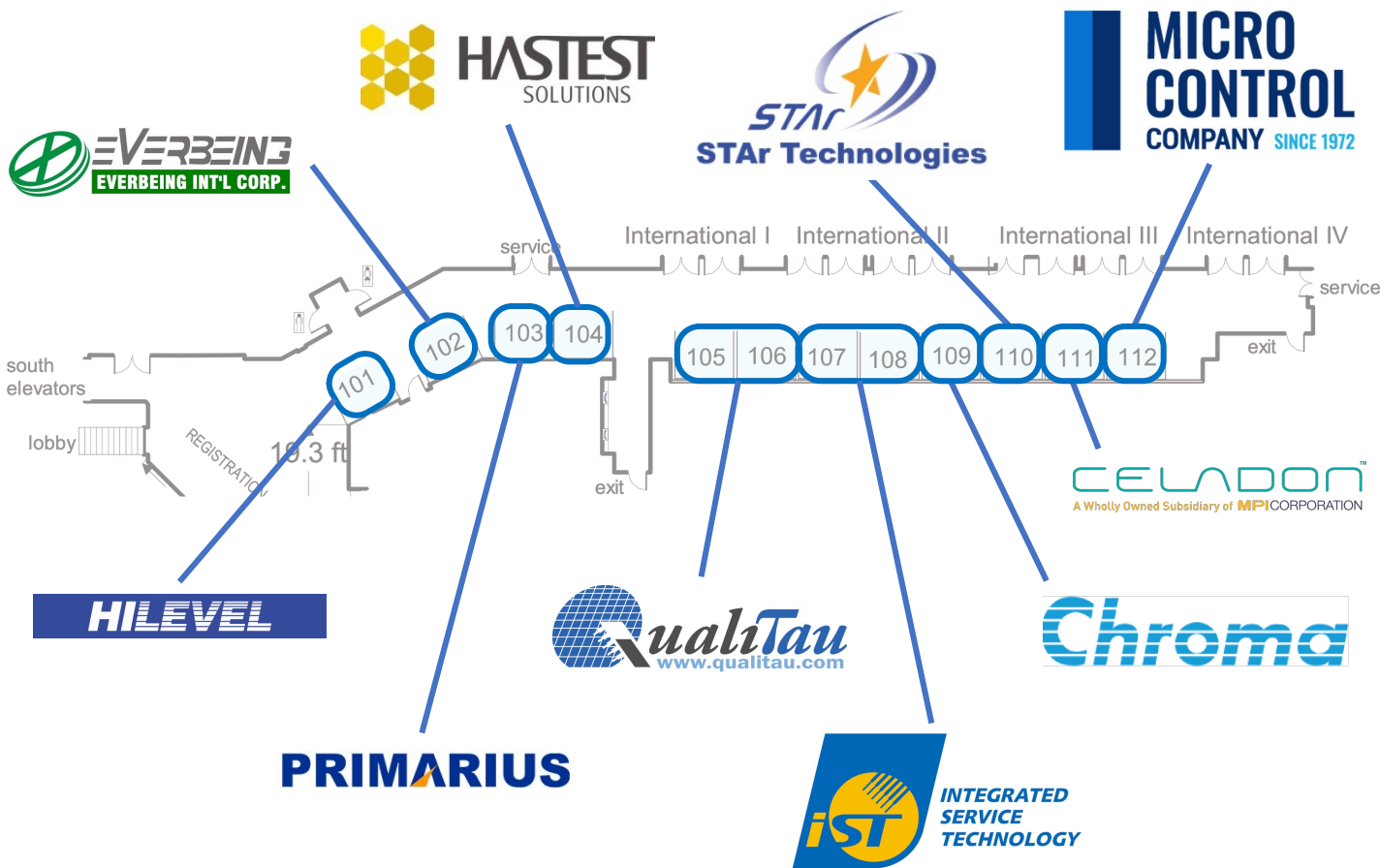
Detail of Exhibition: https://www.irps.org/exhibitors

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Workshop

Don't miss the Workshop

- **Date:** Apr. 16th (Tue)
- **Time:**
  - 6:00 PM-7:30 PM: Reception
  - 7:30 PM-8:30 PM: 1st Session
  - 8:45 PM-9:45 PM: 2nd Session
- **Why Visit Exhibition:**
  - **Discovering:** In-person discussion on the hottest reliability topics.
  - **Networking:** Connect with global professionals

7:30 | 8:30	Circuit Aging Simulation Challenges & Solution	Reliability Aware EDA (BEOL /Heating)	PID-Well Charging in product design	Increasing urgency of GaN reliability physics development	RAS (Reliability, Availability, Serviceability) in the Data Center
8:45 | 9:45	Technology scaling challenges: Power vs Reliability	HCl and self-heating advance devices Nanosheets	Challenges in RF /mmW /5G	ESD EDA: What Can be Done Now and in the Future?	Functional Safety: Industrial, Automotive and AI

Detail of Workshop: https://www.irps.org/workshops

IRPS International Reliability Physics Symposium

Invited Speaker

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| Session	Speaker	Title
Circuit Reliability and Aging	H. Amrouch (Technische Universität München)	Machine Learning Unleashes Aging and Self-Heating Effects: From Transistors to Full Processor
Emerging Memory	U. Schroeder (Namlab)	Ferroelectric HfO2-based Capacitors for FeRAM: Reliability from Single Devices to Memory Arrays
Failure Analysis	A. Griffin (TI)	TBD
GaN Devices	S. Bahl (Texas Instrument)	Status of JEDEC JC-70 Standards for GaN Power Devices Characterization and Reliability
Gate/MOL Dielectrics	M. Kobayashi (Univ.of Tokyo)	Performance and reliability of nanosheet oxide semiconductor FETs with ALD-grown InGaO for 3D integration
Gate/MOL Dielectrics	H. Zhou (IBM)	TDDB on gate-all-around nanosheets
Memory Reliability	R.Frickey (Solidigm)	Comparing the Reliability of Solid State Drives based on TLC and QLC NAND Flash Memories
Metallization/BEOL Reliability	M. Herklotz (Globalfoundries)	EDA method to address interconnect reliability and reduce overdesign in custom analog designs
Neuromorphic Computing Reliability	K.Toprasertpong (The Univ. of Tokyo & Stanford Univ.)	Robustness to Device Degradation in Silicon FeFET-based Reservoir Computing
Packaging and 2.5/3D Assembly	K. Mysore (AMD)	2.5/3D Package Reliability
Product Reliability	T. Zhang (Ansys)	Design for Reliability (DFR) Aware EDA Solution for Product Reliability
Radiation Effect Reliability	E. Zhang (Univ.of Central Florida)	Charge Trapping in Irradiated 3D Devices and ICs
Reliability Testing	R.Herrick (Robert Herrick Consulting)	Reliability testing for silicon photonics and optoelectronics
RF/mmW/5G	J. Dunworth (Qualcomm)	RF/mmW 5G/beyond 5G: advances & reliability
SiC Devices	P. Moens (onsemi)	Evaluating SiC MOSFET Gate Reliaibility, Life Models and Safe Operating Area
System Electronics Reliability	Pradeep Lall(Auburn University)	Assessment of Fracture Propensity of Flip-Chip Ball Grid Array Interfaces under Deformation and Fatigue Loads at Sustained High Temperatures
Transistors	Myunggil Kang (Samsung)	Device design and reliability of GAA MBCFET

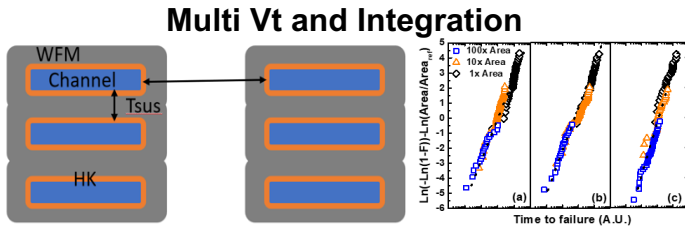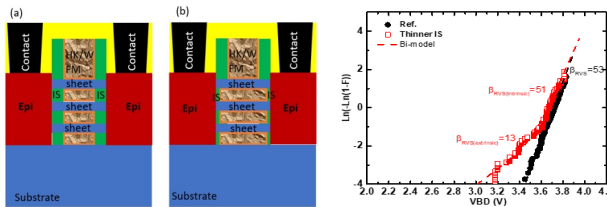**Detail of Invited Speaker:** https://www.irps.org/invited-speakers

Gate/MOL Session

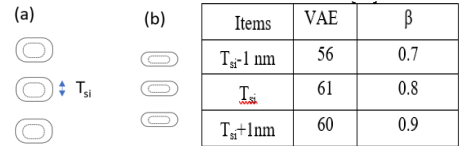**2A.1 "Challenges of gate stack TDDB in gate-all-around nanosheet towards further scaling"** H. Zhou et al., IBM Research, presents GAA features and impact on TDDB reliability: Multi-VT integration, WSI and area scaling, spacer, Tsi.

Multi Vt and Integration

Wsi and Area Scaling
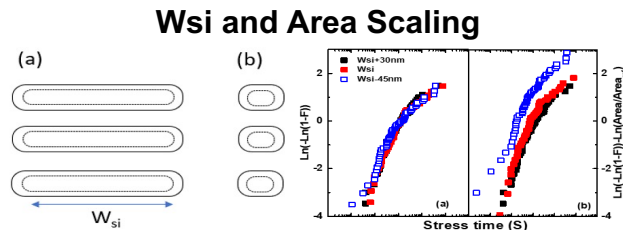
Inner Spacer and Bi-model

Tsi and TDDB

Items	VAE	β
T_{si}-1 nm	56	0.7
T_{si}	61	0.8
T_{si}+1nm	60	0.9

Gate/MOL Session

9A.2 "Joint Weibull-Fréchet model for dielectric breakdown in filament formation including reverse area scaling" E. Wu et al, IBM Research, presents a statistics-based model "Join Weibull-Fréchet" to characterize reverse area-scaling of RRAM TBD, and enabling reliability projection from test area to chip/product area.
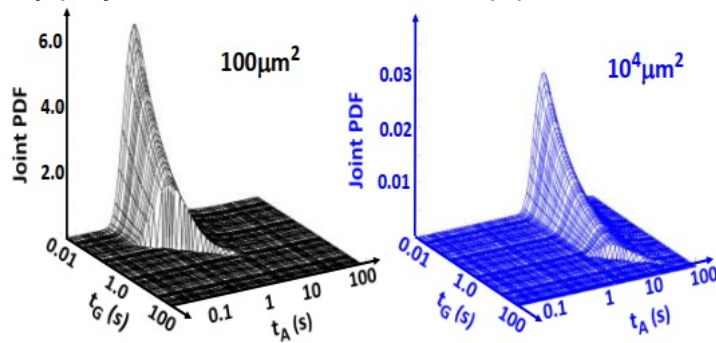
Fig. 3. The joint PDF (Eq. 5) of the Weibull-Fréchet model for 100 and $10^4 \mu m^2$ using the parameters in Fig. 5 (a)
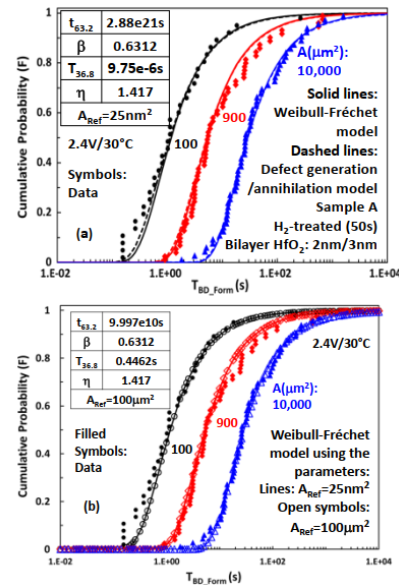
Transistor Session

4A.1 "Fundamental understanding of NBTI degradation mechanism in IGZO channel devices" Y. Zhao, et. al., KU Leuven, presents a comprehensive understanding of NBTI in IGZO TFTs with varying channel thickness and gate length.

Negative shifts are enhanced for thicker IGZO films

Shorter gate length → enhanced Vg stress
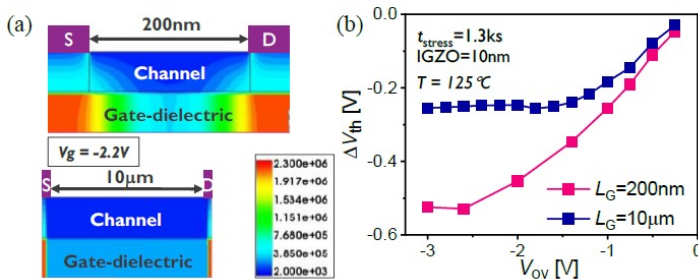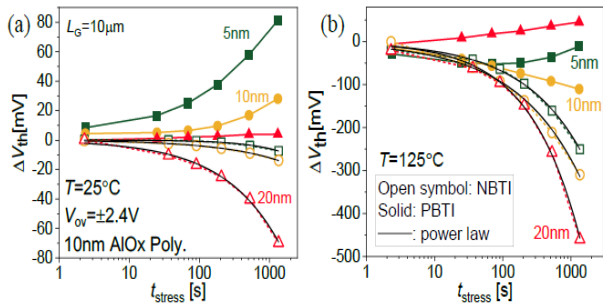
Fig.2 ΔV_{th} as function of stress time (time kinetics) of NBTI (open symbols) and PBTI (solid) under $T=25°C$ (a) and $125°C$ (b). NBTI increases for thicker IGZO films. At 125C, NBTI is more pronounced than PBTI. All the NBTI curves can be fitted by power laws (black lines), see Eq. (1).

Fig. 6 (a) 2D distribution of electric field in short(upper) and long(lower) devices, showing higher E_{ox} in the regions under S/D. The shorter device experiences increased E_{ox} in the center of the channel due to larger impact from the regions under S/D. (b) Voltage dependence of ΔV_{th} at $t_{stress}=1.3ks$ for short and long devices. The shorter device shows larger degradation and stronger voltage dependence.

GaN Device Session

6B.1 "PBTI in Scaled Oxide Submicron Enhancement Mode High-K Gallium Nitride Transistors," S. Joy, et. al., Intel, presents E-mode HEMT with 2nm Hf-based dielectric (high-k) in Fabricated on 300 mm GaN-on-Si wafer
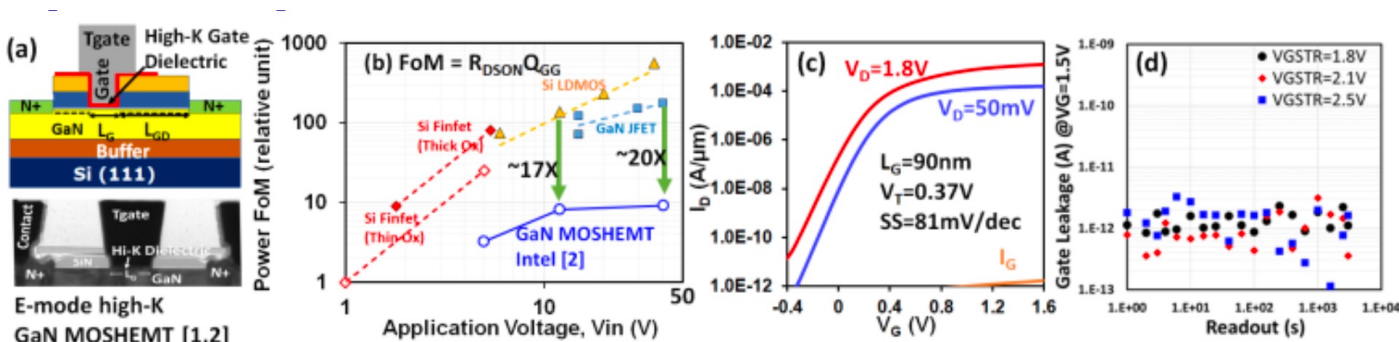
Figure 1. (a) Schematic and TEM of gate-recessed, high-k E-mode GaN MOSHEMT in this work; (b) reported Power FoM ($R_{DSON}Q_{GG}$) of Intel GaN MOSHEMT [2]. (c) I_D-V_G of L_g=90nm GaN MOSHEMT showing ON/OFF ratio>10^8, SS~80mV/dec, and I_G<5pA/µm (d) no prominent increase in I_G during PBTI measurements.

Radiation Effect Reliability Session

10C.1 "Soft-Error Sensitivity in SRAM of 3 nm Gate-All-Around (GAA) Technology" T. Uemura, et. al., Samsung Electronics, presents Alpha- and neutron-SERs in SRAMs manufactured with 3 nm bulk gate-all-around (bulk-GAA) process technology. The SER in SRAM of bulk-GAA is maximally 1.56X higher than in the same cell-size SRAM of bulk-FinFET. Moreover, shrinking cell size decreases the SER by a maximum of 0.38X in bulk-GAA. The SER of the minimum-size SRAM in bulk-GAA is lower than in bulk-FinFET.
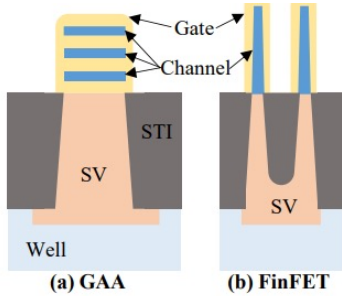
Fig. 6 The cross-section image of Y-cut (**Fig. 4(a)**) in (a) bulk-GAA and (b) bulk-FinFET transistors. The sensitive volume (SV) in bulk-GAA is larger than in bulk-FinFET.
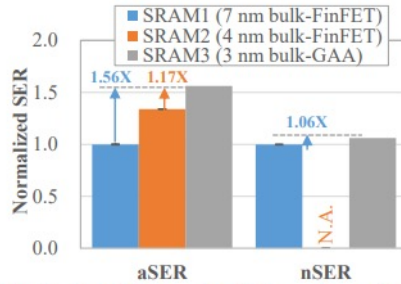
Fig. 2 The aSER and nSER at the nominal voltage (0.75V in all the SRAM) in FinFET SRAMs (SRAM1 and SRAM2) and GAA SRAMs (SRAM3). The cell size is identical in SRAM1, 2, and 3 (**Table I** and **Fig. 1**).
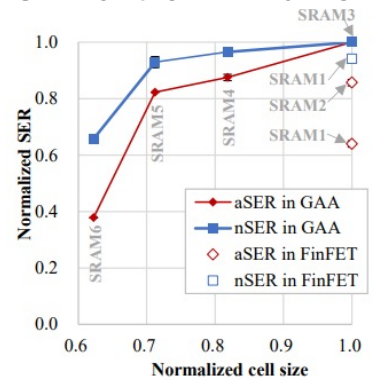
Fig. 7 Normalized aSER and nSER as a function of the cell size in the SRAMs.

ESD&Latch-up Session

8C.1 "Insight into Latchup Risk in 28nm Planar Bulk Technology for Quantum Computing Applications" K. Servulova, et. al., imec. A Cryogenic environment is needed for quantum computing and a latch-up property will be changed. This paper presents well defined experiment and interpretation, and the current gain characterization of the parasitic bipolar transistors over wide temperature range is a valuable reference for future work
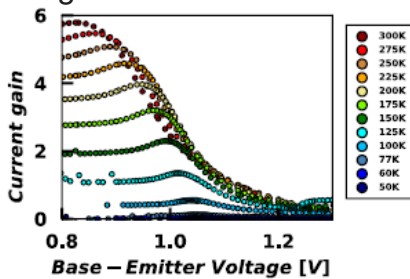
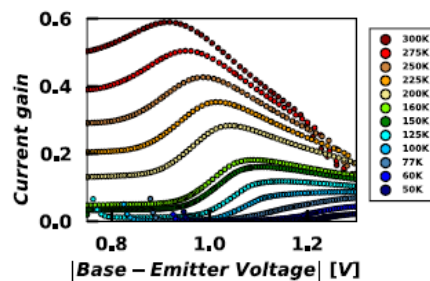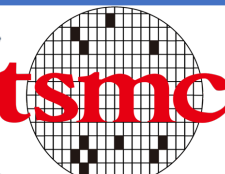Figure 10: Simulation results of NPN β-gain in advanced planar technology at temperatures from 300 K to 30 K.

Figure 11: Simulation results of PNP β-gain in advanced planar technology at temperatures from 300 K to 30 K.

RF/mmW/5G Session
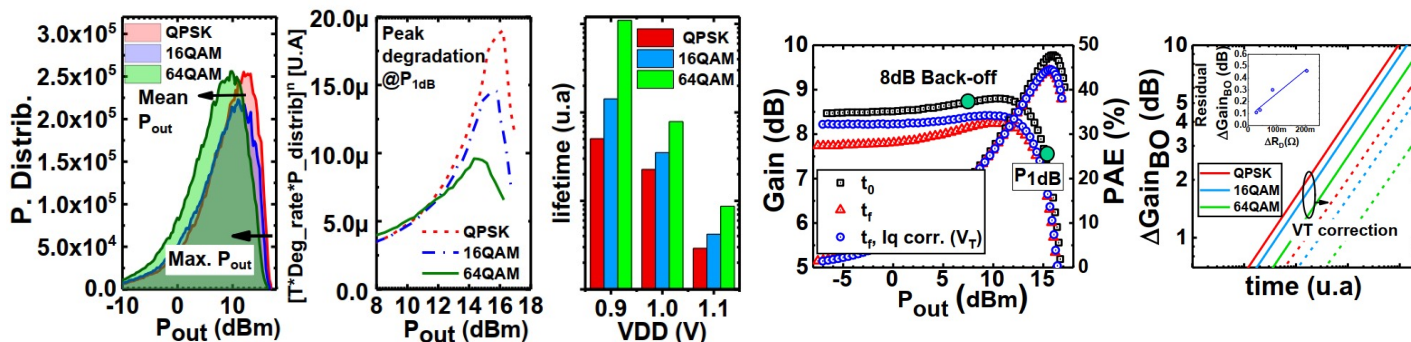
4B.2 "A Methodology to address RF aging of 40nm CMOS PA cells under 5G mmW modulation profiles," A. Divay, et. al, cea, presents a simplified methodology to link CW RF stresses to complex profiles, and Improved lifetime for most complex 5G modulation due to output power/linearity constraints

RF/mmW/5G Session

4B.1 "DC Reliability study of high-k GaN-on-Si MOSHEMTs for mm-Wave Power Amplifiers" B. O'Sullivan, et. al.,imec, presents High-k GaN-on-Si MOSHEMTS for mm-Wave Power Amplifiers monolithically integrated on 200 mm Si substrates. Defects in HfO2 or Al2O3 result in significant Vt instabilities, with dielectric-dependent charge emission kinetics: band alignment between high-k shallow defect levels and AlGaN conduction band enables full (Al2O3) or partial (HfO2) charge de-trapping
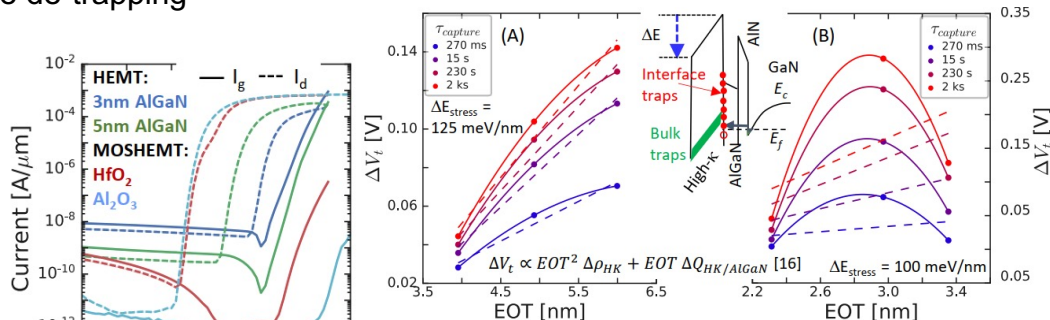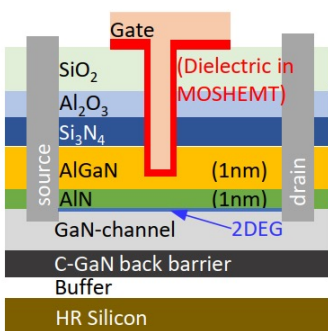
Fig. 5. ΔV_t vs EOT for (A) Al$_2$O$_3$ and (B) HfO$_2$ MOSHEMTs at 125°C. A non-linear trend is seen in both cases, suggesting high-κ bulk trapping (inset). Stress bias to yield constant oxide field from calibrated simulated deck for each thickness

Circuit Reliability Session

4C.1 "Demonstration of Chip Overclock Detection by Employing Tamper-aware Odometer Technology," R. J. Diaz-Fortuny, et. al., imec, proposes a significant improvement of the tamper-aware odometer concept to obtain the degradation of a chip utilizing enhanced ring-oscillators-based degradation monitors . The authors present two new aging odometers designed in 28nm tech that, together with clear and concise data, allows avoiding the need of a pre-stres phase to obtain the age of a chip based on individual BTI and HCD RO readings. With the presented technology, the authors can unequivocally detect a previous overclock test to conducted intentionally to the chip's digital circuitry.
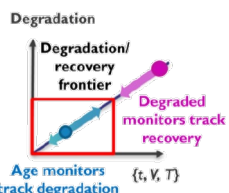
Fig. 1. Tamper-aware odometer concept where two sets of odometers are deployed: one non-degraded set (blue oval) for chip age determination, and a second set highly pre-stressed during production (pink oval) for tamper-awareness. Through chip lifetime, the age monitors track wear-out while the degraded monitors track recovery to detect fraudulent IC anneal.
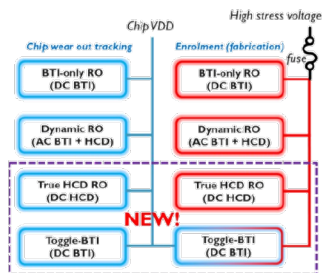
Fig. 2. Updated tamper-aware odometer technology with two new RO designs: the true-HCD RO, an enhanced version of our previous eHCD RO [8], and the toggle-BTI RO that allows having different RO degradation kinetics in a single RO design.
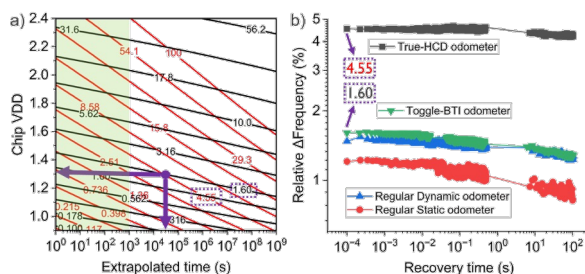
Fig. 9. (a) shows the modelled degradation data of the True-HCD (red isolines) and the Toggle-BTI (black isolines). The green section determines the new data space used in this work, i.e., as from 0.9 V, while in our previous works [8-9], the degradation maps were obtained as from 1.8 V. In (b), the 4 odometers full recovery traces are shown and, by selecting the corresponding isolines matching the first recovery values of the True-HCD (ΔFreq(%) = 4.55) and the Toggle-BTI (ΔFreq(%) = 1.60), we unequivocally unveil that the chip has been overclocked for ~12 h at a VDD of 1.3V (purple arrows), at their intersection.

System Electronics Session

5C.3 "Virtual FA methodology for DRAM: Real-time analysis and prediction method using Telemetry, Field data," J. Lee, et. al, Samsung Electronics, presents Fast methodology of failure detection in deployed systems compared to conventional failure analysis flow. The paper describes a methodology that is widely conceptualized but in practice is hard to implement. The authors were successful in providing examples of failure modes that are classifiable on a database and are able to be resolved and confirmed through collaboration with customers. Both these elements are key to the success of this vFA methodology.
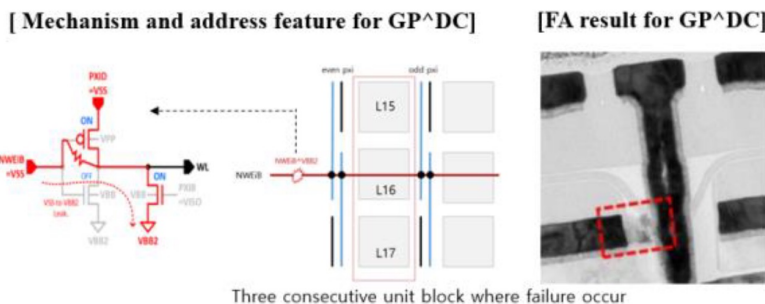

Fig.2: Address feature for GP^DC: When a defect occurs in a NEWiB^VBB2 node, the GP^DC failure occurs in three consecutive unit blocks that share NWEiB and PXi. [3]

Failure Analysis Session

10B.1 "**Laboratory X-Ray-Assisted Device Alteration for Fault Isolation and Post-Silicon Debug,**" K. Celio, et. al., intel, present new fault isolation technique and post-silicon debug for backside power delivery networks and multi-die stacking devices.
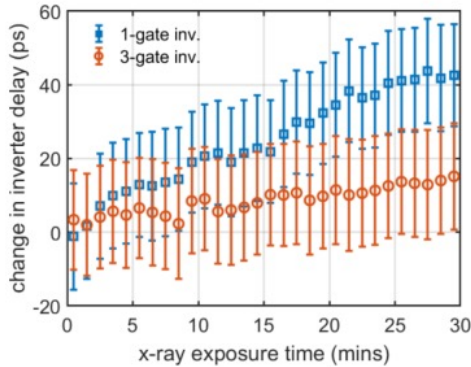

Figure 3. *Observed change in single CMOS inverter delays with x-ray exposure time. X-ray beam size and circuit layout enable overlap of ray with only 1 inverter in the inverter chain. Data shown for x-ray perturbation of both a 1-gate and a 3-gate inverter. Errorbars sho +/- standard deviaion in measured delay.*
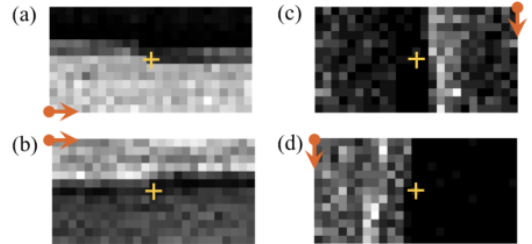
Figure 4. *Demonstration of XADA localization of a physical defect in an SRAM circuit. Defect location is notated by a cross, and x-ray scan directions are notated by arrows. DUT is operated near failing voltage in a looping test pattern fashon, and the number of failing tests per pixel in the XADA raster are plotted, with white pixels corresponding to more failing tests, and black pixels to less. The XADA raster area is 60x30 µm, the pixel size is 2.4 µm, the dwell time is 1 s/px, and the x-ray beam diameter is ~4.7 µm. X-ray rasters in different directions (a-d) each observe a change in the number of failing tests near the defect location, with the x-ray beam interaction causing a decrease in the number of failing tests (an improvement in V_{min}).*

Reliability Testing Session

2B.1 "**Modeling Dark Current Degradation of Monolithic InGaAs/GaAs-On-Si Nano-Ridge Photodetectors,**" P. Hsieh, et. al., imec, thoroughly investigated dark current conduction mechanisms and degradation. The proposed semiempirical carrier emission/capture model successfully portrays the degradation and recovery, therefore enabling acceleration factor and device lifetime estimation, providing a more precise vision toward defect kinetics.
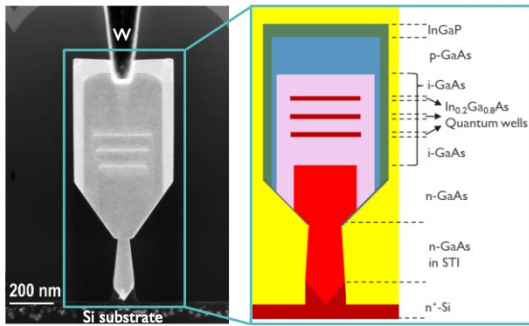

Figure 1. The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the InGaAs/GaAs nano-ridge p-i-n photodetectors. Detailed layer stacks are shown in the zoom-in schematic.
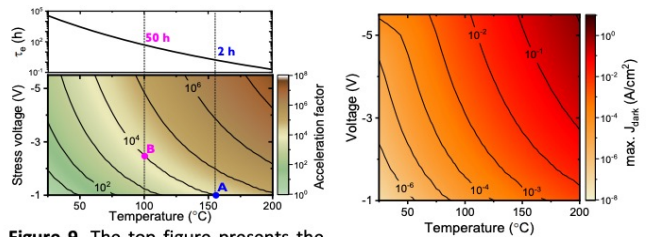

Figure 9. The top figure presents the emission time constant as a function of the temperature, and the contour map below calculated the acceleration factor (AF) at various voltages and temperatures ($T_{ref.}$ = 25 °C, $V_{ref.}$ = -1 V). A and B are equivalent stress conditions with AF = 10^4.

Figure 10. Estimated max. I_{dark} degradation (at V_{sense} = -1 V) in device operating life under various stress conditions, based on the comprehensive model developed in this work.
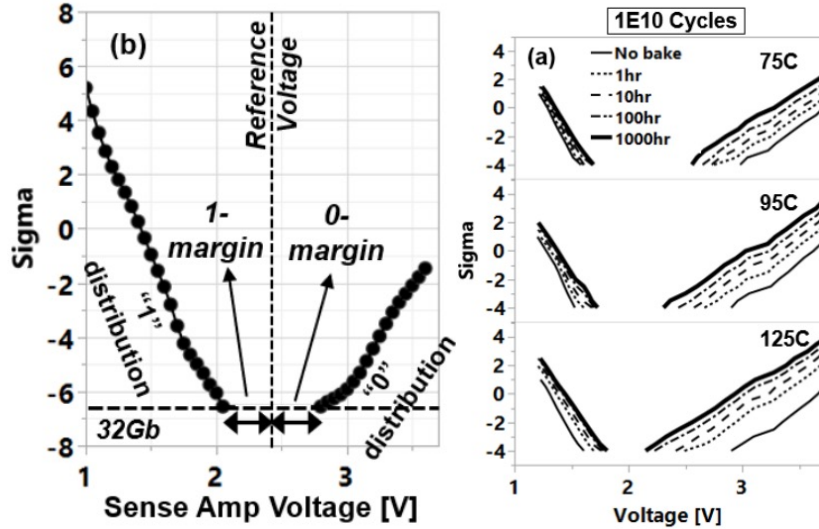
Emerging Memory Session

7A.4 "Comprehensive Reliability Assessment of 32Gb HfZrOx-Based Ferroelectric NVDRAM Memory," D. Ettisserry, et. al., Micron, presents array level HZO ferroelectric, and describes new reliability mechanisms.

Memory Reliability Session

3A.2 "Experimental Segmentation of Vertical Charge Loss Mechanisms in Charge Trap-Based 3D NAND Arrays," L. Chiavarone, et. al., Micron, presents that vertical charge loss in charge trap 3D NAND arrays is characterized and modeled. The contributions of charge de-trapping from bandgap-engineered tunnel stack and charge loss from silicon nitride storage node are experimentally separated for the first time.
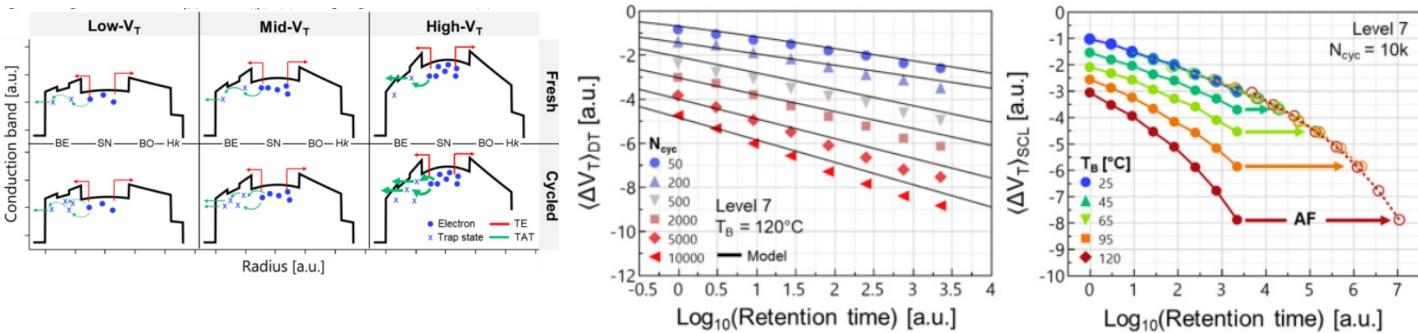
Late news (Gate/MOL Dielectrics)

7B.4 "On-Chip Single-Shot Pulse Generator for TDDB Characterization on a Sub-nanosecond Timescale," M. Drallmeier, et. al., Univ. of Illinois, Presents an on-chip pulse generator fabricated in a 65-nm CMOS process capable of producing clean single-shot pulses with amplitude up to 6 V and pulse width as short as 200 ps. Experimentally investigates use of pulse generator on MOS gate oxide breakdown voltage on a sub-ns timescale and to assess the validity of the power-law model.
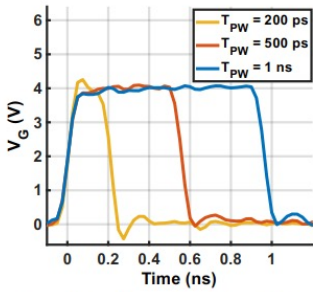
Figure 7: Measured V_G pulses for the 200-ps, 500-ps, and 1-ns pulse generators.
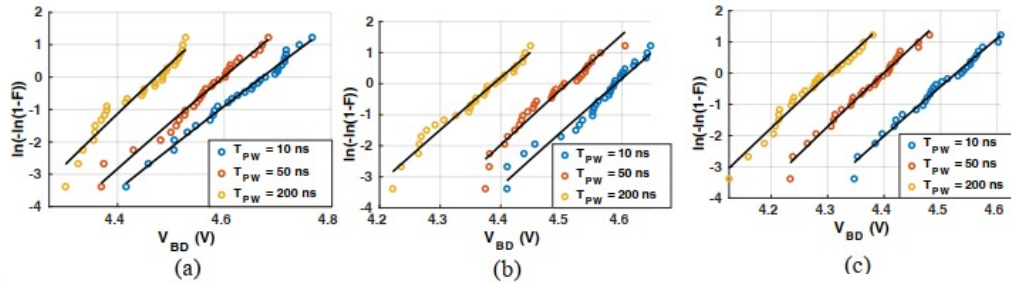
Figure 12: Weibit vs. V_{BD} measured using direct vf-TLP. Victim devices are the same as for Fig. 11.

Late news (Transistor Session)

7B.5 "Modeling of Negative Bias Temperature Instability (NBTI) for Gate-all-around (GAA) Stacked Nanosheet Technology," J. Fang, et. al., Synopsys, Implements a physics-based NBTI framework involving trap generation and trapping, validates against measured data, investigated the impact of nanosheet thickness, channel stress and SiGe channel on GAA characteristics, demonstrates a TCAD to SPICE framework
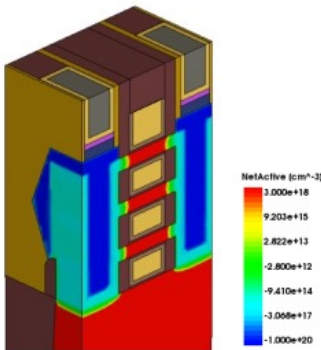

Figure 2 Three-dimensional model GAA p-type transistor with 3 nanosheets. The source and drain epitaxy regions are highly p-type doped. The channel is assumed to be lightly n-type doped. The sub-fin is assumed to be n-type doped to minimize source-to-drain leakage.
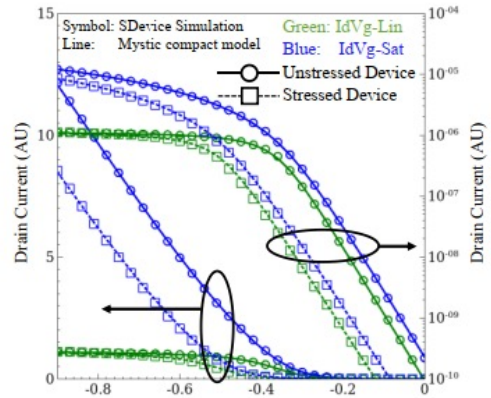
Figure 12. Comparison of unstressed and stressed GAA PMOS device characteristics generated with TCAD simulation and Mystic compact model. After calibration, the electrical characteristics generated by Mystic compact model aligns very well with physics based TCAD simulation.

Late news (Gate/MOL Dielectrics)

8C.4 "On-Chip Single-Shot Pulse Generator for TDDB Characterization on a Sub-nanosecond Timescale," M. Drallmeier, et. al., Univ. of Illinois, performed a thermal analysis of a server SoC considering a realistic layer stack configuration mounted on a printed circuit board (PCB) with an active heat sink for the cooling solution and proposes a holistic co-optimization of the thermal interface material, cooling solution and SoC design.
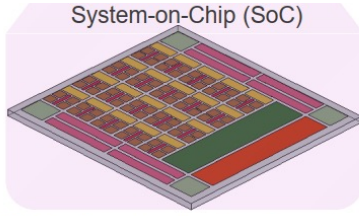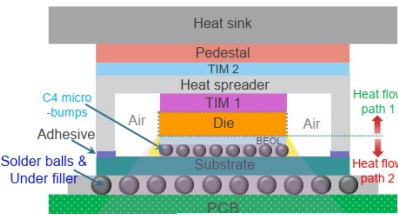

Figure 1. 2D cross-sectional view of the SoC packaging to the cooling solution. Convection boundary conditions in terms of HTC are used on the top of the heat sink and the bottom of the PCB. The side surfaces of the heat spreader are assumed to be adiabatic conditions.
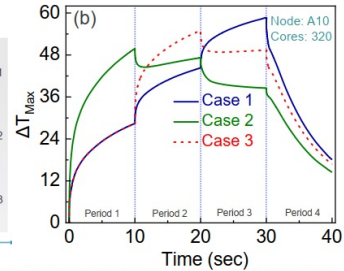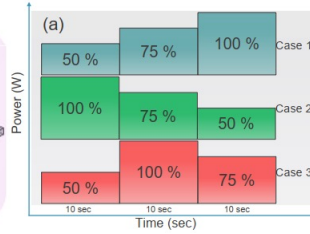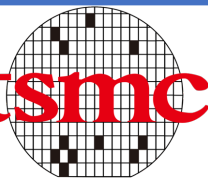
Figure 15. Variation of maximum temperature (ΔT_{Max}) with respect to time for multiple cases of 50% to 100% power workload variations.