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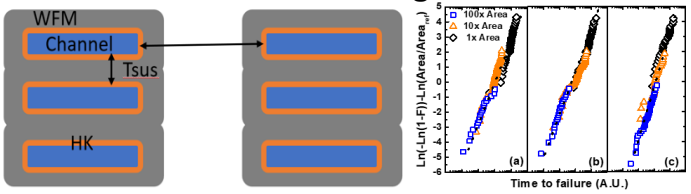
Highlight Paper 1

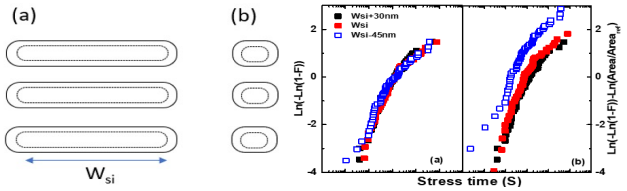
Gate/MOL Session

2A.1 "Challenges of gate stack TDDB in gate-all-around nanosheet towards further scaling" H. Zhou et al., IBM Research, presents GAA features and impact on TDDB reliability: Multi-VT integration, WSI and area scaling, spacer, Tsi.

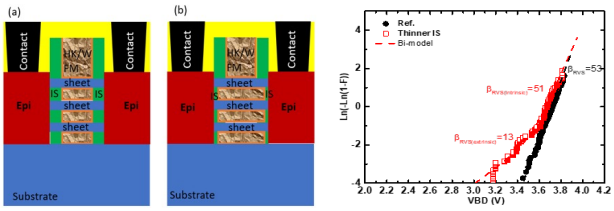
Multi Vt and Integration



Wsi and Area Scaling



Inner Spacer and Bi-model



Tsi and TDDB

(b)

Items	VAE	β
T_{Si}-1 nm	56	0.7
T_{Si}	61	0.8
T_{Si}+1nm	60	0.9

Gate/MOL Session

9A.2 "Joint Weibull-Fréchet model for dielectric breakdown in filament formation including reverse area scaling" E. Wu et al, IBM Research, presents a statistics-based model "Join Weibull-Fréchet" to characterize reverse area-scaling of RRAM TBD, and enabling reliability projection from test area to chip/product area.

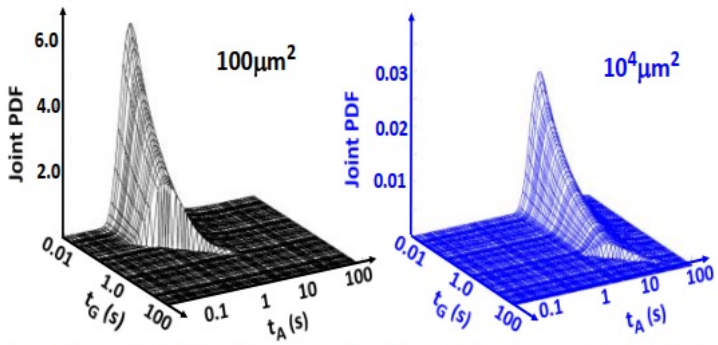
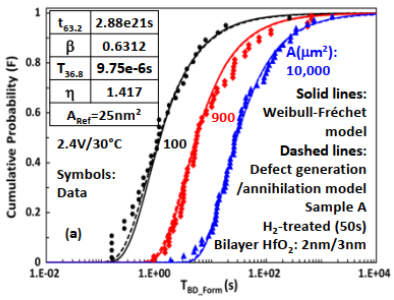
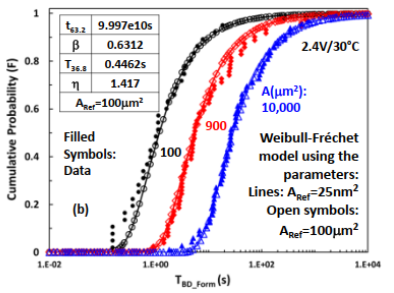


Fig. 3. The joint PDF (Eq. 5) of the Weibull-Fréchet model for 100 and $10^4\mu m^2$ using the parameters in Fig. 5 (a)





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Highlight Paper 2

Transistor Session

4A.1 "Fundamental understanding of NBTI degradation mechanism in IGZO channel devices" Y. Zhao, et. al., KU Leuven, presents a comprehensive understanding of NBTI in IGZO TFTs with varying channel thickness and gate length.

Negative shifts are enhanced for thicker IGZO films

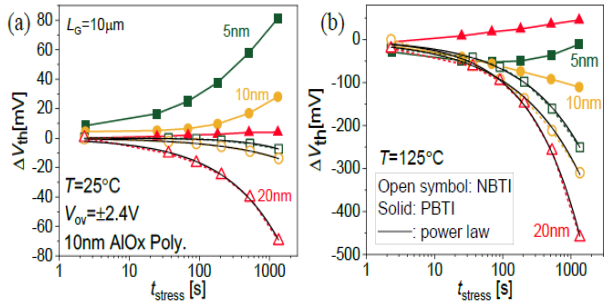

Fig.2 ΔV_{th} as function of stress time (time kinetics) of NBTI (open symbols) and PBTI (solid) under T=25°C (a) and 125°C (b). NBTI increases for thicker IGZO films. At 125C, NBTI is more pronounced than PBTI. All the NBTI curves can be fitted by power laws (black lines), see Eq. (1).

Shorter gate length → enhanced Vg stress

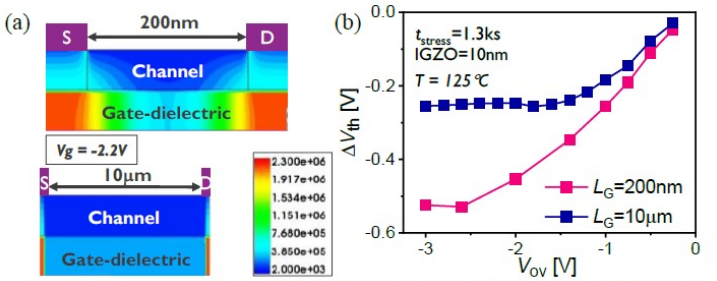

Fig. 6 (a) 2D distribution of electric field in short(upper) and long(lower) devices, showing higher E_{ox} in the regions under S/D. The shorter device experiences increased E_{ox} in the center of the channel due to larger impact from the regions under S/D. (b) Voltage dependence of ΔV_{th} at t_{stress}=1.3ks for short and long devices. The shorter device shows larger degradation and stronger voltage dependence.

GaN Device Session

6B.1 "PBTI in Scaled Oxide Submicron Enhancement Mode High-K Gallium Nitride Transistors," S. Joy, et. al., Intel, presents E-mode HEMT with 2nm Hf-based dielectric (high-k) in Fabricated on 300 mm GaN-on-Si wafer

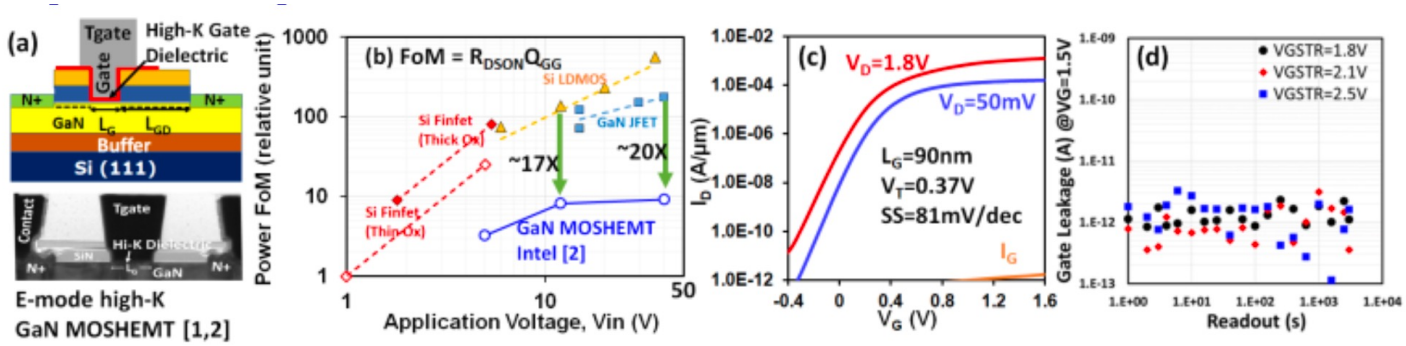

Figure 1. (a) Schematic and TEM of gate-recessed, high-k E-mode GaN MOSHEMT in this work; (b) reported Power FoM ($R_{DSON}Q_{GG}$) of Intel GaN MOSHEMT [2]. (c) I_D-V_G of L_g=90nm GaN MOSHEMT showing ON/OFF ratio>10^8, SS~80mV/dec, and I_G<5pA/μm (d) no prominent increase in I_G during PBTI measurements.

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Highlight Paper 3

Radiation Effect Reliability Session

10C.1 "Soft-Error Sensitivity in SRAM of 3 nm Gate-All-Around (GAA) Technology" T. Uemura, et. al., Samsung Electronics, presents Alpha- and neutron-SERs in SRAMs manufactured with 3 nm bulk gate-all-around (bulk-GAA) process technology. The SER in SRAM of bulk-GAA is maximally 1.56X higher than in the same cell-size SRAM of bulk-FinFET. Moreover, shrinking cell size decreases the SER by a maximum of 0.38X in bulk-GAA. The SER of the minimum-size SRAM in bulk-GAA is lower than in bulk-FinFET.

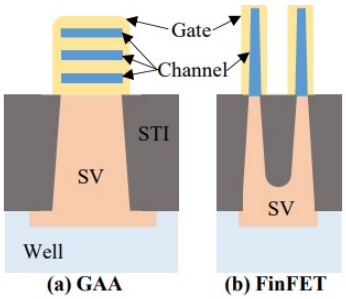

Fig. 6 The cross-section image of Y-cut (**Fig. 4(a)**) in (a) bulk-GAA and (b) bulk-FinFET transistors. The sensitive volume (SV) in bulk-GAA is larger than in bulk-FinFET.

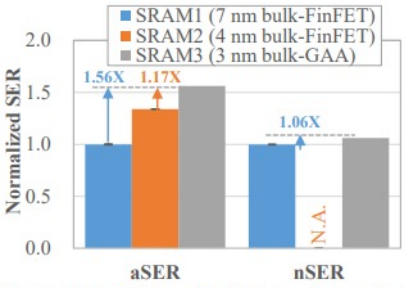

Fig. 2 The aSER and nSER at the nominal voltage (0.75V in all the SRAM) in FinFET SRAMs (SRAM1 and SRAM2) and GAA SRAMs (SRAM3). The cell size is identical in SRAM1, 2, and 3 (**Table I** and **Fig. 1**).

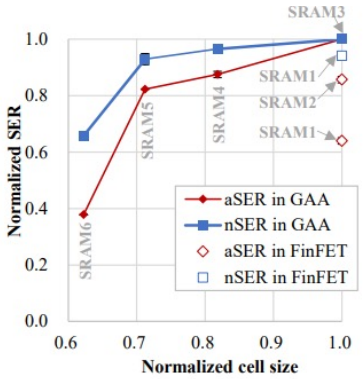

Fig. 7 Normalized aSER and nSER as a function of the cell size in the SRAMs.

ESD&Latch-up Session

8C.1 "Insight into Latchup Risk in 28nm Planar Bulk Technology for Quantum Computing Applications" K. Servulova, et. al., imec. A Cryogenic environment is needed for quantum computing and a latch-up property will be changed. This paper presents well defined experiment and interpretation, and the current gain characterization of the parasitic bipolar transistors over wide temperature range is a valuable reference for future work

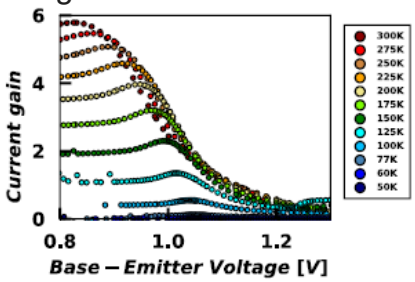

Figure 10: Simulation results of NPN β-gain in advanced planar technology at temperatures from 300 K to 30 K.

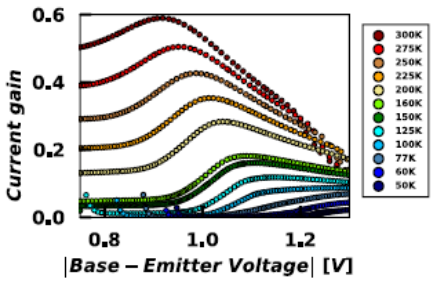

Figure 11: Simulation results of PNP β-gain in advanced planar technology at temperatures from 300 K to 30 K.

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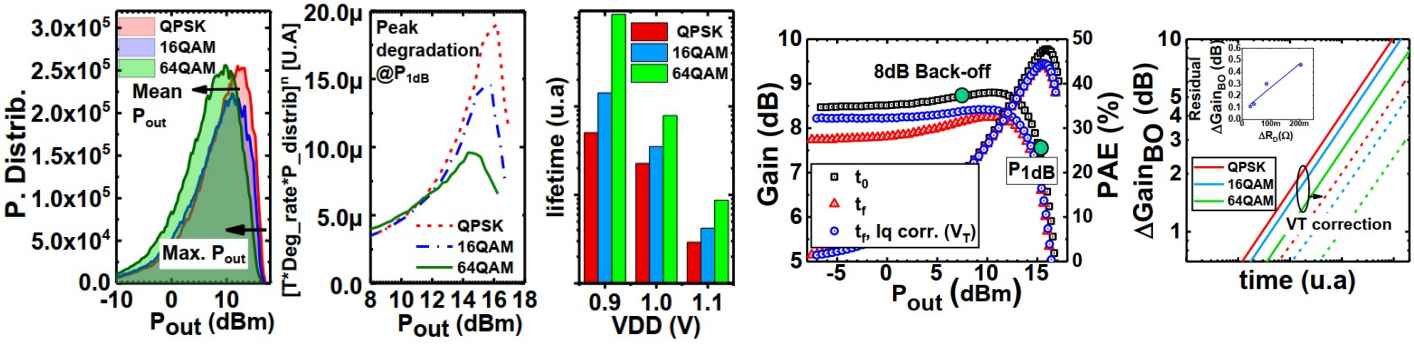
Highlight Paper 4

RF/mmW/5G Session

4B.2 "A Methodology to address RF aging of 40nm CMOS PA cells under 5G mmW modulation profiles," A. Divay, et. al, cea, presents a simplified methodology to link CW RF stresses to complex profiles, and Improved lifetime for most complex 5G modulation due to output power/linearity constraints



RF/mmW/5G Session

4B.1 "DC Reliability study of high-k GaN-on-Si MOSHEMTs for mm-Wave Power Amplifiers" B. O'Sullivan, et. al.,imec, presents High-k GaN-on-Si MOSHEMTS for mm-Wave Power Amplifiers monolithically integrated on 200 mm Si substrates. Defects in HfO2 or Al2O3 result in significant Vt instabilities, with dielectric-dependent charge emission kinetics: band alignment between high-k shallow defect levels and AlGaN conduction band enables full (Al2O3) or partial (HfO2) charge de-trapping

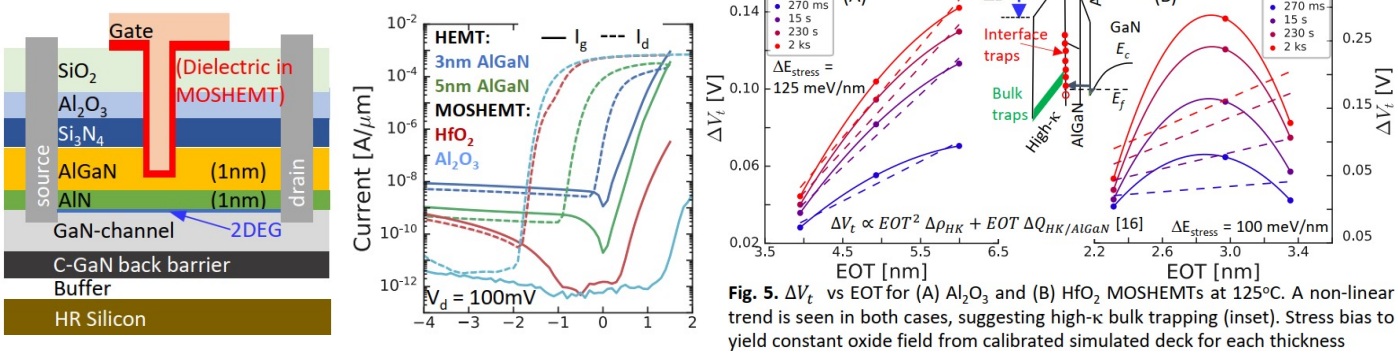


Fig. 5. ΔV_t vs EOT for (A) Al_2O_3 and (B) HfO_2 MOSHEMTs at 125°C. A non-linear trend is seen in both cases, suggesting high-κ bulk trapping (inset). Stress bias to yield constant oxide field from calibrated simulated deck for each thickness

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Highlight Paper 5

Circuit Reliability Session

4C.1 "Demonstration of Chip Overclock Detection by Employing Tamper-aware Odometer Technology," R. J. Diaz-Fortuny, et. al., imec, proposes a significant improvement of the tamper-aware odometer concept to obtain the degradation of a chip utilizing enhanced ring-oscillators-based degradation monitors . The authors present two new aging odometers designed in 28nm tech that, together with clear and concise data, allows avoiding the need of a pre-stres phase to obtain the age of a chip based on individual BTI and HCD RO readings. With the presented technology, the authors can unequivocally detect a previous overclock test to conducted intentionally to the chip's digital circuitry.

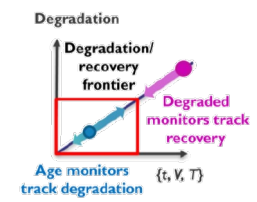

Fig. 1. Tamper-aware odometer concept where two sets of odometers are deployed: one non-degraded set (blue oval) for chip age determination, and a second set highly pre-stressed during production (pink oval) for tamper-awareness. Through chip lifetime, the age monitors track wear-out while the degraded monitors track recovery to detect fraudulent IC anneal.

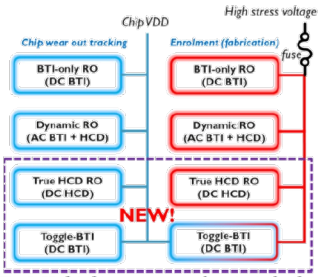

Fig. 2. Updated tamper-aware odometer technology with two new RO designs: the true-HCD RO, an enhanced version of our previous eHCD RO [8], and the toggle-BTI RO that allows having different RO degradation kinetics in a single RO design.

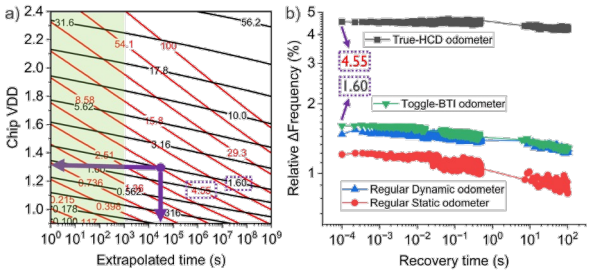

Fig. 9. (a) shows the modelled degradation data of the True-HCD (red isolines) and the Toggle-BTI (black isolines). The green section determines the new data space used in this work, i.e., as from 0.9 V, while in our previous works [8-9], the degradation maps were obtained as from 1.8 V. In (b), the 4 odometers full recovery traces are shown and, by selecting the corresponding isolines matching the first recovery values of the True-HCD (ΔFreq(%) = 4.55) and the Toggle-BTI (ΔFreq(%) = 1.60), we unequivocally unveil that the chip has been overclocked for ~12 h at a VDD of 1.3V (purple arrows), at their intersection.

System Electronics Session

5C.3 "Virtual FA methodology for DRAM: Real-time analysis and prediction method using Telemetry, Field data," J. Lee, et. al, Samsung Electronics, presents Fast methodology of failure detection in deployed systems compared to conventional failure analysis flow. The paper describes a methodology that is widely conceptualized but in practice is hard to implement. The authors were successful in providing examples of failure modes that are classifiable on a database and are able to be resolved and confirmed through collaboration with customers. Both these elements are key to the success of this vFA methodology.

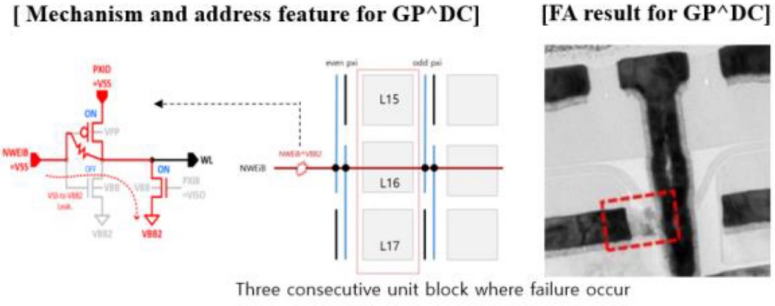

Fig.2: Address feature for GP^DC: When a defect occurs in a NEWiB^VBB2 node, the GP^DC failure occurs in three consecutive unit blocks that share NWEiB and PXi. [3]

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Highlight Paper 6

Failure Analysis Session

10B.1 "**Laboratory X-Ray-Assisted Device Alteration for Fault Isolation and Post-Silicon Debug,"** K. Celio, et. al., intel, present new fault isolation technique and post-silicon debug for backside power delivery networks and multi-die stacking devices.

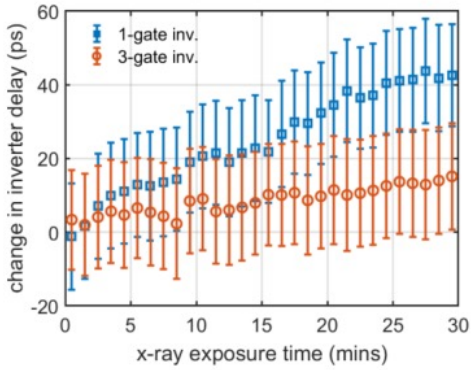

Figure 3. *Observed change in single CMOS inverter delays with x-ray exposure time. X-ray beam size and circuit layout enable overlap of ray with only 1 inverter in the inverter chain. Data shown for x-ra perturbation of both a 1-gate and a 3-gate inverter. Errorbars sho +/- standard deviaion in measured delay.*

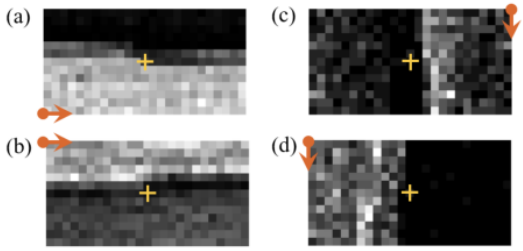

Figure 4. *Demonstration of XADA localization of a physical defect in an SRAM circuit. Defect location is notated by a cross, and x-ray scan directions are notated by arrows. DUT is operated near failing voltage in a looping test pattern fashon, and the number of failing tests per pixel in the XADA raster are plotted, with white pixels corresponding to more failing tests, and black pixels to less. The XADA raster area is 60x30 µm, the pixel size is 2.4 µm, the dwell time is 1 s/px, and the x-ray beam diameter is ~4.7 µm. X-ray rasters in different directions (a-d) each observe a change in the number of failing tests near the defect location, with the x-ray beam interaction causing a decrease in the number of failing tests (an improvement in V_{min}).*

Reliability Testing Session

2B.1 "Modeling Dark Current Degradation of Monolithic InGaAs/GaAs-On-Si Nano-Ridge Photodetectors," P. Hsieh, et. al., imec, thoroughly investigated dark current conduction mechanisms and degradation. The proposed semiempirical carrier emission/capture model successfully portrays the degradation and recovery, therefore enabling acceleration factor and device lifetime estimation, providing a more precise vision toward defect kinetics.

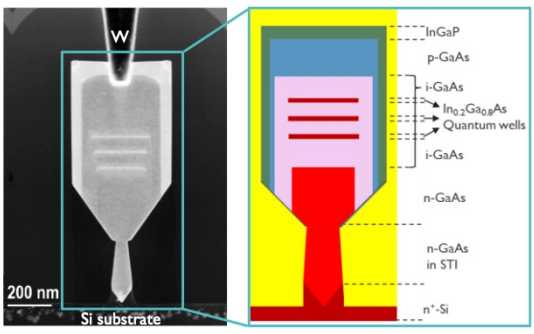

Figure 1. The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the InGaAs/GaAs nano-ridge p-i-n photodetectors. Detailed layer stacks are shown in the zoom-in schematic.

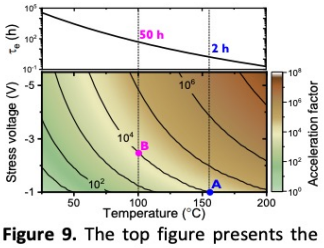

Figure 9. The top figure presents the emission time constant as a function of the temperature, and the contour map below calculated the acceleration factor (AF) at various voltages and temperatures ($T_{ref.}$ = 25 °C, $V_{ref.}$ = -1 V). A and B are equivalent stress conditions with AF = 10^4.

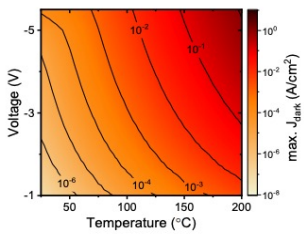

Figure 10. Estimated max. I_{dark} degradation (at V_{sense} = -1 V) in device operating life under various stress conditions, based on the comprehensive model developed in this work.

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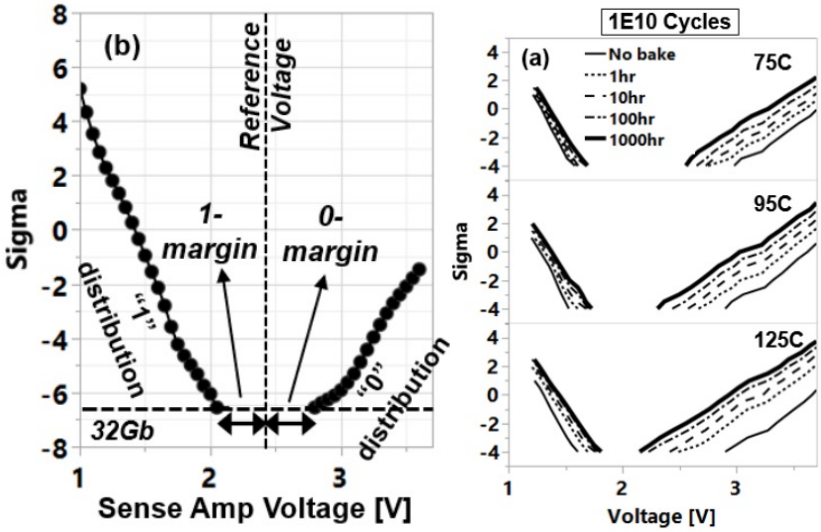
Highlight Paper 7

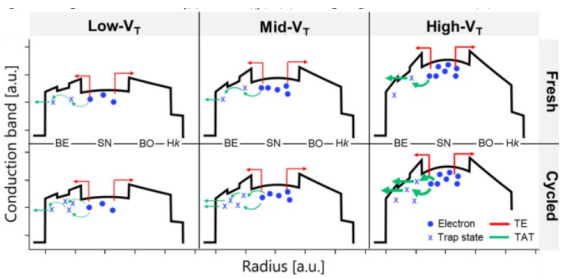
Emerging Memory Session

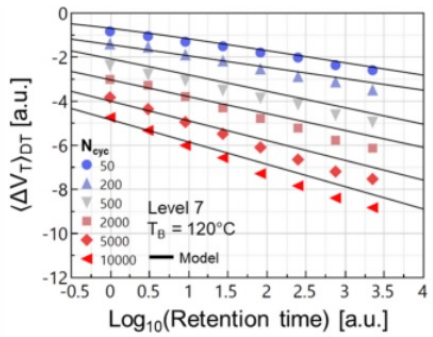
7A.4 "Comprehensive Reliability Assessment of 32Gb HfZrOx-Based Ferroelectric NVDRAM Memory," D. Ettisserry, et. al., Micron, presents array level HZO ferroelectric, and describes new reliability mechanisms.

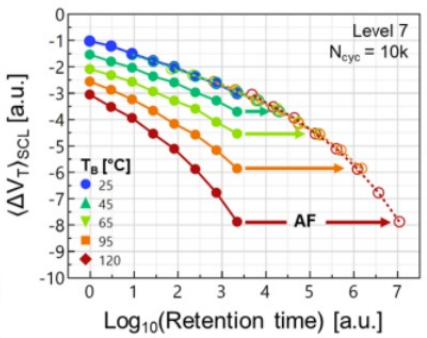


Memory Reliability Session

3A.2 "Experimental Segmentation of Vertical Charge Loss Mechanisms in Charge Trap-Based 3D NAND Arrays," L. Chiavarone, et. al., Micron, presents that vertical charge loss in charge trap 3D NAND arrays is characterized and modeled. The contributions of charge de-trapping from bandgap-engineered tunnel stack and charge loss from silicon nitride storage node are experimentally separated for the first time.







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Highlight Paper 8

Late news (Gate/MOL Dielectrics)

7B.4 "On-Chip Single-Shot Pulse Generator for TDDB Characterization on a Sub-nanosecond Timescale," M. Drallmeier, et. al., Univ. of Illinois, Presents an on-chip pulse generator fabricated in a 65-nm CMOS process capable of producing clean single-shot pulses with amplitude up to 6 V and pulse width as short as 200 ps. Experimentally investigates use of pulse generator on MOS gate oxide breakdown voltage on a sub-ns timescale and to assess the validity of the power-law model.

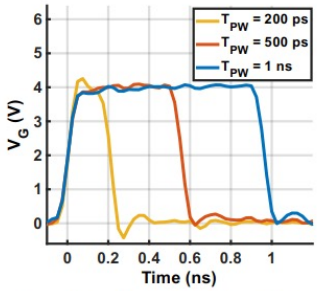

Figure 7: Measured V_G pulses for the 200-ps, 500-ps, and 1-ns pulse generators.

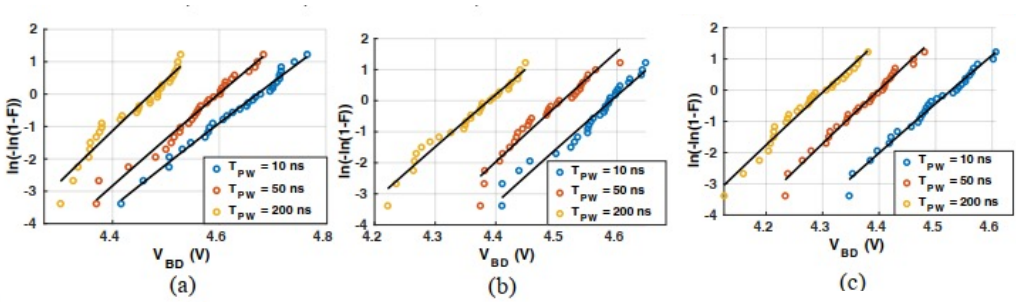

Figure 12: Weibit vs. V_{BD} measured using direct vf-TLP. Victim devices are the same as for Fig. 11.

Late news (Transistor Session)

7B.5 "Modeling of Negative Bias Temperature Instability (NBTI) for Gate-all-around (GAA) Stacked Nanosheet Technology," J. Fang, et. al., Synopsys, Implements a physics-based NBTI framework involving trap generation and trapping, validates against measured data, investigated the impact of nanosheet thickness, channel stress and SiGe channel on GAA characteristics, demonstrates a TCAD to SPICE framework

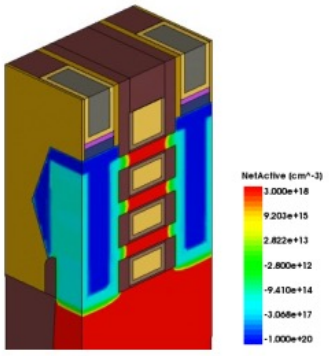

Figure 2 Three-dimensional model GAA p-type transistor with 3 nanosheets. The source and drain epitaxy regions are highly p-type doped. The channel is assumed to be lightly n-type doped. The sub-fin is assumed to be n-type doped to minimize source-to-drain leakage.

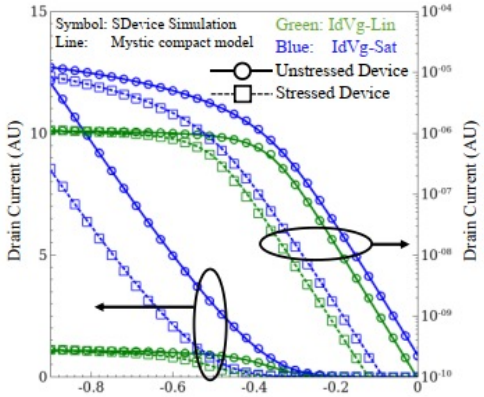

Figure 12. Comparison of unstressed and stressed GAA PMOS device characteristics generated with TCAD simulation and Mystic compact model. After calibration, the electrical characteristics generated by Mystic compact model aligns very well with physics based TCAD simulation.

Late news (Gate/MOL Dielectrics)

8C.4 "On-Chip Single-Shot Pulse Generator for TDDB Characterization on a Sub-nanosecond Timescale," M. Drallmeier, et. al., Univ. of Illinois, performed a thermal analysis of a server SoC considering a realistic layer stack configuration mounted on a printed circuit board (PCB) with an active heat sink for the cooling solution and proposes a holistic co-optimization of the thermal interface material, cooling solution and SoC design.

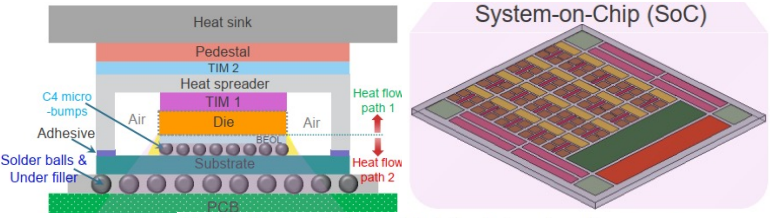

Figure 1. 2D cross-sectional view of the SoC packaging to the cooling solution. Convection boundary conditions in terms of HTC are used on the top of the heat sink and the bottom of the PCB. The side surfaces of the heat spreader are assumed to be adiabatic conditions.

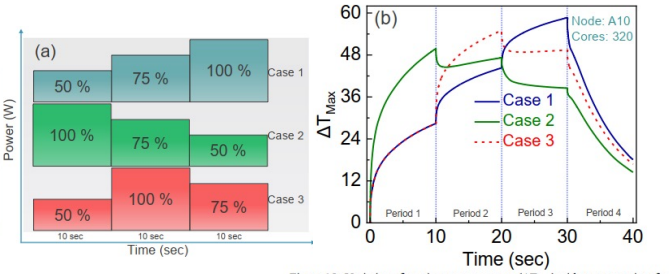

Figure 15. Variation of maximum temperature (ΔT_{Max}) with respect to time for multiple cases of 50% to 100% power workload variations.