IRPS
International Reliability Physics Symposium

2021 IEEE International Reliability Physics Symposium (IRPS)

Virtual Conference
21 March – 24 March 2021

2021 IEEE International Reliability Physics Symposium (IRPS 2021)

Sunday, March 21

Welcome & IRPS Introduction
Sunday, March 21, 8:00 a.m. – 8:35 a.m. PDT
Robert Kaplar, Sandia National Labs
Chris Connor, Intel
Charlie Slayman, Cisco Systems
Venue: Monterey Main Stage

Keynote 1
Sunday, March 21, 08:35 a.m. – 09:20 a.m. PDT
Robert Kaplar, Sandia National Labs
Chris Connor, Intel
Venue: Monterey Main Stage

08:35 a.m.
KN1 (Keynote) - Memory's Journey Towards the Future Information and Communications Technology (ICT) World, Seok-Hee Lee, CEO SK hynix

With the acceleration of digital transformation under the fourth industrial revolution, the COVID-19 pandemic has completely changed our daily lives, giving rise to digital healthcare, remote learning/conferencing, to name a few. Such transformation, along with the integration of AI and 5G network, is likely to help create new values from a vast pool of data, and is likely to lead us towards an era of information, communication, and technology, where large amounts of information are delivered with unprecedented speed and accuracy. To enable such transformation, increasingly high speed, low power, high capacity, and high reliability memory semiconductors are required. Within the memory semiconductor industry, we have continued to overcome the technological challenges of DRAM scaling and NAND flash stacking by making continuous improvements. However, the pace of semiconductor technology development is yet to catch up with the rate at which data is produced, which necessitates still more innovative semiconductor technologies to handle the explosive growth in data. In this speech, I would like to introduce SK Hynix's journey towards future technological advancement. Also, I would like to suggest finding solutions to problems together through the collaboration among the industry/academia/research, with a goal of making a better world with information and communications technologies (ICT) through sharing rather than through competition.

2A – GD (Gate/MOL Dielectrics)
Sunday, March 21, 09:20 a.m. – 11:30 a.m. PDT
Francesco Maria Puglisi, Università di Modena e Reggio Emilia
Andrea Padovani, Applied Materials
Venue: Big Sur

2A – Intro
09:20 a.m. – 09:25 a.m. PDT

09:25 a.m.
2A.1 (ESREF) - Assessing the Pre-Breakdown Carriers' Multiplication in SiC Power MOSFETs by Soft Gamma Radiation and its Correlation to the Terrestrial Cosmic Rays Failure Rate Data as Measured by Neutron Irradiation, Mauro Ciappa, Marco Pocaterra, ETH Zurich

The susceptibility to terrestrial cosmic rays (TCR) of power devices is strongly correlated to the peak of the local electric field, thus to the resulting local carriers' multiplication. In this paper, the soft gamma radiation from an Am^{241} source is used to characterize the pre-breakdown carriers' multiplication in SiC MOSFETs as a function of the applied blocking bias. The resulting multiplication levels are then compared to TCR failure rate literature data assessed by neutron irradiation.

09:50 a.m.
2A.2 - Characterization of Slow Traps in SiGe MOS Interfaces by TiN/Y_2O_3 Gate Stacks, T.-E. Lee*, K. Toprasertpong, M. Takenaka, S. Takagi, The University of Tokyo

We have examined the slow electron and hole trap density at TiN/Y_2O_3/SiGe MOS interfaces. The effect of trimethylaluminum (TMA) pre-treatment before Y_2O_3 deposition on the slow trap density has been studied. Also, the dependency of the slow trap density on Ge contents of SiGe has been systematically evaluated and the influence of the composition of interfacial layers (ILs) is examined. It is found that 10-cycle TMA treatment is effective to suppress the formation of slow traps attributable to Ge-O bonds in ILs. On the other hand, the density of electron and hole slow traps in the Y_2O_3/SiGe MOS interfaces increases with higher Ge content of SiGe, which can be explained by the formation of vacancy-related defects due to incorporation of Ge-O bonds into SiO_2 IL networks.

10:15 a.m.
2A.3 - Off-State TDDB in FinFET Technology and its Implication for Safe Operating Area, M. Toledano-Luque, P. Paliwoda, M. Nour, T. Kauerauf, B. Min, G. Bossu, M. Siddabathula, Fab 1 Reliability, T. Nigam, GlobalFoundries

Standard CMOS reliability has been focused on digital applications and the user profiles associated with these products. However, emerging applications in mobility, automotive, communication networks and data centers require additional, more rigorous reliability specifications. For these applications, the devices operate beyond the typical safe operation area (SOA) mostly because large drain biases are applied during the normal operation. In this situation, off-state TDDB could be a concern and it must be considered during product design. In this study, we present the models to describe off-state TDDB and the methodology to accurately predict the SOA for circuits under standard operation condition in field. The presented SOA approach relaxed the stringent reliability requirements defined on DC operation, reducing design overhead, and developing and verification costs.

10:40 a.m.
2A.4 - Drastic Reliability Improvement using H_2O_2/UV Treatment of HfO_2 for Heterogeneous Integration, S.M. Kim[12], T.M.H. Nyugen[3], J.W. Oh[3], Y.S. Lee[12], S C. Kang[4], H.I. Lee[12], C.H. Kim[12], S. Some[12], H.J. Hwang[12], B.H. Lee[12]*, [1]Center for Semiconductor Technology Convergence, [2]Pohang

University of Science and Technology (POSTECH), [3]Gwangju Institute of Science and Technology (GIST), [4]Electronics and Telecommunications Research Institute (ETRI)

For heterogeneous integration, the heat cycle constraint limits the available number of options for the process of fabricating high-quality reliable high-k dielectrics, for example, post-deposition annealing and high-temperature deposition. To solve this problem, we examine the effects of H_2O_2/UV treatment on the reliability characteristics of low-temperature-grown HfO_2 via atomic layer deposition, wherein it is treated with a minimal post-deposition heat cycle. The leakage current and time zero dielectric breakdown characteristics of the H_2O_2/UV-treated HfO_2 are drastically improved without having applied the post-deposition heat cycle, compared with those of the control group that undergoes O_2 post-deposition annealing. The proposed process is a promising method to improve the quality of dielectrics for heterogeneous integration.

11:05 a.m.
2A.5 - Modeling of HKMG Stack Process Impact on Gate Leakage, SILC and PBTI, Dimple Kochar, Tarun Samadder, Subhadeep Mukhopadhyay, Souvik Mahapatra, Department of Electrical Engineering Indian Institute of Technology Bombay (IIT Bombay)

Gate stack process (pre-clean, IL, IL/HK interface, HK, post-HK Nitridation) impact on gate leakage, SILC and PBTI is analyzed. IL and HK thickness, channel/IL and IL/HK energy-barrier offsets impact on gate leakage and SILC response from generated bulk traps inside IL and HK is quantified. Time kinetics of generated IL and HK bulk traps for SILC, and IL/HK interface traps for PBTI are simulated by a generic Reaction-Diffusion-Drift (RDD) framework. Model is validated using measurements from differently processed HKMG stacks.

2A – Authors' Corner
11:30 a.m. – 12:00 p.m. PDT

2B – GaN (Wide-Bandgap Semiconductors - GaN)
Sunday, March 21, 09:20 a.m. – 11:30 a.m. PDT
Kaustubh Joshi, Intel Corporation
Luca Perniola, CEA/LETI
Venue: Carmel

2B – Intro
09:20 a.m. – 9:25 a.m. PDT

09:25 a.m.
2B.1 (Invited) - Progress and Current Topics of JEDEC JC-70.1 Power GaN Device Quality and Reliability Standards Activity Or: What is the Avalanche Capability of Your GaN Transistor?, Infineon, Chair, JEDEC JC-70.1, Stephanie Watts Butler, Texas Instruments, Chair, JEDEC JC-70

"What is the avalanche (UIS or undamped inductive switching) capability of a GaN based power transistor?" is a question that is commonly posed in supplier / customer interactions today. The history, motivation and use of this rating (as applied to silicon based power MOSFETs) will be reviewed and its suitability for use with GaN based power HEMTs considered. UIS testing methods and standards are shown not to be a relevant gage of application robustness for GaN based power devices. Thus, for GaN devices, a gap exists between designer needs and existing industry standards. The state of supplier ratings to meet the gap is briefly highlighted and demonstrates why JEDEC subcommittee JC-70.1 should create relevant new standards for GaN overvoltage/ surge robustness. Finally, a brief review of overall JEDEC JC-70.1 scope, structure, process, and progress is provided.

09:50 a.m.
2B.2 - Failure Mechanisms of Cascode GaN HEMTs under Overvoltage and Surge Energy, Qihao Song*, Ruizhe Zhang, Joseph P. Kozak, Jingcun Liu, Qiang Li Yuhao Zhang*, Virginia Polytechnic Institute and State University

This work, for the first time, studies the surge-energy robustness and failure mechanisms of 650-V rated cascode GaN HEMTs in the unclamped inductive switching (UIS) tests. Different from the p-GaN HEMT which has a purely electric failure, two failure modes were observed, both occurring in the GaN HEMT. The cascode HEMT failure can be either electrically induced or thermally related. A preliminary explanation was proposed for the failure mechanisms under different load inductance.

10:15 a.m.
2B.3 - Vertical Stack Reliability of GaN-on-Si Buffers for Low-Voltage Applications, E. Fabris, M. Borga, N. Posthuma, M. Zhao, B. De Jaeger, S. You, S. Decoutere, imec, M. Meneghini, G. Meneghesso, E. Zanoni, University of Padova

In this paper the reliability of the vertical GaN-on-Si stack for lateral p-GaN HEMTs dedicated to low-voltage applications is discussed in detail by comparing wafers with different buffer thicknesses and growth condition of the AlN nucleation layer. The vertical robustness and the time-dependent vertical breakdown will be investigated in detail, demonstrating that the buffers with reduced thickness are suitable for 100 V applications. Moreover, the voltage drop on the different layers of the vertical stack will be extracted at the breakdown, and a model able to explain the degradation of the vertical stack will be proposed.

10:40 a.m.
2B.4 - A Generalized Approach to Determine the Switching Reliability of GaN HEMTs on-Wafer Level, Nicola Modolo[1], Andrea Minetto[2], Carlo De Santi[1], Luca Sayadi[1], Sebastien Sicre[2], Gerhard Prechtl[2], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Matteo Meneghini[1], 1. University of Padova, 2. Infineon Technologies Austria

A detailed analysis of the turn-on behavior of E-mode p-GaN HEMT is reported. A novel system has been developed to investigate the impact of hard-switching stress in terms of dynamic on-resistance, turn-on switching locus, and power dissipation. The novelty of our approach comes from the high speed of the turn-on commutations (in the range of 10 V/ns), enabling a realistic assessment of the power device performances before the packaging-level, thus shortening the technological development loop.

11:05 a.m.
2B.5 - Study on the Difference between $I_D(V_G)$ and $C(V_G)$ pBTI Shifts in GaN-on-Si E-Mode MOSc-HEMT, A.G. Viey, W. Vandendaele, M.-A. Jaud, J. Coignus, J. Cluzel, A. Krakovinsky, S. Martin, J. Biscarrat, R. Gwoziecki, V. Sousa, F. Gaillard, University Grenoble-Alpes, R. Modica, F. Iucolano, Research and Development Department STMicroelectronics, M. Meneghini, G. Meneghesso, University of Padova Via Gradenigo 6/B, G. Ghibaudo, IMEP-LAHC MINATEC University Grenoble-Alpes

In this paper, we investigate the difference between $I_D(V_G)$ and $C(V_G)$ pBTI shifts on GaN-on-Si E-mode MOS-channel HEMTs, under various gate voltage stresses $V_{GStress}$ and temperatures T. A new experimental setup using ultra-fast simultaneous $I_D(V_G)$ and $C(V_G)$ enables to monitor V_{TH} drift through two metrics, ΔV_{THI} and ΔV_{THC}. TCAD simulations supports that $I_D(V_G)$ shift (ΔV_{THI}) is related to charge trapping at the gate corners regions, while $C(V_G)$ shift (ΔV_{THC}) is ascribed to the gate bottom.

2B – Authors' Corner
11:30 a.m. – 12:00 p.m. PDT

2C – NC (Neuromorphic Computing Reliability)
Sunday, March 21, 09:20 a.m. – 11:30 a.m. PDT
Stefano Ambrogio, IBM Research – Almaden
Venue: Pebble Beach

2C - Intro
09:20 a.m. – 09:25 p.m. PDT

09:25 a.m.
2C.1 (Focus) - Conductance Variations and their Impact on the Precision of in-Memory Computing with Resistive Switching Memory (RRAM), Giacomo Pedretti[1], Elia Ambrosi[1], Daniele Ielmini[1]*, [1]Politecnico di Milano and IU.NET

This work addresses the reliability of RRAM, with a focus on conductance variation and its impact on in-memory computing (IMC). The core advantage of IMC is the ability to execute matrix-vector multiplication (MVM) in one step in crosspoint memory arrays, which can significantly accelerate data-intensive computing tasks, such as the inference and training of deep neural networks (DNNs). Since MVM is executed in the analogue domain, the imprecision of weight parameters stored in the memory array can result in errors which can affect the accuracy of the computation. By referring to a typical IMC device, that is the resistive switching memory (RRAM), we describe the conductance variations and stability with time, high-lighting their impact on IMC accuracy. Then we discuss various options for mapping coefficients in the memory device, including multilevel, binary, unary, redundancy and slicing schemes, and their robustness with respect to conductance errors. It turns out that a tradeoff exists between accuracy and memory area occupation in the IMC circuit. Accurate IMC circuits thus must rely on the co-design of highly-precise, highly-stable devices and error tolerant mapping/computing schemes.

09:50 a.m.
2C.2 (Focus) - Embedded Emerging Memory Technologies for Neuromorphic Computing: Temperature Instability and Reliability, Yao-Feng Chang[1], Ilya Karpov[1], Reed Hopkins[2], David Janosky[2], Jacob Medeiros[2], Benjamin Sherrill[2], Jiahan Zhang[2], Yifu Huang[2], Tanmoy Pramanik[1], Albert Chen[1], Tony Acosta[1], Abdullah Guler[1], James A. O'Donnell[1], Pedro A Quintero[1], Nathan Strutt[1], Oleg Golonzka[1], Chris Connor[1], Jack C Lee[2], Jeffrey Hicks[1], 1. Intel Corporation, 2. The University of Texas at Austin

The impact of temperature instability of resistive memory switching on potential neuromorphic computing applications has been extensively studied using eNVM-R and eNVM-M technologies developed on Intel 22FFL process. The reliability risk assessment shows that the effects of ambient temperature (e.g. resistance or conductance shifting with varying temperature) can lead to potential degradation of the neural network accuracy. Our results provide additional insight into device-level physical models and circuit-level design guidance for potential AI hardware applications.

10:15 a.m.
2C.3 - Characterization and Mitigation of Relaxation Effects on Multi-level RRAM Based in-Memory Computing, Wangxin He[1], Wonbo Shim[2], Shihui Yin[1], Xiaoyu Sun[2], Deliang Fan[1], Shimeng Yu[2], Jae-sun Seo[1, 1]Arizona State University, [2]Georgia Institute of Technology

In this paper, we investigate the relaxation effects on multi-level resistive random access memory (RRAM) based in-memory computing (IMC) for deep neural network (DNN) inference. We characterized 2-bit-per-cell RRAM IMC prototypes and measured the relaxation effects over 100 hours on multiple 8 kb test chips, where the relaxation is found to be most severe in the two intermediate states. We incorporated the experimental data into SPICE simulation and software DNN inference, showing DNN accuracy for CIFAR-10 dataset could degrade from 87.35% to 11.58% after 144 hours. To recover the largely degraded accuracy, mitigation schemes are proposed: 1) at the circuit level, the reference voltage for RRAM IMC could be calibrated after 80 hours when the relaxation is saturated. 2) At the algorithm level, the weights are trained

with lower percentages to be quantized to the two intermediate states. With both schemes applied, the accuracy could be recovered to 87.32% for long-term stability.

10:40 a.m.
2C.4 - Optimized Programming Algorithms for Multilevel RRAM in Hardware Neural Networks, Valerio Milo[1] *, Francesco Anzalone[1], Cristian Zambelli[2], Eduardo Pérez[3], Mamathamba K. Mahadevaiah[3], Óscar G. Ossorio[4], Piero Olivo[2], Christian Wenger[3,5], Daniele Ielmini[1], [1]Politecnico di Milano and IU.NET, [2]Università degli Studi di Ferrara, [3]IHP-Leibniz-Institut für innovative Mikroelektronik, [4]Universidad de Valladolid, [5]BTU Cottbus-Senftenberg

A key requirement for RRAM in neural network accelerators with a large number of synaptic parameters is the multilevel programming. This is hindered by resistance imprecision due to cycle-to-cycle and device-to-device variations. Here, we compare two multilevel programming algorithms to minimize resistance variations in a 4-kbit array of HfO_2 RRAM. We show that gate-based algorithms have the highest reliability. The optimized scheme is used to implement a neural network with 9-level weights, achieving 91.5% (vs. software 93.27%) in MNIST recognition.

11:05 a.m.
2C.5 - Transient Investigation of Metal-Oxide Based, CMOS-Compatible ECRAM, Paul M. Solomon*, Douglas M. Bishop, Teodor K. Todorov, Simon Dawes, Damon B. Farmer, Matthew Copel, Ko-Tao Lee, John Collins, John Rozen, IBM Thomas J. Watson Research Center

Metal-oxide based Electrochemical Random-Access Memory (MO-ECRAM) has shown unique potential as a nonvolatile element for analog in-memory computation of deep learning tasks. Using a specially designed interdigitated device geometry, we investigate transient effects of MO-ECRAM and correlate them with programming speed, read speed and read-after write speed. Programming speed is shown to exponentially increase with programming voltage. Read speed reached the ns range, while read-after-write delay can be limited by decay of write transients in the studied devices. Two mechanisms of channel modulation were found; a prompt field effect and a field-induced memory effect. The charge control of the prompt effect was vastly greater than that of the memory effect. So to reduce and mitigate transient impact, we discuss both device improvements, and learning algorithm engineering strategies.

2C – Authors' Corner
11:30 a.m. – 12:00 p.m. PDT

Tutorial 1
Sunday, March 21, 09:20 a.m. – 10:50 a.m. PDT
Prem Chirayarikathuveedu, Consultant
Preeti Chauhan, Google
Venue: Monterey Main Stage

09:20 a.m.
TuT1 (Tutorial) - Reliability Challenges with 3D Integration of Semiconductor Packaging, Mohammad Kabir, Intel Corporation

Process technology scaling has driven the need for advancement in semiconductor packaging technology to address insatiable demand in performance, power and form factor. A growing number of innovative 3D package assembly technologies have evolved to enable semiconductor industry to maximize products functionality. This tutorial will cover history on packaging development with focus on 3D integrations. In-depth reliability studies of 3D integration of packaging technologies will be discussed along with some general industry perspective on future roadmaps.

Exhibitor Meet & Greet
11:20 a.m. – 03:00 p.m. PDT

Break
12:00 p.m. – 03:00 p.m. PDT

2D – NC (Neuromorphic Computing Reliability)
Sunday, March 21, 03:00 p.m. – 04:45 p.m. PDT
John Paul Strachan, Hewlett Packard Labs
Venue: Big Sur

2D – Intro
03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
2D.1 (Focus) - Can Emerging Computing Paradigms Help Enhancing Reliability Towards the End of Technology Roadmap?, Runsheng Wang[1]*, Zuodong Zhang[1], Yawen Zhang[1], Yixuan Hu[1], Yanan Sun[2], Weikang Qian[3], Ru Huang[1], [1]Institute of Microelectronics, [2]Shanghai Jiao Tong University, [3]UM-SJTU Joint Institute and MoE Key Lab of Artificial Intelligence, Shanghai Jiao Tong University

With CMOS technology shrinking into nanoscale, the design margin has become extremely tight due to the severer transistor aging and process variations. We present a new perspective to enhance design reliability: using emerging computing paradigms. As the preliminary attempts, three reliability-enhanced design flows based on approximate computing and/or stochastic computing are demonstrated. The results show that some computing paradigms are inherently robust, or can trade off computing accuracy for reliability, providing designers with more flexibility.

03:30 p.m.
2D.2 - Robust Brain-Inspired Computing: On the Reliability of Spiking Neural Network using Emerging Non-Volatile Synapses, Ming-Liang Wei[1,2], Hussam Amrouch[3], Cheng-Lin Sung[1], Hang-Ting Lue[1], Chia-Lin Yang[2], Keh-Chung Wang[1], Chih-Yuan Lu[1], [1]Macronix International Co., Ltd., [2]National Taiwan University, [3]University of Stuttgart

Reliability issues arise due to the characteristics of Non-Volatile Memory synapses operating under the limited circuit cost. Through a simulation study, we identified several criteria of the memory synapses for the membrane capacitor size of 1pF. (1) The required ON-OFF ratio needs to be >1000 to preserve classification accuracy. (2) Low ON-current Ion (<10uA) is preferred for low power. (3) The variation and error of Ion should be lower than +/- 10% of mean value.

03:55 p.m.
2D.3 - Novel Weight Mapping Method for Reliable NVM Based Neural Network, L.X.Han, Y.C.Xiang, P. Huang*, G. H. Yu, R. Z. Han, X. Y. Liu, J. F. Kang, Institute of Microelectronics, Peking University

Errors of vector-matrix-multiplication induced by interconnect resistance become a crucial reliability challenge in non-volatile memory (NVM) based neural network. Here, we propose a novel weight mapping method, called weight mapping correction (WMC), to mitigate the deviation of weight represented by the conductance of NVM array without time-consuming retraining and circuit overheads. Simulation results show that accuracy is recovered significantly when WMC is applied to various size arrays consisting of mainstream NVM in advanced technology nodes.

04:20 p.m.
2D.4 - Low-Bit Precision Neural Network Architecture with High Immunity to Variability and Random Telegraph Noise Based on Resistive Memories, Tommaso Zanotti, Francesco Maria Puglisi, Paolo Pavan, Università di Modena e Reggio Emilia

In this work, we devise and train a low-bit precision neural network with binary weights and 4-bits activations and study the impact of RRAM nonidealities on the classification accuracy by means of full circuit-level simulations enabled by a physics-based RRAM compact model, calibrated on experimental data from the literature. Results show that combining binary weights with low-precision activations allows retaining software-level accuracy even in the presence of Random Telegraph Noise and weight variability.

2D - Authors' Corner
04:45 p.m. – 05:10 p.m. PDT

Tutorial 2
Sunday, March 21, 03:00 p.m. – 04:30 p.m. PDT
Chetan Prasad, Intel Corporation

03:00 p.m.
TuT2 (Tutorial) - Practical Applications of Bayesian Reliability, Yan Liu, Medtronic

This tutorial provides fundamental knowledge of Bayesian reliability and utilizes numerous examples to show how Bayesian models can solve real life reliability problems. It covers what Bayesian analysis is, what its benefits are, and how it can be applied to reliability engineering.

Basic concepts of Bayesian statistics, models, reasons, and computation are presented. The tutorial then goes on to cover Bayesian models for estimating system reliability and design capability; a discussion of Bayesian Hierarchical Models and their applications; and more. To help readers get started quickly, the tutorial presents Bayesian model examples that use JAGS and which require fewer than 10 lines of command, and short R scripts.

Tutorial 3
Sunday, March 21, 03:00 p.m. – 04:30 p.m. PDT
Jim Ashton, NIST

03:00 p.m.
TuT3 (Tutorial) - Reliability Testing of Devices: From DC to Sub- ns Region, Yi Zhao, Zhejiang University

Conventionally, for both industry applications and research purposes, DC measurement methodology is adopted in semiconductor device characterizations. However, the clock frequency in real circuits has already been over GHz for many years and the devices, specially transistors, in the circuit also work in the sub-nano second (sub-ns) region, resulting in the strong demand for ultra fast device testing methodologies. On the other hand, traditional semiconductor parameters analyzing tools and methodologies still cannot capture the transient electrical properties of devices in the sub-ns time scale.

In this tutorial, we will first review the basics of DC device testing and then introduce ultra-fast device testing methodologies and measurement systems for both logic and memory devices. For logic devices, the impact of measurement speed on device parameter extractions will be discussed first upon considering the self heating effect and trap behaviors. And then the applications of nano second and sub-ns device testing methodologies to device reliability study will be introduced, including bias temperature instability, hot carrier degradation, and the self-heating effect in advanced technology nodes. As for new memories, device behavior

characterizations using ultra-fast device testing methodologies will be demonstrated for ferroelectric devices and MRAM.

Tutorial 4
Sunday, March 21, 03:00 p.m. – 04:30 p.m. PDT
Jason Ryan, NIST

03:00 p.m.
TuT4 (Tutorial) - 5G/mmW/RF - Silicon & 5G/mmW/RF - GaN

Silicon Reliability for 5G/mmWave/RF Applications, Fernando Guarin, Purushothaman Srinivasan, GlobalFoundries

The reliability infrastructure developed for Silicon based logic applications is not sufficient to address the requirements for 5G circuits. This tutorial will provide a practical overview of the key reliability mechanisms along with the challenges faced by reliability engineers studying the reliability of 5G/mmWave/RF applications implemented with Silicon based technologies. We will review reliability within the context of scaling, power and integration showing how these have positioned the Silicon and Silicon Germanium technologies as viable contenders for very high speed, high integration and high reliability applications. We will show a practical approach to the reliability evaluation of Power Amplifiers operating in the 28 to 39 GHz range along with a discussion of the qualification methodologies required for the release of these technologies to the field. We will cover aspects of the development of reliability models that work under industry standard circuit simulators that provide circuit designers with the necessary tools to extract the maximum performance while achieving optimum reliability. A brief overview of Self heating and its characterization in Silicon based systems will be also be presented. Throughout this tutorial we will show several examples of reliability stress data along with the models to support our methodology and conclusions.

GaN RF Device Reliability for 5G/mmW Applications, Don Gajewski, Wolfspeed

In this tutorial, I will review the reliability failure mechanisms and predictive lifetime extrapolations published in the open literature for GaN RF devices for 5G/mmW applications. I will cover failure mechanisms including field plate electromigration, piezo-electric GaN cracking/pitting, ohmic contact degradation, trap generation, hot electron injection, Schottky gate contact degradation, through-SiC via degradation, field plate dielectric dielectric breakdown, hydrogen poisoning, and gate electromigration. I will give an overview of the DCand RF-driven accelerated life testing methods, data, and intrinsic lifetime predictions. I will also cover product level reliability aspects related to humidity, high junction temperatures and temperature cycling. Finally, I will discuss some of the key implications of these reliability aspects for 5G/mmW applications.

Reliability Year-in-Review
Sunday, March 21, 05:10 p.m. – 07:30 p.m. PDT
Charlie Slayman, Cisco Systems
Venue: Monterey Main Stage

Year-in-Review: Reliability Intro
05:10 p.m. – 05:15 p.m. PDT

05:15 p.m.
YIR1 (Year-in-Review) - FinFET vs GAA: Main Reliability Differences and Concerns, Adrian Chasin, imec

FinFET devices have reigned in the last decade, allowing continuous scaling of silicon devices since first Intel adoption in the 22nm node up to the 5nm products recently released by TSMC. The adoption of a more

advanced architecture that can provide even better channel control and, therefore, allowing further scaling seems unavoidable. Gate-All-Around (GAA) devices were proposed as a natural follower and has been the focus of intensive research in the last years. Following a brief overview of the claimed performance advantages of such architecture, we will review the most recent reliability studies of this new device and how it compares to FinFETs. In particular, we will focus on new inherent features of this new technology and how they can impact the overall device reliability.

06:05 p.m.
YIR2 (Year-in-Review) - Reliability Testing: Considerations for Physics-Based Reliability Testing Development, Derek W. Slottke, Intel Corporation

Deviation from previous dependence on scaling based strategies of existing process technologies, the development of more diverse products, and pressures to minimize reliability margins are driving the need for a greater variation in available test capabilities. I hope to cover the considerations for volume reliability testing, challenges and trends, as well as some specific topics of personal interest where I believe substantial novel work should be done.

06:55 p.m.
(In cooperation with IEW)
YIR3 (Year-in-Review) - Industry Council on ESD Target Levels: Review of Achievements, Activities, and Initiatives, Charvaka Duvvury, ESD Consulting, Harald Gossner, Intel Corporation

The Industry Council on ESD Target Levels has been recommending realistic specifications for ESD to be compatible with high-speed circuit performance. This review will cover the key accomplishments of the Council that changed the industry qualification processes for ESD reliability. Also, an overview of the myriad of root causes that lead electrical overstress (EOS) damage and the notion of Absolute Maximum Rating (AMR) as it relates to probability of EOS during applications will be discussed.

Monday, March 22

Keynote 2
Monday, March 22, 08:00 a.m. – 08:45 p.m. PDT
Chris Connor, Intel
Robert Kaplar, Sandia National Labs
Venue: Monterey Main Stage

08:00 a.m.
KN2 (Keynote) - SiC MOSFET Reliability: An overnight success 30 years in the making, John Palmour, Wolfspeed, a Cree Company

The rapid adoption of SiC MOSFETs may seem like an overnight sensation, but it was actually more than 30 years in the making. It has required orders of magnitude improvements in performance, cost, availability and quality. Improved material defect densities and larger wafer diameters are lowering cost and are allowing higher current products that fit the needs of the battery electric vehicle market.
In the early days of SiC power device technology, it was thought that SiC MOSFETs could never achieve the reliability lifetimes required for commercial markets. However, the quality of oxides grown on SiC are now being shown to be on par with the best silicon devices. Measurements of TDDB, breakdown voltages, radiation resistance and other critically important tests for SiC MOS devices will be demonstrated, and the issue of bias temperature instability (threshold voltage shift) in actual application conditions will also be discussed.

3A – PI (Process Integration)
Monday, March 22, 08:45 a.m. – 10:30 a.m. PDT
Anisur Rahman, Intel
Guido Sasse, NXP Semiconductors
Mustapha Rafik, Aledia
Venue: Big Sur

3A– Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
3A.1 - Impact of Spacer Interface Charges on Performance and Reliability of Low Temperature Transistors for 3D Sequential Integration, T. Mota Frutuoso, J. Lugo-Alvarez, X. Garros, L. Brunet, J. Lacord, L. Gerrer, M. Casse, E. Catapano, C. Fenouillet-Beranger, F. Andrieu, F. Gaillard, CEA, P. Ferrari, Univ. Grenoble Alpes

The impact of interface charges under the gate spacer on FDSOI devices integrated in low temperature process are explored. A great number of traps (~10^{13} /cm^2) are identified on the interface between the spacer oxide and the silicon film using Terman's method for interface states characterization. Thanks to electrical characterization and TCAD simulations, it is shown that the trapped charges induce the formation of a depleted region in the vicinities of the spacer. Moreover, a strong degradation of performances on underlap channels is observed. The spacer charges influence on reliability measurements is finally explored.

09:15 a.m.
3A.2 - Systematic Study of Process Impact on FinFET Reliability, Rakesh Ranjan, Ki-Don Lee, Md Iqbal Mahmud, Mohammad Shahriar Rahman, Pavitra Ramadevi Perepa, Charles Briscoe Larow, Caleb Dongkyun Kwon, Maihan Nguyen, Minhyo Kang, Ashish Kumar Jha, Ahmed Shariq, Shamas Musthafa Ummer, Susannah Laure Prater, Samsung Austin Semiconductor, LLC, Hyunchul Sagong, HwaSung Rhee, Samsung Electronics, Korea

Reliability of Core and IO FinFET is extensively investigated with various process steps at Fin, Source/ Drain, sacrificial Gate-Metal, and High-Pressure D2 Anneal. By modulating the process knobs, we quantified the effect of oxide traps (at bulk or interface) on reliability mechanisms of replacement metal gate (RMG). The results are summarized as a process-reliability optimization guideline.

09:40 a.m.
3A.3 - TDDB Reliability in Gate-All-Around Nanosheet, Huimei Zhou, Miaomiao Wang, Ruqiang Bao, Tian Shen, Ernest Wu, Richard Southwick, Jingyun Zhang, Veeraraghavan Basker, Dechao Guo, IBM Research Division

Time dependent dielectric breakdown (TDDB) reliability is studied on interfacial layer (IL)/high-K gate stack of Gate-All-Around Nanosheet (GAA-NS) N- and P-type Field Effect Transistors (FETs) with volume-less multiple threshold voltage (multi-Vt) integration scheme enabled by the dual dipoles (n-dipole and p-dipole). We report for the first time Key TDDB Modeling parameters: voltage acceleration exponent (VAE), Weibull slope (β), and activation energy (E_a) and show robust TDDB reliability in multi-Vt NS transistors enabled by different dipoles.

10:05 a.m.
3A.4 - Process-Induced Charging Damage in IGZO nTFTs, Gaspard Hiblot, Nouredine Rassoul, Lieve Teugels, Katia Devriendt, Adrian Vaisman Chasin, Michiel van Setten, Attilio Belmonte, Romain Delhougne, Gouri Sankar Kar, IMEC

In this work, charging damage induced by processing in 300mm FAB on Indium-Gallium-Zinc-Oxide (IGZO) n-type Thin Film Transistors (TFT) is investigated using antennae connected at different levels. A compounded degradation due to two different mechanisms is revealed. Plasma etch damage is found to degrade the gate oxide leakage and reliability, while CMP-related charging affects the conductivity of the extension regions of the transistor.

3A - Authors' Corner
10:30 a.m. – 10:55 a.m. PDT

3B – 5G (RF/mmW/5G Reliability)
Monday, March 22, 08:45 a.m. – 10:30 a.m. PDT
Jose Jimenez, Qorvo
Fernando Guarin, GlobalFoundries
Venue: Carmel

3B – Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
3B.1 (Focus) - New Developments in SiGe HBT Reliability for RF Through mmW Circuits, John D. Cressler, School of Electrical and Computer Engineering

This paper reviews current progress in our understanding of the reliability of SiGe HBTs and the circuits built from them, including: 1) fundamental understanding of the multiple operative damage mechanisms, 2) the differences between DC and RF reliability, 3) the path to predictive reliability-aware compact models, and 4) the concept of Circuit- Safe Operating Area (C-SOA), which offers a better benchmark for understanding reliability-imposed constraints on circuits and systems.

09:15 a.m.
3B.2 (Focus) - Reliability and Failure Analysis of 100 nm AlGaN/GaN HEMTs under DC and RF Stress, M. Dammann, M. Baeumler, T. Kemmer, H. Konstanzer, P. Brückner, S. Krause, Fraunhofer Institute for Applied Solid State Physics IAF, A. Graff, M. Simon-Najasek, Fraunhofer Institute of Microstructure of Materials and Systems

Degradation of 100 nm AlGaN/GaN HEMTs under DC and 10 GHz stress conditions has been compared and a promising median lifetime of more than 2000 h under RF stress in air at a drain voltage of 15 V and an average channel temperature of 230°C has been achieved. It has been found that the devices degrade faster under RF stress compared to DC stress. Physical failure analysis using electroluminescence, TEM and EDX has been done.

09:40 a.m.
3B.3 - RF Reliability of SOI-Based Power Amplifier FETs for mmWave 5G Applications, P. Srinivasan, F. Guarin, S. Syed, J. A. S. Jerome, W. Liu, S. Jain, D. Lederer, S. Moss, P. Colestock, A. Bandyopadhyay, N. Cahoon, B. Min, M. Gall, Globalfoundries Inc.

RF reliability at 28GHz in PAFETs under constant and varying output load (Z0) was evaluated. Time domain analyses show that in addition to non-conducting TDDB (ncTDDB), both **o**nducting (cHCI) and non-conducting Hot Carrier Injection (ncHCI) degradation play key roles as primary mechanisms. RF power as stress variable under linear, P1dB and compression shows higher degradation in compression attributed to higher peak voltage swings. Degradation under varying load is correlated to ruggedness power and VSWR ratio.

10:05 a.m.
3B.4 - Large Signal RF Reliability of 45-nm RFSOI Power Amplifier Cell for Wi-Fi6 Applications, Aarti Rathi[1], P.Srinivasan[2], F.Guarin[2], Abhisek Dixit[1], 1. Indian Institute of Technology, 2. GLOBALFOUNDRIES Inc

A power amplifier cell having a single n-channel transistor fabricated in 45-nm RFSOI technology is stressed using both DC drain voltage as well as RF power at 7GHz applied to the gate reproducing Wi-Fi6 like operating conditions. Impact of the stress is studied using both DC as well as RF metrics. Impact on impedance matching is also studied using small signal characteristics. Through this work, we attempt to explore differences in hot carrier degradation mechanisms between DC and RF stress conditions. Impact of hot carrier degradation on DC and RF parameters is also presented by analyzing the time slope exponent. Degradation in DC and RF performance (small and large signal) is compared under varying stress conditions (DC, RF, and DC+RF).

3B - Authors' Corner
10:30 a.m. – 10:55 a.m. PDT

Tutorial 5
Monday, March 22, 08:45 a.m. – 10:15 a.m. PDT
Jason Ryan, NIST

08:45 a.m.
TuT5 (Tutorial) - Neuromorphic Computing, Brian Hoskins, NIST

The different requirements of neuromorphic computers, including enormous demand for memory and a high tolerance for defects, is causing a reassessment of research priorities into integrated circuit manufacturing. We will review the foundations of the most important new computing approaches in A.I. and the ways these operations can be accelerated using nanotechnology for critical use cases, but especially for online training of networks as well as inference in the field where they will be deployed.

Tutorial 6
Monday, March 22, 08:45 a.m. – 10:15 a.m. PDT
Marta Bagatin, University of Padova

08:45 a.m.
TuT6 (Tutorial) - Calculation of Terrestrial Cosmic-Ray Displacement Damage, Melanie Raine, CEA, DAM, DIF, Nicolas Richard, CEA, DAM, DIF

Terrestrial neutrons due to cosmic rays from the outer space are constantly striking electronic devices at ground level. Each neutron is likely to generate a cascade of atomic displacement, that can be referred to as Single Particle Displacement Damage. With device integration, these single cascades might impact the properties of integrated devices. This tutorial presents a comprehensive approach for the simulation of Single Particle Displacement Damage, from the incident particle interaction to the resulting electrical effect observed experimentally. The different steps of the global approach are presented, first describing the succession of phenomena at stake, and then identifying the corresponding simulation technique chosen for each step of the process, some outputs of one step being the inputs of the next. Combining different techniques allows covering large time scales, from the fs for the interaction itself to long-term evolution observed after seconds and more.

Monte Carlo simulation of the interaction between an incident particle and silicon, in the Binary Collision Approximation (BCA) is first performed. The next step is a classical Molecular Dynamics (MD) simulation of the trajectory of selected Primary Knock-on Atoms (PKA), with the detailed displacement cascade and the

first steps of its evolution. To explore the long term evolution of this structure and reach time scales comparable with experimental data, a new technique called the kinetic Activation-Relaxation Technique (k-ART) is then used. Finally, first principles calculations are performed to calculate the electronics properties of the selected atomic damage structure. The output is, for each selected atomic damage structure, the energy levels introduced in the bandgap and the associated electronic activity. The originality of this comprehensive approach is to link these different types of simulations that are usually performed independently, to obtain realistic damage structures representative of what results from the initial neutron-silicon interaction and to identify defect structures detrimental to the technology's performances.

Tutorial 7
Monday, March 22, 10:15 a.m. – 11:45 a.m. PDT
Bonnie Weir, Broadcom

10:15 a.m.
TuT7 (Tutorial) - Understanding and Challenges of MOL/BEOL TDDB Reliability, Andrew Kim, Intel

MOL (Middle-Of-Line) and BEOL (Back-End-Of-Line) dielectric reliabilities have become a great importance for advanced semiconductor process technology development and qualifications. Particularly, dielectric thickness variation effect on MOL/BEOL TDDB has become a severe issue to deal with in terms of characterization and lifetime modeling. This tutorial will begin with an introductory review of MOL/BEOL TDDB followed by various topics such as statistical modeling of Tbd (Time-to-Breakdown), thickness variation effect on Tbd, review of voltage acceleration models, requirements of voltage acceleration model validation, consideration for TDDB test device designs and advanced characterization/modeling methods. As supplemental characterization/screening methods of TDDB, ramped voltage stress (RVS) and ramped current stress (RCS) will also be discussed. Both entry-level and experienced TDDB reliability colleagues are strongly encouraged to attend.

Tutorial 8
Monday, March 22, 10:15 a.m. – 11:45 a.m. PDT
Robert Kaplar, Sandia National Labs

10:15 a.m.
TuT8 (Tutorial) - GaN Reliability, Enrico Zanoni, University of Padova, Department of Information Engineering, Padova

GaN HEMTs represent nearly ideal devices for high efficiency switching converters and power management systems, as well as for microwave and millimeter-wave communication apparatus and imaging systems. Power MISHEMT devices have attained blocking voltages of several hundred volts, yet maintaining extremely low values of on-resistance. By carefully controlling short-channel effects, sub-100 nm GaN microwave devices can achieve record values of RF power density and power added efficiency up to W-band. Mature, stable technologies have been demonstrated, with remarkable extrapolated lifetimes. Power and RF GaN HEMTs share common failure mechanisms (e.g. hot-electron effects and threshold voltage instabilities); specific failure mechanisms depend on operating conditions and environment, technology, material quality. Surface and interfaces play a dominant role in determining device reliability.In power devices, time-dependent breakdown mechanisms affect both dielectrics and GaN-based semiconductor epitaxial layers. For microwave devices, thermally accelerated interdiffusion effects and electrochemical oxidation still represent a potential issue. The tutorial will review failure mechanisms of GaN HEMTs in relation with high voltage operation, high current density, high electric field and hot-electrons, and compare their impact on the various device applications.

Exhibitor Meet & Greet
11:20 a.m. – 03:00 p.m. PDT

Break
12:05 p.m. – 03:00 p.m. PDT

3D – SY/SE (System Electronics Reliability & Soft Error)
Monday, March 22, 03:00 p.m. – 05:10 p.m. PDT
Flavio Griggio, Microsoft
Daisuke Kobayashi, isas/jaxa
Yan Liu, Medtronic
Yanran Chen, Xilinx, Inc.
Venue: Big Sur

3D – Intro
03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
3D.1 (Invited) - Single Event Hard Error Due to Terrestrial Radiation, Jin-Woo Han, M. Meyyappan, NASA Ames Research Center Moffett Field, Jungsik Kim, Gyeongsang National University

Alpha particle radioactive contamination is often found in semiconductor packaging materials, and neutrons generated by cosmic rays constantly approach the ground. Historically, these radiations are regarded as a source of soft-error. We are in era of aggressive device miniaturization, operation voltage scaling and increasing frequency. Herein, we present that the terrestrial radiation-induced single event can potentially result in hard-error. As a result, radiation hardening might be necessary in the near future even in consumer electronics.

03:30 p.m.
3D.2 - Scaling Trends in the Soft Error Rate of SRAMs from Planar to 5-nm FinFET, B. Narasimham, V. Chaudhary, M. Smith, L. Tsau, Broadcom Inc, D. Ball, B. Bhuva, Vanderbilt University

SRAM SER measurements across technology nodes indicate that while scaling from planar processes down to the 7-nm FinFET process provided a reduction in the per-bit SER at every node, subsequent scaling to the 5-nm FinFET process results in an increase in the per-bit SER relative to the 7-nm FinFET process. Extensive data collected across a range of supply voltages show strong exponential bias dependence of SRAM SER for FinFET processes, but the rate of increase in SER as supply voltage is reduced is lower for the 5-nm process compared to the 7-nm. Simulations and modeling indicate that variations in the critical charge (Q_{crit}) is the key reason for the observed trends.

03:55 p.m.
3D.3 - Soft-Error Suseptability in Flip-Flop in EUV 7 nm Bulk-FinFET Technology, Taiki Uemura, Byungjin Chung, Jeongmin Jo, Mijoung Kim, Dalhee Lee, Gunrae Kim, Seungbae Lee, Taesjoong Song, Hwasung Rhee, Brandon Lee, Samsung Electronics, Jaehee Choi, Semiconductor Research and Development Center

This paper presents single-event upset (SEU) rates in flip-flops (FFs) in EUV 7 nm bulk-FinFET technology. EUV technology achieves high transistor-density, small FF cell-size, and low SEU rate. The alpha-SEU rate in EUV 7 nm FFs is 0.7X of the SEU rates in 10 nm FFs. The neutron-SEU rate in EUV 7 nm FFs is 0.6X of the SEU rates in 10 nm FFs. This paper also discusses the circuit dependence of the SEU rate in Normal-, Reset-, Set-FFs, and a soft-error immune FF (SEIFF), and SRAM.

04:20 p.m.
3D.4 - A Study on System Level UFS M-PHY Reliability Measurement Method using RDVS, NamHyuk Yang[1], JinHwan Kim[1], GeonGu Park[1], ChulHyuk Kwon[1], SeungTaek Lee[1], SangWoo Pae[1], HooSung Kim[1], SangWon Hwang[1], 1. Samsung Electronics

With the development of high speed serial interface technology, data transmission speed is increasing and it is important to secure the signal transmission quality. In particular, in the case of smartphones, the signal compatibility of the physical layer (M-PHY) is critical with various application processors (AP) and devices communicating eachother. This study proposes a method for verifying M-PHY reliability similar to the actual user environment based on a Universal Flash Storage (UFS) used in smartphone.

04:45 p.m.
3D.5 - Reliability Characterization of a Flexible Interconnect for Cryogenic and Quantum Applications, Emma R. Schmidgall, Flavio Griggio, George H. Thiel, Microsoft Corporation Redmond, Sherman E. Peek, Bhargav Yelamanchili, Archit Shah, Vaibhav Gupta, John A. Sellers, Michael C. Hamilton, Department of Electrical and Computer Engineering/Alabama Micro/Nano Science and Technology Center, David B. Tuckerman, Tuckerman & Associates, Samuel d'Hollosy, Hightec MC AG

We present reliability characterization of a polyimide/copper-based flexible interconnect designed for cryogenic and quantum computing applications. This interconnect design uses commercial fabrication processes and off-the-shelf parts. This paper presents results from the flexible interconnects bonded to a commercial connector part. A model is described to estimate a system failure rate due to interconnect and connector subassembly failures. The results of this study conclude that the flexible interconnect tapes are well suited for cryogenic temperature applications.

3D - Authors' Corner
05:10 p.m. – 05:30 p.m. PDT

3E – 5G (RF/mmW/5G Reliability)
Monday, March 22, 03:00 p.m. – 04:45 p.m. PDT
Fernando Guarin, GlobalFoundries
Jose Jimenez, Qorvo
Venue: Carmel

3E – Intro
03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
3E.1 - CMOS RF Reliability for 5G mmWave Applications – Challenges and Opportunities, P. Srinivasan, F. Guarin, GLOBALFOUNDRIES Inc

CMOS RF technologies are now entering mainstream due to opportunities presented by 5G technologies. RF Front-End-Module designs to enable 5G mmWave applications focus on performance and efficiency RF metrics. One key element that also requires focus and attention is RF reliability. This work will focus on key challenges in evaluating RF reliability at device and circuit level and the opportunities that exist towards meeting these requirements to enable successful designs.

03:30 p.m.
3E.2 (Focus) - Guidelines for Space Qualification of GaN HEMTs and MMICs, John Scarpulla, The Aerospace Corporation

GaN HEMTs and MMICs are candidates for use in space systems because of their many advantages especially as RF/microwave amplifiers. To date however, no GaN devices have successfully been qualified high reliability, long duration missions. The purpose of this paper is to recommend GaN-specific test protocols and guidelines to attempt to amend this situation. A document expanding upon this paper is now available, and a working group continues to refine it.

03:55 p.m.
3E.3 - On the Impact of Buffer and GaN-Channel Thickness on Current Dispersion for GaN-on-Si RF/mmWave Devices, V. Putcha[1], L. Cheng[2], A. Alian[1], M. Zhao[1], H. Lu[2], B. Parvais[1,3], N. Waldron, D. Linten[1], N. Collaert[1, 1]imec, [2]Nanjing University, [3]Vrije Universiteit Brussels

An important degradation monitor for GaN-on-Si technology is the current dispersion, resulting from charge (de-)trapping into the defects in the buffer stack or the barrier layer. It is commonly monitored as device's ON-resistance (R ON). In this work, a detailed study of the impact of buffer thickness and the GaN-channel layer thickness on the dynamic- R ON is carried out and important insights that are useful for optimizing the buffers for GaN-on-Si technology are obtained.

04:20 p.m.
3E.4 - Role of the AlGaN Cap Layer on the Trapping Behaviour of N-Polar GaN MISHEMTs, F. Chiocchetta, C. Calascione, C. De Santi, C. Sharma, F. Rampazzo, X. Zheng, B. Romanczyk, M. Guidry, H. Li, S. Keller, U. K. Mishra, G. Meneghesso, M. Meneghini, E. Zanoni, 1. University of Padova, Department of Information Engineering, 2. University of California Santa Barbara

We investigate the performance of N-polar GaN MIS-HEMT devices as a function of the aluminum concentration in the top AlGaN cap layer. It is demonstrated that the use of high aluminum concentration in the cap layer results a lower gate leakage current. It's also shown that the use of high Al concentration can suppress the current collapse. The results points out the key role of the AlGaN cap layer on the performance of AlGaN-based MISHEMTs.

3E - Authors' Corner
04:45 p.m. – 05:10 p.m. PDT

3F – MB (Metallization/BEOL Reliability)
Monday, March 22, 03:00 p.m. – 05:10 p.m. PDT
Rahim Kasim, Intel Corporation
Venue: Pebble Beach

3F – Intro
03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
3F.1 (Invited) - Back End of Line Opportunities and Reliability Challenges for Future Technology Nodes, Mauro J. Kobrinsky[1], Rahim Kasim[2], 1. Intel Corporation, 2. CQN, Intel Corporation

In this presentation, we will describe both evolutionary and disruptive Back End of Line innovations needed to enable scaling and performance improvements, and their reliability impact.

03:30 p.m.
3F.2 - Reliability of a DME Ru Semidamascene Scheme with 16 nm wide Airgaps, A. Leśniewska, O. Varela Pedreira, M. Lofrano, G. Murdoch, M. van der Veen, A. Dangol, N. Horiguchi, Zs. Tőkei, K. Croes, imec

We evaluate the reliability of a semidamascene BEOL scheme with direct metal etched (DME) Ruthenium and 16 nm wide air gaps (AG). First, we show that Ru can be barrierless independent of the type of deposition (ALD, CVD, PVD) using planar capacitor structures with a metal-etch-based flow. We present TDDB results of semidamascene Ru +AG showing V_{max} to be above 1.5 V for TTF 0.1% of 3 km long lines at 100ºC (using power law model). We show no change in resistance after >1200 h during electromigration tests at 330ºC with 5 MA/cm^2 stress. We identify increased Joule heating as a reliability concern.

03:55 p.m.
3F.3 - Electromigration Limits of Copper Nano-Interconnects, Houman Zahedmaesh, Olalla Varela Pedreira, Zsolt Tokei, Kristof Croes, imec

In this paper the electromigration (EM) limits of Cu nano-interconnects are studied considering the impact of microstructure in Co cap schemes and performance booster technologies i.e. via pre-fill and scaled barrier-liner schemes. A combination of experimental and physics-based modelling approaches is employed to provide fundamental understanding.

04:20 p.m.
3F.4 - Intrinsic Reliability of BEOL Interlayer Dielectric, J. Palmer[1]*, G. W. Zhang[1], J. R. Weber[2], Che-yun Lin[1], C Perini[1], R. Kasim[1], [1] Quality and Reliability, 2. TCAD, Intel Corporation

As interconnect dimensions shrink, interlayer breakdown is increasingly relevant to reliability. This paper presents TDDB, voltage acceleration, and leakage data for Cu and Co interconnects. The leakage mechanism is found to be Poole-Frenkel saturation transitioning to Fowler-Nordheim tunneling at high field. We conclude the interlayer lifetime is limited by the low-k dielectric and propose an E-model acceleration. The reliability of interlayer TDDB must consider the asymmetric voltage division of the etch stop/low-k stack.

04:45 p.m.
3F.5 - Strategy to Characterize Electromigration Short Length Effects in Cu/Low-k Interconnects, [1]Z. Zhang, [2]M. Kraatz, [1]M. Hauschildt, [1]S. Choi, [2]A. Clausner, [2]E. Zschech, [1]M. Gall, 1. GLOBALFOUNDRIES, 2. Fraunhofer Institute for Ceramic Technologies and Systems IKTS

With the increasing amount of on-chip interconnects and continuous down-scaling, electromigration will play a more critical role especially for automotive reliability, which requires high statistical confidence. In confined metal lines, tensile stress builds up at the cathode side before void nucleation; compressive stress builds up at the anode side. A critical stress is required for EM-induced void formation to occur. Proper understanding of the critical stress is crucial for boosting interconnect RC performance, yet guaranteeing robust electromigration reliability. This study aims to characterize the short length effect and physical degradation behavior with a modified Wheatstone Bridge structure to significantly increase the statistical confidence.

3F – Authors' Corner
05:10 p.m. – 05:30 p.m. PDT

Tutorial 9
Monday, March 22, 03:00 p.m. – 04:30 p.m. PDT
Mark Anders, NIST

03:00 p.m.
TuT9 (Tutorial) - Device Instability Considerations for Future Materials and Devices That Require Low Temperature Gate Oxide Processing, Chadwin Young, University of Texas at Dallas

Current metal-oxide-semiconductor (MOS) research and development is engaged in high-k dielectrics on non-silicon semiconductors for use in cutting-edge CMOS technology, large- area/flexible electronics, monolithic 3D back-end-of-line (BEOL) integration, and power electronics. In many of these explored technologies, quality high-k dielectric deposition has not been solved. Furthermore, conventional deposition process conditions (i.e., deposition temperatures > 200°C, relatively high temperature annuals, etc.) may not be possible in large- area/flex or 3D BEOL integration. In addition, top-gate dielectric deposition on novel semiconductors such as transition metal dichalcogenides (TMDs) may require relatively low deposition temperatures as well. This will usher in a host of new device performance and reliability challenges. In order to investigate these challenges, one cannot assume that these relatively low temperature high-k gate dielectrics will be as robust as the current state of the art high-k. There are clear challenges with dielectric interface and bulk quality. Therefore, electrically characterized evaluation of as-deposited gate dielectric performance as well as time- dependent evaluation (i.e., voltage stress) will require scrutiny and revisiting characterization methods from the "early days" of high-k exploration. This tutorial will provide an overview of MOS-related research on promising non-silicon semiconductors with an emphasis on electrically active defect characterization.

Tutorial 10
Monday, March 22, 04:30 p.m. – 06:00 p.m. PDT
Jim Ashton, MIST

04:30 p.m.
TuT10 (Tutorial) - Advanced 3D Flash Memory Architectures, Lue Hang-Ting, Macronix

In this tutorial, I will briefly introduce the history of various 3D NAND Flash architectures, including BiCS, TCAT, VG, VSAT, and twin-bit cells (SGVC, HC, or split-gate cell). And then I will briefly illustrate the mainstream 3D NAND structure used in mass production, followed by the future directions for 3D NAND scaling. Next, I will introduce the recently developed 3D NORtype architecture for low-latency high-speed purposes, including vertical-channel split-gate Flash and 3D AND-type architecture. Finally, I will introduce computing--in-memory (CIM) using 3D NAND and 3D NOR.

3G – PR/ESD (IC Product Reliability & ESD and Latchup)
(In cooperation with IEW)
Monday, March 22, 05:30 p.m. – 06:50 p.m. PDT
Mototsugu Okushima, Renesas Electronics
Richard Rao, Inphi Corp.
Venue: Big Sur

3G – Intro
05:30 p.m. – 05:35 p.m. PDT

05:35 p.m.
3G.1 - Product Lifetime Estimation in 7nm with Large Data of Failure Rate and Si-Based Thermal Coupling Model, Jae-Gyung Ahn, Rhesa Nathanael, I-Ru Chen, Ping-Chin Yeh, Jonathan Chang, Central Engineering Group

We got lifetime (LT) of FPGA chips with FEOL TDDB and EM. Reliability results from design are saved as a database of TDDB Aeff and EM Cumulative Failure Rate (CFR). With use conditions, EM CFR of each metal layers are used to get more accurate EM LT. We measured Thermal Coupling Factor (TCF) by using 4-point probe metal resistance test structures and found that the values are lower than assumed model in thermal-aware flow. It was demonstrated that lower TCF results in better product EM LT. We built Product-Level Reliability Estimator (PLRE) with better GUI and it provides quantitative answers for product reliability.

06:00 p.m.
3G.2 - Considerations in High Voltage Lateral ESD PNP Design, Milan Shah[1], Yujie Zhou[1], David LaFonteese[2], Elyse Rosenbaum[1], [1]University of Illinois at Urbana-Champaign, [2]Texas Instruments

This work investigates design options for three different classes of high voltage lateral ESD PNPs in a 0.5-µm BCD technology. The PNP layout topology is observed to affect the area efficiency as well as the device's I-V characteristic. Collector-tied field plates exert significant control over the device's turn-on voltage, and this is explored using TCAD. A "two-valued on-resistance" is observed in some PNP devices, depending on the doping profile.

06:25 p.m.
3G.3 - Compact Model of ESD Diode Suitable for Sub-Nanosecond Switching Transients, Shudong Huang, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

This work presents a non-quasi-static compact model of ESD diodes for circuit simulation. The model accurately predicts the transient behavior of the diode during both turn-on and turn-off. The accurate representation of the turn-off transient is achieved in part by modeling the time delay from an applied reverse bias to the avalanche multiplication of the reverse current. There is good agreement between measurement and simulation, even when the device is tested using sinusoidal rather than square pulses.

3G - Authors' Corner
06:50 p.m. – 07:10 p.m. PDT

3H – MY (Memory Reliability)
Monday, March 22, 05:30 p.m. – 06:50 p.m. PDT
Jiezhi Chen, Shandong University
ShuJen Lee, Intel
Venue: Carmel

3H – Intro
05:30 p.m. – 05:35 p.m. PDT

05:35 p.m.
3H.1 (Invited) - Challenges of Flash Memory for Next Decade, Kazunari Ishimaru, Institute of Memory Technology Research and Development

We investigate the performance of N-polar GaN MIS-HEMT devices as a function of the aluminum concentration in the top AlGaN cap layer. It is demonstrated that the use of high aluminum concentration in the cap layer results a lower gate leakage current. It's also shown that the use of high Al concentration can suppress the current collapse. The results points out the key role of the AlGaN cap layer on the performance of AlGaN-based MISHEMTs.

06:00 p.m.
3H.2 - Reliability of Mo as Word Line Metal in 3D NAND, D. Tierno, K. Croes, A. Ajaykumar, S. Ramesh, G. Van den Bosch, M. Rosmeulen, imec

We evaluate the reliability of Mo as word line metal for 3-D NAND Flash devices, by mimicking the stacked architecture using planar capacitors with SiO_2/Al_2O_3 and SiO_2/HfO_2 dielectric stacks. By combining TDDB and TVS measurements with simulations, we show that Mo does not drift in the two examined stacks. Moreover, our study highlights the importance of controlling the defectivity at the SiO_2/high-k interface and within the high-k to avoid the risk of early dielectric breakdown.

06:25 p.m.
3H.3 - Effect of High Temperature on Recovery of Hot Carrier Degradation of Scaled nMOSFETs in DRAM, D. Son, G.-J. Kim, J. Kim, N. Lee, K. Kim, S. Pae, Samsung Electronics

Recovery mechanism of hot carrier degradation of nMOSFETs under a high temperature was investigated. Hot carrier injection was tested, and the devices were stored under 25℃~280℃. The device stored under high temperature showed recovery characteristics for 64~70% of Idsat, 71% of Vth. The fast measurement method was used, and there was no fast recovery. These results indicate that hot carrier lifetime should be carefully evaluated by concerning not only temperature effect but also recovery effect.

3H - Authors' Corner
06:50 p.m. – 07:10 p.m. PDT

3I – MB (Memory Reliability)
Monday, March 22, 05:35 p.m. – 06:00 p.m. PDT
Rahim Kasim, Intel Corporation
Venue: Pebble Beach

3I – Intro
05:30 p.m. – 05:35 p.m. PDT

5:35 p.m.
3I.1 - Moisture Diffusion Rate in an Ultra-Low-k Dielectric and its Effect on the Dielectric Reliability, N. Duan, V. Subramanian, E. Olthof, P. Eggenkamp, M. van Soestbergen, R. Braspenning, NXP Semiconductors, Nijmegen

Moisture diffusion behavior in an ultra-low-k (ULK) dielectric has been studied using a ring oscillator. The diffusion constant of water in the ULK dielectric was found to be temperature and moisture concentration dependent and can be modeled as an Arrhenius function with an activation energy of 0.27 eV. Furthermore, the impact of moisture on dielectric reliability was investigated by a comb-meander test structure without edge seals. The experimental results showed that moisture could easily be absorbed by an ULK dielectric. The absorbed moisture cannot be completely desorbed with high temperature dry baking. The presence of moisture has significant impact on the dielectric breakdown voltage and the time-dependent dielectric breakdown (TDDB) lifetime.

3I - Authors' Corner
06:00 p.m. – 06:25 p.m. PDT

Tutorial 11
Monday, March 22, 06:00 p.m. – 07:30 p.m. PDT
Jason Ryan, NIST

06:00 p.m.
TuT11 (Tutorial) - Magnetic Resonance Techniques for Electronic Materials, Mark Anders, NIST

Understanding the nanoscale nature of defects and their roles in reliability problems offers a path towards their engineering and mitigation. Electron paramagnetic resonance (EPR) based analytical techniques offer a unique approach to understanding reliability issues as they directly interrogate the physical and chemical nature of defects (typically point defects) in materials. EPR utilizes the effects of magnetic fields on electron spin to extract this nanoscale information. Classical EPR measurements have a sensitivity of about 1010 total spins, involves measurement of bulk samples: substrates, thin films, dielectric stacks, etc., and are sensitive to

all paramagnetic defects in these materials. While classical EPR has been successful in identifying some defects involved in reliability problems, its sensitivity is much too low for modern scaled devices. However, advances in techniques able to detect EPR in device characteristics such as resistance or capacitance offer many advantages over classical EPR. Techniques such as electrically detected magnetic resonance (EDMR) and capacitively detected magnetic resonance (CDMR) have much higher sensitivity, about 107 higher than EPR, and, critically, interrogate only defects which are directly related to electronic transport. Thus, these techniques are uniquely positioned to directly elucidate the roles of defects in problems such as threshold voltage instabilities, hot carrier stress, dielectric breakdown, etc. This tutorial will develop a basic understanding of the physics involved in EPR and EPR based techniques, their applications, experimental setups, and some examples of their use and success in reliability studies.

Tuesday, March 23

Keynote 3
Tuesday, March 23, 08:00 a.m. – 08:45 a.m. PDT
Robert Kaplar, Sandia National Labs
Chris Connor, Intel
Venue: Monterey Main Stage

08:00 a.m.
KN3 (Keynote) - Laying the Groundwork for 6G communications, Peter Gammel, GlobalFoundries

With the deployment of 5G accelerating, it is essential to lay the groundwork for 6G now. In this talk we will explore some of the megatrends driving the need to 6G, as well as some of the unique opportunities that 6G will enable. We will also review the need for coordination between WLAN, 6G and LEO communication to create the seamless, ubiquitous and secure communications network of the future. As the spectrum for 6G data rates is likely to extend beyond 100GHz, we will also review semiconductor device performance for 100GHz-300GHz networks, with a focus on advance SiGe and fully-depleted SOI technologies.

4A – CR (Circuit Reliability and Aging)
Tuesday, March 23, 08:45 a.m. – 11:45 a.m. PDT
Mingoo Seok, Columbia University
Venue: Big Sur

4A – Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
4A.1 (Invited) - Silicon Lifecycle Management (SLM) with in-Chip Monitoring, Rajesh Kashyap, Hardware Analytics and Test Business Unit

Increasing chip and system complexity, coupled with growing performance and reliability requirements, are driving the need for ongoing post-silicon analysis, maintenance and optimization. In-chip monitor and sensor data provide visibility into critical performance, reliability and security issues for the entirety of a chip's lifespan. Silicon lifecycle management closes the silicon loop through the analysis of the data from monitors and sensors and enables new levels of insights for both SoC teams and their customers and provide the ability to optimize operational activities at each stage of the device and system lifecycles.

09:15 a.m.
4A.2 - Reliability and Variability-Aware DTCO Flow: Demonstration of Projections to N3 FinFET and Nanosheet Technologies, G. Rzepa*, M. Karner*, O. Baumgartner*, G. Strof*, F. Schanovsky*, F. Mitterbauer*, C. Kernstock*, H.W. Karner*, P. Weckx•, G. Hellings•, D. Claes•, Z. Wu•◊, Y. Xiang•◊, T. Chiarella•◊, B. Parvais•°, J. Mitard•, J. Franco•, B. Kaczer•, D. Linten•, Z. Stanojevic*, *Global TCAD Solutions, •imec, ◊ KU Leuven, ° Vrije Universiteit Brussels

Reliability and variability-aware simulations of logic cells are essential to correctly analyze and predict the performance of upcoming technologies. A simulation flow for DTCO is presented here, which combines the accuracy of TCAD with the performance of SPICE - utilizing parasitic extractions, the impedance field method for variations, and the compact- physics simulator Comphy for reliability. Good agreement with experimental RO performance of iN14 is demonstrated and projections to N3 FinFET and nanosheet technologies are made.

09:40 a.m.
4A.3 - An All BTI (N-PBTI, N-NBTI, P-PBTI, P-NBTI) Odometer Based on a Dual Power Rail Ring Oscillator Array, Gyusung Park, Intel Corporation, Hanzhao Yu, Minsu Kim, Chris H. Kim, University of Minnesota

An on-chip reliability monitor capable of characterizing all four bias temperature instability (BTI) modes is proposed. Stressed ring oscillators with independent dual power rails are implemented in which odd and even stages of an inverter chain are subject to different stress voltage configurations. A beat frequency detection technique with 3 reference ring oscillators achieves a frequency measurement resolution as low as 0.01% with a short measurement interruption time of 4µs. Extensive BTI data collected from a 65nm ROSC array is presented for different stress conditions.

10:05 a.m.
4A.4 - A BSIM-Based Predictive Hot-Carrier Aging Compact Model, Y. Xiang[1,2]*, S. Tyaginov[1,3,4], M. Vandemaele[1,2], Z. Wu[1,2], J. Franco[1], E. Bury[1], B. Truijen[1], B. Parvais[1,5], D. Linten[1], B. Kaczer[1], [1]imec, [2]Department of Electrical Engineering (ESAT), [3]Institute for Microelectronics (IuE), [4]Ioffe Physical-Technical Institute of the Russian Academy of Sciences, [5]Department of Electronics and Informatics (ETRO)

We present a predictive HCD compact model built upon industry-standard BSIM, thus embedding the essential HCD physics within common SPICE simulation flows. We leverage and augment the established BSIM model for self-consistently estimating the V TH shift and mobility degradation caused by the HCD-generated interface states. Our approach exhibits non-empirical predictabilities of stress time- and sensing bias- dependency of transistor-level degradation, which further accommodate the arbitrary transient waveforms for evaluating the power-performance degradation at circuit level.

10:30 a.m.
4A.5 - Overhead Reduction with Optimal Margining using A Reliability Aware Design Paradigm, S. Mishra, P. Weckx, O. Zografos, J. Y. Lin, A. Spessot, F. Catthoor, IMEC vzw

With technology scaling, a significant portion of the clock period goes into margining against timing fluctuations caused by PVT variations and aging related timing drift. If not modeled properly, corner based designs are adopted which involve applying optimistic/pessimistic margins. In this paper, we propose a workload-dependent reliability aware optimization flow by utilizing an optimal margining scheme under the influence of NBTI aging. This flow thus enables achieving desired PPA goals without severe reliability penalty.

10:55 a.m.
4A.6 - Bias Temperature Instability Depending on Body Bias through Buried Oxide (BOX) Layer in a 65 nm Fully-Depleted Silicon-on-Insulator Process, Ryo Kishida*, Ikuo Suda[1], Kazutoshi Kobayashi[1], *Tokyo University of Science, [1]Kyoto Institute of Technology

Bias temperature instability (BTI) depending on body bias through the buried oxide (BOX) layer was measured using ring oscillators at nominal gate-source voltage. BTI through the BOX layer becomes dominant on OFF-state transistors by applying reverse body bias (RBB) even at nominal gate-source voltage. BTI-induced degradation is accelerated by RBB, which is opposite to previous results at which only ON-state transistors were measured. The degradation rate at 1.0 V RBB is more than 5x larger than that in zero body bias.

11:20 a.m.
4A.7 (IIRW) - Circuit Reliability Analysis of In-Memory Inference in Binarized Neural Networks, Tommaso Zanotti, Francesco Maria Puglisi, Paolo Pavan, Università di Modena e Reggio Emilia

Logic-in-memory architectures based on the material implication logic (IMPLY) and resistive RAM (RRAM) devices enable the realization of energy efficient Binarized Neural Networks (BNNs) hardware accelerators. However, conventional circuit implementations suffer from several reliability issues that hinder real circuit implementations. By using a physics-based RRAM compact model, we demonstrate that the smart IMPLY (SIMPLY) architecture solves these reliability issues, and results in a >10 2 energy-delay-product (EDP) improvement with respect to a conventional low-power solution.

4A - Authors' Corner
11:45 a.m. – 12:05 p.m. PDT

4B – RT (Reliability Testing)
Tuesday, March 23, 08:45 a.m. – 10:30 a.m. PDT
Yi Zhang, Zhejiang University
Jifa Hao, ON Semiconductor
Venue: Carmel

4B - Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
4B.1 - Dielectric Relaxation, Aging and Recovery in High-K MIM Capacitors, Konner E. K. Holden*, Oregon State University, Gavin D. R. Hall, Michael Cook, Chris Kendrick, Kaitlyn Pabst, Bruce Greenwood, Robin Daugherty, Jeff P. Gambino, Derryl D. J. Allman, ON Semiconductor

High-K metal-insulator-metal capacitors are used in many high-performance applications that require both excellent energy storage and minimal energy loss. Often the increase in dielectric permittivity is coupled with an increase in dielectric relaxation or absorption. Additionally, scaling demands that the devices often be used at higher fields, leading to the need to characterize the impact of voltage stress. In this work, the impact of temperature and constant voltage stress on dielectric relaxation in Al_2O_3 MIM capacitors is studied using measurements of the complex permittivity as a function of frequency and time with a measure-stress-measure program. We observe both the degradation of loss parameters extracted from these spectra and the slow recovery over time. We postulate the existence of a potential threshold of temperature acceleration, and a state of permanent irreversible degradation.

09:15 a.m.
4B.2 - A Fast DCIV Technique for Characterizing the Generation and Repassivation of Interface Traps under DC/AC NBTI Stress/Recovery Condition in Si p-FinFETs, Longda Zhou[1,3], Zhaohao Zhang[1,3], Hong Yang[1,3]*, Zhigang Ji[2], Qianqian Liu[1], Qingzhu Zhang[1]*, Eddy Simoen[4], Huaxiang Yin[1,3], Jun Luo[1,3], Anyan Du[1,3], Chao Zhao[1,3], Wenwu Wang[1,3], [1]Institute of Microelectronics, Chinese Academy of Science, [2]Shanghai Jiaotong University, [3]University of Chinese Academy of Sciences, [4]IMEC

A simple fast DCIV technique is demonstrated to measure the time kinetics of ΔN IT during and after DC/AC NBTI stress in Si p-FinFETs. The repassivation of ΔN IT after DC stress is a very fast process and happens within 200 μs recovery time. The delayed recovery phenomenon of ΔN IT is observed only for Mode-B and high f Mode-A AC stress, resulting in the f-dependent ΔN IT under Mode-A AC stress and f-independent ΔN IT under Mode-B AC stress.

09:40 a.m.
4B.3 - Time-Efficient Characterization of Time-Dependent Gate Oxide Breakdwon using Tunable Ramp Voltage Stress (TRVS) Method for Automotive Applications, S C. Hung, S C. Chen, P.S. Chien, Y.S. Cho, Y.-H. Lee, W.S. Hung, Taiwan Semiconductor Manufacturing Company (TSMC)
We develop a new gate oxide reliability test method, called tunable ramp voltage stress. It can perform a quick gate oxide reliability test like breakdown voltage though a ramp voltage stress method, and also receive the data accuracy similar to conventional TDDB, which is a constant voltage stress method. Moreover, we exploit this method to enable large-sample-size measurement. More samples imply lower projection error. This greatly benefits TDDB lifetime projection of devices for automotive applications.

10:05 a.m.
4B.4 - Evaluation Methodology for Assessment of Dielectric Degradation and Breakdown Dynamics using Time-Dependent Impedance Spectroscopy (TDIS), Tomohiro Kuyama, Keiichiro Urabe, Koji Eriguchi, Graduate School of Engineering, Kyoto University

We propose a method to analyze the dielectric degradation and breakdown dynamics under electrical stressing on the basis of time-resolved impedance *Z(ω,t)* spectra—time- dependent impedance spectroscopy (TDIS). Nyquist plots of *Z(ω,t)* show unique features at soft- and hard-breakdown stages for various dielectric films (SiO_2, SiN, and high-k) depending on the defect creation dynamics under electrical stressing. The time evolution of *Z(ω,t)* spectra—*R(t)* and *C(t)*—implies the dynamics of defects (charge trapping/de-trapping features) during stressing in accordance with degradation kinetics. At the post-breakdown stage of high-*k* dielectrics, the *Z(ω,t)* spectra was observed to be distorted, implying the presence of different degenerated phases. This method was also applied to the evaluation of plasma-induced damage to SiN films. The TDIS method is useful for investigating the electrical nature of defects and the degradation and breakdown dynamics of dielectric films.

4B - Authors' Corner
10:30 a.m. – 10:55 am. PDT

Tutorial 12
Tuesday, March 23, 08:45 a.m. – 10:15 a.m. PDT
Ben Kaczer, imec

08:45 a.m.
TuT12 (Tutorial) - DRAM Reliability Overview, Hokyung Park, Seongwan Ryu, SK hynix

As DRAM has been scaled down, reliability issues have been getting worse and new issues have been arisen from new materials, integration schemes, and operation modes. In this tutorial, we will cover reliability mechanisms and current reliability challenges of DRAM's Cell/Core/Periphery transistors, including Row-Hammer, variable retention time (VRT), HEIP, drain off stress, HCI and BTIs.

Tutorial 13
Tuesday, March 23, 08:45 a.m. – 10:15 a.m. PDT
Yi Zhao, Zhejiang University
Maria Toledano Luque, GlobalFoundries

08:45 a.m.
TuT13 (Tutorial) - Hot-carrier Degradation in Si Devices – From Experimental Observations to Accurate Physical Modeling, Stanislav Tyaginov, imec / TU Wien / Ioffe Institute

The breath-taking development of modern microelectronics resulted in transistor dimensions shrunk below tens of nanometres. However, this scaling is being accompanied by a much slower reduction of the supply voltage, thereby resulting in high electric fields in the modern ultra-scaled FETs, which, in turn, substantially shift the carrier ensemble from equilibrium. These non-equilibrium carriers are also called “hot” and responsible for the most detrimental reliability concern in modern FETs, i.e., hot-carrier degradation (HCD). The degradation phenomenon of HCD is very challenging to model because it is driven by the reaction converting neutral precursors (Si-H bonds) to electrically active defects (Pb centers) and this reaction can be triggered by severely non-equilibrium, hot, carriers as well as by multiple cold carriers interacting with the Si/SiO2 interface. Even more cumbersome, HCD can be accelerated/inhibited by self-heating and mixed this another reliability effect of bias temperature instability. This tutorial provides a summary of main characteristic featured of HCD, discusses phenomenological/empirical models, and finally presents physics-based approaches to HCD modeling. Attention will be paid to stochastic modeling of HCD capturing the impact of random dopants and random traps, as well as to coupling with bias temperature instability and selfheating.

Tutorial 14
Tuesday, March 23, 10:15 a.m. – 11:45 a.m. PDT
Christine Hau-Riege, Qualcomm

10:15 a.m.
TuT14 (Tutorial) - Metal reliability for advanced interconnects, Olalla Varela Pedreira, imec

With the continuous transistor scaling, there is a need to reduce the interconnects size, so that the signals, power and ground can be distributed in the circuit. Scaling of Cu interconnect dimensions is becoming increasingly difficult due to the increase in the resistance-capacitance (RC) delay which will cause a degradation in the chip performance. Currently there are two trends that are being researched: One proposal is to replace Cu by other materials (i.e., Co, Ru...) and the second route is to increase the Cu area by scaling the barrier and liner (B/L). The common aspect from both trends is that they need to meet all the reliability requirements. Therefore, metal reliability has become an essential area of research for the semiconductor technology.

This tutorial will begin with the physical and statistical fundamentals of electromigration and stress migration on Al and Cu interconnects. Different test methods, test structures and models will be used for illustrating recent findings on EM and SIV for Cu scaling which include B/L scaling, via prefill schemes and metal capping. Following, reliability aspects of different alternative metals like Co and Ru will be introduced as alternative for Cu. To conclude, new advances on novel integration schemes and their reliability challenges will be discussed.

Tutorial 15
Tuesday, March 23, 10:15 a.m. – 11:45 a.m. PDT
Byoung Min, GlobalFoundries

10:15 a.m.
TuT15 (Tutorial) - Automotive Semiconductor Reliability and its Changed Importance for Complex System Engineering – from Processing Challenges and the Need of Changing Mission Profiles to Reliability / Security Co-Design, Andreas Aal, Volkswagen, Oliver Aubel, GlobalFoundries

The complexity increase of electronic functions in vehicles forces car manufacturers to adapt the electrical system's architecture in order to reduce historically grown and architecture based complexity as well as to optimize complexity management (processes, methods, tools).

Being part of an IoT ecosystem, a car itself becomes a connected entity where data streams enable various new functions and corresponding business models.

However, with respect to reliability this implies two urgent fields of actions. First, automotive electronic systems become strongly software dependent which not only affects the hardware (generation, technology) needed (i.e. AI acceleration), it also causes hardware mission profiles to change over lifetime with central importance to the design-for-reliability process. Second, the increased amount of software algorithm optimized hardware also increases the vulnerability of software based attack windows that focus explicitly on cell-aware aging. Hardware and software based security measures can slow down data processing. To compensate where needed, performance will increase – what is the effect on reliability? The upcoming amount of hardware trojans shows that a much stronger and aligned engagement model along the supply chain is necessary.

Lastly to fulfill requirements of advanced nodes and increased manufacturing challenges – reliability and robustness are essential to meet marked needs.

This tutorial will discuss the above mentioned challenges and also approaches how to deal with them. As reliability aware design for advanced nodes goes down to process design kits, activities regarding standardized mission profiles based on new automotive load categories and classes and their effect on library cell development will also be discussed.

Exhibitor Meet & Greet
11:20 a.m. – 03:00 p.m. PDT

Break
12:10 p.m. – 03:00 p.m. PDT

Career Fair
02:00 p.m. – 03:00 p.m. PDT

This year, a new career fair feature is being introduced at IRPS to allow students and others seeking jobs to meet with prospective employers. The career fair will occur Tuesday afternoon from 2:00-3:00 and may be accessed using the Gathertown feature in the virtual platform.

4D – PK (Packaging and 2.5/3D Assembly)
Tuesday, March 23, 03:00 p.m. – 04:45 p.m. PDT
Prem Chirayarikathuveedu, Consultant
Preeti Chauhan, Google
Venue: Big Sur

4D – Intro
03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
4D.1 (Invited) - Reliability of Optoelectronic Module: An Introduction, John Osenbach, Optical Modules Group, Infinera

Degradation and ultimate failure of Optical and Electronic Multi-Component Packages (O-MCP and E-MCP respectively) are controlled by performance affecting degradation/changes in the materials and joints used in the components and assembly of the MCPs when exposure to the environmental and operational stresses. Environmental stresses include, but not limited to, temperature, humidity, temperature cycling, shock, and vibration. Operational stresses include current, voltage, optical power, power cycling, and temperature. Since most of the materials and devices used in E-MCPs are also used in O-MCPs, many degradation mechanisms are common to both.

03:20 p.m.
4D.2 - Excellent Reliability of Xtacking™ Bonding Interface, Yan Ouyang, Suhui Yang, Dandan Yin, Xiang Huang, Zhiqiang Wang, Shengwei Yang, Kun Han, Zhongyi Xia, Yangtze Memory Technologies Co., Ltd.

XtackingTM is a novel 3D NAND flash architecture, in which memory cell and peripheral circuit are bonded by millions of pairs of metal via. Herein, we explore its reliability to help related workers better understand XtackingTM. The stable electrical properties, intact bonding layer image, unchanged bonding layer strength and unreduced IMD Vbd after ultra-long time environment related stress reflect the excellent reliability of bonding interface. And it is further proved by the followed EM test.

03:35 p.m.
4D.3 - Reliability of Wafer-Level Ultra-Thinning Down to 3 μm using 20 nm-Node DRAMs, Zhwen Chen[1,2], Youngsuk Kim[1,2], Tadashi Fukuda[1], Koji Sakui[1], Takayuki Ohba[1], 1. Tokyo Institute of Technology, 2. DISCO Corporation, 13-11 Omori-Kita 2-chome, Tatsuji Kobayashi[3], Takashi Obara[3], 3. Micron Memory Japan

Ultra-thin DRAMs with 3-5 μm-thick Si wafers have been developed for Wafer-on-Wafer applications. The influences of Cu contamination and backside defects on device reliability were evaluated. The retention characteristics were mainly degraded due to Cu contamination. Increasing the backside defects is useful for improving retardation of Cu contamination. However, the defects also cause degradation of standby currents. Thus, it is important to control the defects carefully to balance the standby currents and the retention characteristics.

03:50 p.m.
4D.4 - Chip to Package Interaction Risk Assessment of FCBGA Devices using FEA Simulation, Meta-Modeling and Multi-Objective Genetic Algorithm Optimization Technique, Moon Soo Lee, Inhak Baick, Min Kim, Seo Hyun Kwon, Myeong Soo Yeo, Hwasung Rhee, Euncheol Lee, Samsung Foundry Business

A chip to package interaction risk assessment platform has been developed using finite element analysis, meta- modeling and genetic algorithm optimization method to tackle increasing variations in package specifications. The results show that the meta-model can efficiently predict BEOL peeling stress and solder von Mises stress of FCBGA device at reflow condition with eleven design variables. Baselines for two critical stresses are determined from qualification and mass production experiences. Room for stress mitigation is also investigated.

4D - Authors' Corner
04:45 p.m. – 05:05 p.m. PDT

4E – RT (Reliability Testing)
Tuesday, March 23, 03:00 p.m. – 04:45 p.m. PDT
Samia Suliman, Penn State
Osama Awadelkarim, Penn State
Venue: Carmel

4E – Intro
03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
4E.1 - Charge Pumping Source-Drain Current for Gate Oxide Interface Trap Density in MOSFETs and LDMOS, Jifa Hao*, Yuhang Sun, Amartya Ghosh, ON Semiconductor

We obtained the interface trap through CP source-drain current, I ds instead of the substrate current, I sub in MOSFETs and LDMOS. We demonstrated that interface trap is same for both I sub and I ds methods when LOCOS is used to separate substrate (body) and source, CP I ds is higher than I sub when STI is used to separate the substrate and source in MOSFETs. We showed CP I ds current is a useful method for interface traps in LDMOS.

03:30 p.m.
4E.2 - Quantifying Region-Specific Hot Carrier Degradation in LDMOS Transistors using a Novel Charge Pumping Technique, Bikram Kishore Mahajan[1]*, Yen-Pu Chen[1], Dhanoop Varghese[2], Vijay Reddy[2], Srikanth Krishnan[2], Muhammad Ashraful Alam[1†], 1. Purdue University, 2. Texas Instruments Inc.

Hot carrier degradation (HCD) has been a persistent reliability challenge for LDMOS since its inception. Unfortunately, classical charge pumping techniques cannot be used to locate/quantify interface defects in traditional source-body tied LDMOS. Here we identify the hot-spots of HCD using TCAD; introduce a novel charge pumping technique for spatial and temporal profiling of the defects, and develop a unified multi hot-spot model to interpret the HCD kinetics in power transistors.

03:55 p.m.
4E.3 - Nanosecond-Scale and Self-Heating Free Characterization of Advanced CMOS Transistors Utilizing Wave Reflection, Wei Liu, Yaru Ding, Liang Zhao, Yi Zhao*, Zhejiang University Hangzhou

We demonstrate a novel nanosecond scale electrical characterization technique utilizing the natural reflection of alternating signals for MOSFETs characterizations. With this method, the Joule heating effect is negligible and the extra stress on device under test (DUT) by the test itself is minimized, which is crucial for certain reliability applications, such as the test of bias temperature instability and self-heating effects.

04:20 p.m.
4E.4 - Machine Learning on Transistor Aging Data: Test Time Reduction and Modeling for Novel Devices, Neel Chatterjee*‡, John Ortega*, Inanc Meric*, Peng Xiao*, Ilan Tsameret*, *Intel Corp., †University of Minnesota

We apply advanced regression techniques for spot measurements, and neural-networks for learning of IV curves to a transistor hot-carrier data set. Models are fit which can generally play back in bias and time. EOL predictions from the advanced regression model are compared with those made from a standard-analysis and options for test-time reduction are explored. The neural-network approach is suggested as a framework for modeling emerging devices where physics-of-failure models may not yet be available.

4E - Authors' Corner
04:45 p.m. – 05:05 p.m. PDT

Tutorial 16
Tuesday, March 23, 03:00 p.m. – 04:30 p.m. PDT
Jason Ryan, NIST

03:00 p.m.
TuT16 (Tutorial) - Reliability and Performance Limiting Defects in 4H SiC Metal Oxide Semiconductor Field Effect Transistors, Pat Lenahan, Penn State

Enormous progress has been made in the development of metal oxide semiconductor (MOS) technology based upon 4H SiC. However, this promising technology is significantly limited by reliability and performance limiting defects. The most important defects are at and very near the SiC/SiO2 interface. Fairly extensive electron paramagnetic resonance studies (EPR) have developed an extensive but not yet complete understanding of the atomic scale structure of defects responsible for these problems. Most of the EPR studies have utilized extremely sensitive electrically detected magnetic resonance (EDMR) detection. These EDMR studies clearly demonstrate links between processing chemistry and the densities of at least some of these defects. In addition, EDMR results elucidate the role they play in limiting device performance and, to some extent, device reliability. Because EDMR directly involves measurements of device currents, they provide direct and completely unambiguous links between defect chemistry and device performance. These studies show that the SiC/SiO2 interface/ near interface defects are far more complex than is the case for the much better understood Si/SiO2 system. In the Si/SiO2 system, interface silicon dangling bond defects called Pb centers usually dominate interface traps. Oxide silicon dangling bond centers called E' centers (often associated with oxygen vacancies) usually play dominating roles in oxide charge trapping. In the 4H SiC/SiO2 system near interface SiC silicon vacancies, nitrogen complexed defects, and carbon and possibly silicon dangling bond centers can, depending on processing parameters, play significant roles in interface trapping. Near interface E' defects can also play important roles in the SiC/ SiO2 system, in a manner somewhat similar to the roles they play in the Si/SiO2 system.

Tutorial 17
Tuesday, March 23, 03:00 p.m. – 04:30 p.m. PDT
Mark Anders, NIST

03:00 p.m.
TuT17 (Tutorial) – Application and characterization of CMOS cryogenic electronics, Pragya Shrestha, NIST

Cryogenic electronics have a wide range of ever-expanding applications, which span everything from quantum information science to extra-terrestrial electronics to gravitational wave research. However, the most prevalent current application pushing the frontiers of cryogenic electronics, is quantum computing where there has become an unavoidable necessity for electronic functionality at the 4 K level. The most promising candidate to fulfil this functionality is CMOS due to its plethora of analog and digital functions at relatively low power consumption to not perturb the cryogenic environment. Due to these stringent power and performance requirements, accurate device models are desirable for consistent circuit design. Though it has been acknowledged that precise characterization is crucial for reliable low power and low temperature circuit design, obtaining reliable device characterization and reliability at low temperatures has not been sufficiently addressed. This tutorial will review the applications of cryogenic CMOS in various fields and discuss the motivation for creating reliable and accurate cryogenic device characterization tools for consistent high-performance cryogenic CMOS circuit design.

Workshops

05:05 p.m. – 05:55 p.m. PDT

WS 1 - Device Reliability
Xavier Federspiel, STmicroe
Souvik Mahapatra, Indian Institute of Technology Bombay (IIT Bombay)

Workshop on BTI and HCD

Bias Temperature Instability (BTI) continues to remain as a crucial reliability concern in CMOS devices. Although it comes in two variants – Negative BTI (NBTI) in PMOS and Positive BTI (PBTI) in NMOS, modern devices with Replacement Metal Gate (RMG) based High-K Metal Gate (HKMG) processes primarily suffers from NBTI while PBTI is negligible.

The physics of NBTI has remained debated, although any model should be able to explain different experiments (as follows) in order to qualify as something meaningful:

• Time kinetics of NBTI during (stress) and after (recovery) DC and AC stress at multiple gate bias (VG) and temperature (T) – preferably T range covering space to automotive applications, and AC stress at multiple duty cycle and frequency.

• Impact of different processes, such as Nitrogen in gate stack, Germanium in channel, device dimension (e.g. fin length/width), layout, etc., on the time kinetics, Vg and T dependence.

However, from a qualification viewpoint, simple empirical models are sufficient to benchmark foundries or process recipes, although care should be taken that the stress and use conditions are not much different to project to operating conditions. Physical models can provide better estimation of end-of-life NBTI.

Hot Carrier Degradation (HCD) depends on channel length (LCH), drain bias (VD) and ratio of drain to gate bias (VD/VG). Classical worst-case projections approaches, such as mid VG (I/O devices or nodes >90nm) or VG=VD (node <90nm) might be sufficient for foundries or process benchmark. However, accurate aging model dedicated to circuit simulation might require refined models taking into account complex VG dependencies, HCD-BTI interaction as well as self-heating effects. As a matter of fact, the BTI-HCD interaction can become a crucial issue especially for PMOS devices, if qualification is done at VG=VD condition, and the situation can get exacerbated due to self-heating effect in modern devices (FDSOI, FinFET, GAA NSFET) with confined channels.

This workshop would focus on the following:

- Overview of BTI mechanism (~15 mins)
- Overview of HCD mechanism in high and low voltage devices (~20 mins)
- Qualification / test methodologies for HCD and BTI (~ 25 mins)
- Choice of stress bias (VG/VD condition) and AC-DC factor
- Decoupling of BTI and HCD
- Impact of self-heating effect (DC vs. AC stress)

WS 2 - SSD Memory
Jay Sarkar, Miicron Technologies

Advances in 3D NAND enable endurance gains, capacity increase, lower power consumption and cost reduction, thus making SSD technology attractive for new applications such as AI and cloud computing. At the same time, 3D NAND exhibits new reliability challenges that affect both the resiliency and performance at the system level, e.g., increased number of bit errors, threshold voltage instabilities, frequent read retries, higher read latency, etc. To cope with these issues, modern NAND controller architectures become complex. Resilient FW/HW co-design is critical to ensure the reliability and performance requirements of modern SSDs. Machine learning can aid by offering a valuable tool for prediction and anomaly detection. Analytics together with domain knowledge can provide valuable insights of failure modes and error events relevant to system reliability. On the other hand, blind application of machine learning algorithms can lead to pitfalls. Representative datasets for training, models that provide interpretability and repeatability of the results are key enablers in this quest.

This workshop will discuss the reliability challenges of modern SSDs and the requirements for new applications such as AI, cloud or edge computing. Another intent is to discuss the role of machine learning and analytics in improving the resiliency of modern SSDs through accurate prognostics and prediction.

WS 3 – BEOL
Ki-Don Lee, Samsung Austin Semiconductor, LLC
Gavin Hall, ON Semiconductor

Background

Since the introduction of dual-damascene Cu and low-k dielectric materials, there has been continuous device scaling from 130nm down to 7nm (and beyond) during the last two decades. Numerous innovations in materials, processes, and models have enabled the new technology node successful and reliable, thanks to the efforts of our fellow scientists and engineers. In this year's IRPS, more innovations are happening, as we have seen papers on Ru interconnects and 7nm EUV Co-liner Cu interconnects.
Today, BEOL reliability evaluation includes electromigration (EM), stress-induced voiding (SV/SIV/SM) and time-dependent dielectric breakdown (TDDB). Looking forward, we must also include environmental factors and more extreme use cases of current and thermally induced inelastic behavior of interconnects under various loadings. How do we incorporate these into an accelerated test framework, in both modeling and verification?
Regarding materials, it is key to understand intrinsic and extrinsic size effects – e.g. linewidths, networks, grain boundaries, twins, and texture - and how these relate to stress and the inelastic response. How do we measure and understand these effects and what technological impact do they have? What are the impacts of mechanical response of next generation materials - Ru, Co, alloys, and barrier integrations, etc. – on the reliability, and how do we measure these?
Attendants are invited to discuss their experiences and experiments in metallization, as well as diagnostic and physical/electrical failure analysis techniques that have helped develop their understanding. Additionally, we would like to discuss the pros and cons of fast test methods available, like wafer-level EM, TVS, isothermal EM, and others for rapid learning cycles in development.

Discussion Topics

- Ru Interconnect / 7nm EUV Co-liner Cu interconnects.
- BEOL challenges for 5nm and beyond (Roadmap for RC delay)
- EM Short Length effect (Blech) in 7nm and below.
- Model selection for BEOL TDDB.
- BEOL reliability of power devices, and heterogeneously integrated solutions

- Metal fatigue in microelectronics
- Physical and electrical evaluations
- Reliability methodology & test

WS 4 - Wide Band Gap SiC
Thomas Aichinger, Infineon Technologies Austria AG
Ronald Green, CIV USARMY CCDC ARL

The strong push to maximize performance to demonstrate the superiority of SiC technology vis-à-vis Si has in some cases increased the significance of potential reliability issues. One particular case where this has occurred is in the short-circuit rating of SiC power MOSFETs. Continual decreases in on-state resistance by varying design parameters such as channel length make these devices more susceptible to failure during a short-circuit event since the saturation current, along with the bus voltage, determines the power dissipation that occurs, which in turn determines how quickly the internal temperature rises to a critical value at which Al begins to melt, or other failure mechanisms begin to engage. This workshop will focus on short-circuit reliability in SiC MOSFETs. A list of topics includes failure mechanisms, test methods, trade-offs between performance and reliability, and where the burden for short-circuit protection should lie.

Discussion topics include:
- Brief overview of failure mechanisms.
- Difference in short-circuit behavior between silicon and SiC power devices.
- Brief overview of test methods used.
- Existing trade-offs between on-state resistance, cost, and short-circuit performance.
- Proposals on how to improve device design to reduce susceptibility to short-circuit fault conditions.
- What is an appropriate short-circuit withstand time for industry acceptance?
- Should the burden be on the device designer or the circuit designer?
- Is short-circuit withstand capability required by the circuit designer; or are device designers trying to match the inherent short-circuit performance of Si devices?
- Need for different trade-off points between performance and reliability, depending on the application.

WS 5 – Neuromorphic
Gennadi Bersuker, The Aerospace Corporation
Marinella Matthew, Sandia National Labs
Kin Leong Pey, Singapore University of Technology and Design

Neuromorphic technologies include variety of materials/structures and applications imposing specific requirements on device characteristics that translates to a rather wide range of conditions for reliability tests. In particular, while in charge storage technologies (floating gate, SONOS, etc.) traditional reliability drivers should also incorporate more strict requirements for analog operations, memory technologies based on a conductance modulation (RRAM, CBRAM, PCRAM, etc.) are controlled by local structural changes that makes these devices extremely sensitive to operation conditions affecting energy emission, specifically the magnitude and duration of applied voltages. Neural algorithms, on the other hand, rely on low variability of device parameters during network operations that further broadens the scope of reliability assessment. Workshop will discuss needs/requirements for test conditions and equipment aroused from NN operations.

WS 6 - HV Transient IEC ESD Design Challenges
(In cooperation with IEW)
Raj Sankaralingam, Texas Instruments
Alan Righter, Analog Devices

On-chip high voltage system level ESD specifications are becoming increasingly common in industrial and automotive applications. In spite of the cost and complexity, designing onchip ESD solutions to be robust to IEC 61000-4-2 have been around for a while and are reasonably well understood. But ensuring those design

techniques are robust to less controlled test methods like the air discharge option of the test, as well as discharge through a choke are quite challenging. The variability resulting from these test methods demand level-triggered non-snapback ESD solutions like PNP-based ESD protection for consistent results. But such solutions consume more IC die area and reduce design margin due to their high clamping voltage. SCRs are a popular choice due to their area efficiency but they suffer from non-uniform conduction when exposed to waveforms with varied rise times and non-monotonic stress pulses. In addition, SCRs need to be designed with care to avoid latch-up during non-ESD fault conditions, in order to prevent EOS failures.

On the validation side, air discharge tests and gun testing through a choke are quite sensitive to the system level test setup and test methods. This often leads to inconsistent test results with snapbackbased ESD solutions as they can affect uniform conduction.

Break
05:55 p.m. – 06:05 p.m. PDT

06:05 p.m. – 06:55 p.m. PDT

WS 7 - Circuit Reliability and Aging: Measurements and Simulations
Valeriy Sukharev, Mentor
Georgios Konstadinidis, Google

In order to determine the chip performance for a given set of design rules, operating voltage and switching speeds, the reliability must be accounted for specific operating conditions. The question is how to account it in right and most effective way. Should we employ the formal approach treating the circuitry as a sequence of elements characterized by known rates of failures, which are traditionally based on the lab data? Or, should we employ more physics-based description of the failure mechanism of the circuitry as a system in the specific environment?

This workshop focuses on the hot topics in the field of circuit reliability:
1. What has been accomplished so far and what should be the path moving forward?
2. ML based approaches are being explored to establish that. Is this the right approach?
3. Are in situ measurements more appropriate to calibrate the models and close the loop?
4. What is the best approach in addressing the extra challenges coming with 3D integration like thermal and mechanical CPI issues to the whole complexity?
5. How to design a chip with a required functionality and performance while satisfying the intended lifetime of the product?

WS 8 - Emerging Memory
Joe McCrate, Micron Technology
Tetsuo Endoh, Tohoku University

Emerging memories have yet to challenge SRAM, eFlash, DRAM, Storage Class Memory (SCM) and NAND/3D-NAND for a large share of the memory market, but continued improvements in performance, cost and reliability of several technologies has brought them closer to the marketplace. Which emerging technologies are most mature and what is gating their widespread adoption? Are reliability challenges a key roadblock for any contending technologies or are performance, cost, or integration the primary challenges? We shall also consider how the potential location of a technology in the memory hierarchy (embedded memory, main memory, storage, or in between such as SCM) dictates reliability requirements.

WS 9 - Automotive for In-car Safety and Security
Udeerna Doppalapudi, Qualcomm
Jyotika Athavale, Nvidia

Background

Safety and security are crucial technologies for the large-scale deployment of autonomous vehicles (AV). They impact the car architecture end-to-end, from hardware to software and system. They impact several phases of the development lifecycle – from specification to validation and operation in the field. There is also a complex interaction between reliability, availability, resiliency, and real time requirements. To address all these challenges, new paradigms are required and the definition of "defectivity" assumes a broader role. Standardization initiatives themselves need to be adapted to this evolved scope.

In addition, AV are becoming more and more AI-enabled and software defined, with a continuous ongoing update of their software functionalities – and also more interconnected with other vehicles, the infrastructure, and the cloud.

This workshop will explore the challenges of the AV architecture and discuss related countermeasures. It will also provide an overview of the new IEEE P2851 standardization project on the development of dependable machines.

Discussion Topics

- Safety Needs
  - Autonomous driving drives need for tighter FIT rates / DPM targets
    - FinFET and future process technology challenges
  - Autonomous driving drives the need for tighter lower defectivity
    - Safety applications and need for better fault tolerance, outgoing quality DPM
  - Autonomous driving drives the need for advanced features and latest standards
    - Latest technology introduced at a faster rate into the automotive market
  - Autonomous driving drives the need for compliance to stringent use conditions
    - Applications requiring mission profiles with higher temp and operating range
  - Connected car use cases driving the market needs
    - Low latency and high performance use cases driving process limits
  - New process technology nodes used in automotive markets
    - Less time to mature the process before it is introduced into the market
- Security Needs
  - SW defined architecture impact
    - System level impact
    - OTA, Car2Cloud, AI use case impact
    - Low Latency and Real time targets for compute consolidate workloads
  - V2X connectivity use cases
    - Potential threats due to 5G use cases concurrent to other technologies in the vehicle

WS 10 - Wide Band Gap GaN
Shireen Warnock, MIT
Matteo Meneghini, University of Padova

GaN is an excellent material for the fabrication of power transistors. These devices are now rapidly finding applications in next-generation power conversion systems with 600-650V transistors already commercially available. Higher voltages are currently targeted (up to 1.2 kV). The success of GaN depends on the understanding of key failure modes and mechanisms. A market transformation is now underway, and the next step is to demonstrate and qualify high reliability.

This workshop focuses on the hot topics in the field of GaN reliability:
1. What are the largest remaining barriers to widespread commercial adoption?
2. Soft vs. Hard switching: What's new? How do you qualify devices in a dynamic regime?
3. GaN devices do not have avalanche capability—Is this a problem or an opportunity?
4. Extrinsic vs. Intrinsic reliability: What are the biggest challenges?

This workshop will address these questions by stimulating discussion on the issues that presently limit the reliability and performance of GaN-based HEMTs. It will be a natural lead-in for the subsequent workshop on SiC reliability.

WS 11 - RF/mmW/5G
Fernando Guarin, GlobalFoundries
Sriram Kalpat, Qualcomm

Background

Given the power, cost structure and integration required for mmW 5G deployment, what gaps remain for Silicon and SiGe to be viable solutions? The market for cellphones, Base Stations and IoT solutions is predicted to explode in the near future. Many companies are in the process of designing their mmW solutions for 5G. In this session we will review the most likely technologies that will dominate the sizable 5G market. Most key players in the industry realize that there is a sizable opportunity for Si and SiGe technology solutions as we transition from the few antennas required in 4G to the multi element antenna array solutions, hence the power requirements have been reduced to a range that is well suited for Silicon and Silicon Germanium technology offerings. Will this be sufficient to displace the proven and well-entrenched RF mmW solutions offered by III-V?

- Which solution will win in the market from the Power
- Cost / Integration
- Reliability
- Operating lifetime requirements
    - EOL, should it be 10 years, 3 years, X years?
- Duty cycle 100%?
- Power requirements for 5G (Linearity/Efficiency) (Handsets and Basestations)
- Translating reliability behavior from device to circuit level – what matters to the end users?
    - Reliability simulator requirements
- Appropriate methods for testing and characterizing RF reliability?
    - Circuit benchmarks, PA, LNA, and Switches
- Scaled DC measurements
- o Setting up device level tests to accurately reflect circuit level benchmarks
    - Associated impact for various classes of circuits/IP blocks.
- Thermal
    - TCAD modeling
- Self-heating
- simulation vs. practical usage

Discussion Topics
- Operating lifetime requirements
    - EOL, should it be 10 years, 3 years, X years?
- Duty cycle 100%?
- Power requirements for 5G (Linearity/Efficiency) (Handsets and Basestations)
- Translating reliability behavior from device to circuit level – what matters to the end users?
    - Reliability simulator requirements
- Appropriate methods for testing and characterizing RF reliability?
    - Circuit benchmarks, PA, LNA, and Switches

- Scaled DC measurements
- o Setting up device level tests to accurately reflect circuit level benchmarks
    - Associated impact for various classes of circuits/IP blocks.
- Thermal
    - TCAD modeling
- Self-heating
- simulation vs. practical usage perspective of?

Wednesday, March 24

Keynote 4
(In cooperation with IEW)
Wednesday, March 24, 08:00 a.m. – 08:45 a.m. PDT
Chris Connor, Intel
Robert Kaplar, Sandia National Labs
Venue: Monterey Main Stage

08:00 a.m.
KN4 (Keynote) - IoT End-node Device: Built to Last, Alessandro Piovaccari, Silicon Labs

End-node IoT devices are aimed to ubiquitous adoption, with projections of over a trillion installed devices within the next 5-10 years. This translates to requirements such as low-energy consumption and long product life cycles while meeting demanding low-cost constraints. From the engineering point of view, upgradeability, security and reliability are among the main issues to solve. Traditional design techniques based on worst case analysis do not provide the required level of optimization in this case which in turn provides ample opportunities for more innovation.
In this keynote, we will show how knowledge of the usage context and application must be used to achieve this complex and multi-faceted goal. Moreover, the fact that these devices are almost always wirelessly connected to the cloud, can be used to our advantage for monitoring and improving their lifetime in the field via methods such as machine learning.

5A – TX (Transistors)
Wednesday, March 24, 08:45 a.m. – 10:55 a.m. PDT
Chetan Prasad, Intel Corporation
Bonnie Weir, Broadcom
Venue: Big Sur

5A – Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
5A.1 - CV Stretch-Out Correction after Bias Temperature Stress: Workfunction Dependence of Donor-/Acceptor-Like Traps, Fixed Charges, and Fast States, T. Grasser*, B. O'Sullivan[o], B. Kaczer[o], J. Franco[o], B. Stampfer*, M. Waltl*, * TU Wien, [o]imec

Capacitance-voltage (CV) measurements are difficult to analze due to the stretch-out. Based on the assumption of a normally distributed density of slow states responsible for this stretch-out, we suggest a simple correction algorithm. We demonstrate the applicability of our method using experimental NBTI/PBTI data on nMOS/pMOS devices to evaluate the workfunction dependence of the various defect types.

09:15 a.m.
5A.2 - Physics-Based Device Aging Modelling Framework for Accurate Circuit Reliability Assessment, Zhicheng Wu*[1], Jacopo Franco, Brecht Truijen, Philippe Roussel, Stanislav Tyaginov, Michiel Vandemaele[1], Erik Bury, Guido Groeseneken[1], Dimitri Linten, Ben Kaczer, imec, [1]ESAT-MICAS

An analytical device aging modelling framework, ranging from microscopic degradation physics up to aged I-V characteristics, is demonstrated.

09:40 a.m.
5A.3 - Time Dependent Variability in Advanced FinFET Technology for End-of-Lifetime Reliability Prediction, Hai Jiang*, Jinju Kim, Kihyun Choi, Hyewon Shim, Hyunchul Sagong, Junekyun Park, Hwasung Rhee, Euncheol Lee, Technology Quality and Reliability Group

Time dependent variability has become a significant concern for End-of-lifetime(EOL) reliability prediction for advanced technology with continuous scaling. In this work, we explore time dependent variability of BTI and HCI on our advanced FinFET technology to demonstrate that Defect-Centric model is a good candidate to describe both of them and there is no obvious difference between 8nm and 7nm for BTI and HCI variation η parameter. Thus, a framework is proposed for BTI and HCI EOL degradation prediction with given ppm criteria.

10:05 a.m.
5A.4 - Analysis of Sheet Dimension (W, L) Dependence of NBTI in GAA-SNS FETs, Nilotpal Choudhury[1,2], Tarun Samadder[1], Ravi Tiwari[1], Huimei Zhou[2], Richard G. Southwick [2], Miaomiao Wang [2], Souvik Mahapatra[1]*, [1]Indian Institute of Technology, [2]IBM Research Division

Ultra-fast (10µs delay) measured threshold voltage shift (ΔV_T) due to Negative Bias Temperature Instability (NBTI) in Gate All Around Stacked Nano-Sheet (GAA-SNS) Field Effect Transistors (FETs) having various length (L) and width (W) are analyzed. An enhanced, fully physical BTI Analysis Tool (BAT) is used to model the measured ΔV_T stress-recovery kinetics at multiple stress bias (V_{GSTR}) and temperature (T), with only four process dependent parameters. The impact of L and W scaling on ΔV_T magnitude and its Voltage Acceleration Factor (VAF) is explained by considering variation in mechanical stress.

10:30 a.m.
5A.5 - **The Properties, Effect and Extraction of Localized Defect Profiles from Degraded FET Characteristics,** Michiel Vandemaele*[†], Ben Kaczer[†], Stanislav Tyaginov[†‡§], Jacopo Francop[†], Robin Degraeve[†], Adrian Chasing[†], Zhicheng Wu*[†], Erik Bury[†], Yang Xiang*[†], Hans Mertens[†], Guido Groeseneken*[†], *ESAT, [†]imec, [‡]Institute for Microelectronics, [§]Ioffe Physical-Technical Institute

We report simulations of localized defect profiles (DPs), typical for hot-carrier degradation (HCD), with exponential- and step-like shapes. First, we analyze how these localized DPs affect the transistor *I-V* and model the complex relation between DP and FET degradation by considering the degraded FET as a series circuit of an undegraded transistor (the source side) and a degraded one (the drain side). We also compare how the same DP causes different degradation for changes in the device structure. Second, we use the DP simulations to qualitatively understand the DP dependence on stress voltages in measured FETs and assess how uniquely a DP can be extracted from degraded *I-V* metrics. The results are of interest for HCD modeling.

5A - Authors' Corner
10:30 a.m. – 10:55 a.m. PDT

5B – EM (Emerging Memory Reliability)
Wednesday, March 24, 08:45 a.m. – 10:30 a.m. PDT
Richard G. Southwick, IBM
Venue: Carmel

5B – Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
5B.1 (Focus) - Reliability of STT-MRAM for Various Embedded Applications, S. H. Han[1], J. H. Lee[2], K. S. Suh[1], K. T. Nam[1], D. E. Jeong[2], S. C. Oh[2], S. H. Hwang[1], Y. Ji[1], K. Lee[2], K. Lee[1], Y. J. Song[2], Y. G. Hong[1], G. T. Jeong[1], 1. Samsung Electronics Co, 2. R&D Center, Samsung Electronics

Owing to tunability of MTJ stack characteristics based on perpendicular magnetic anisotropy control via sophisticated magnetic material engineering, STT-MRAM can meet a wide range of product specifications for various applications: 1) flash-type applications such as microcontroller and AI inferencing device and 2) SRAM-type applications such as frame buffer memory. However each application has different reliability challenges. In this paper, we discuss the reliability requirements for Flash-type and SRAM-type STT-MRAM, verifying superb reliability of highly tunable STT-MRAM technology.

09:15 a.m.
5B.2 (Focus) - Challenges Toward Low-Power SOT-MRAM, Shy-Jay Lin[1]*, Yen-Lin Huang[1]*, MingYaun Song[1], Chien-Ming Lee[1], Fen Xue[2], Guan-Long Chen[3], Shan-Yi Yang[3], Yao-Jen Chang[3], I-Jung Wang[3], Yu-Chen Hsin[3], Yi-Hui Su[3], Jeng-Hua Wei[3], Chi-Feng Pai[4], Shan X. Wang[2], Carlos H. Diaz[1], [1]Taiwan Semiconductor Manufacturing Company, [2]Stanford University, [3]Industrial Technology Research Institute, [4]National Taiwan University

Spin-orbit-torque magnetic random-access memory (SOT-MRAM) equipped with sub-1-V switching voltage [1,2] is considered to be one of the promising candidates for next-generation low-power, high speed and non-volatile embedded cache memory applications. To fulfill these performance requirements, however, there are many technical bottlenecks to be conquered, such as SOT efficiency and scalability. This paper presents the recent progress on SOT-MRAM exploration of CMOS compatible high spin-Hall conductivity materials and structures.

09:40 a.m.
5B.3 - Edge-Induced Reliability & Performance Degradation in STT-MRAM: An Etch Engineering Solution, Simon Van Beek*, Siddharth Rao*, Shreya Kundu*, Woojin Kim*, Barry J. O'Sullivan*, Stefan Cosemans*, Farukh Yasin*, Robert Carpenter*, Sebastien Couet*, Shamin H. Sharifi*, Nico Jossart*, Davide Crotti*, Gouri Kar*, *imec

To enable high density STT-MRAM, process-induced damage needs to be minimized. High temperature anneals and patterning can degrade performance and reliability. By employing a novel patterning scheme, involving physical ion beam etch, etchback and oxidation steps, we minimize the etch-induced damage and limit the oxygen penetration to the free layer, which can degrade device performance. Moreover, we demonstrate better magnetic properties, lower switching voltages and an improved reliability window. We establish BEOL compatibility with a 3-hour, 400°C anneal at the end-of-line and study scaled MTJ arrays with physical diameter of 50 nm.

5B.4 - Variability Sources and Reliability of 3D – FeFETs, Milan Pešić, Bastien Beltrando, Andrea Padovani, Shruba Gangopadhyay, Muthukumar Kaliappan, Michael Haverty, Marco A. Villena, Enrico Piccinini, Matteo Bertocchi, Tony Chiang, Luca Larcher, Applied AI Santa Clara, Jack Strand, Alexander L. Shluger, University College London

Discovery of ferroelectricity (FE) in binary oxides enables the advent of FE memories and a plethora of novel CMOS compatible building blocks spanning from the logic domain to high-density storage and neuromorphic computing. In this paper we develop the first comprehensive model of vertical Ferroelectric Field Effect Transistor, V-FeFET, to identify sources of variability, understand retention problems, and point a path to improving reliability and enabling high- density storage FE memories with extended endurance.

5B - Authors' Corner
10:30 a.m. – 10:55 a.m. PDT

5C – SiC (Wide-Bandgap Semiconductors - SiC)
Wednesday, March 24, 08:45 a.m. – 11:45 a.m. PDT
Thomas Aichinger, Infineon Technologies Austria AG
Daniel Lichtenwalner, Wolfspeed
Venue: Pebble Beach

5C – Intro
08:45 a.m. – 08:50 a.m. PDT

08:50 a.m.
5C.1 (Invited) - Is there a Perfect SiC MosFETs Device on an Imperfect Crystal?, T. Neyer[1], M. Domeij[2], H. Das[3], S. Sunkari[3], [1]ON Semiconductor Germany, [2]Corporate R&D, SiC MosFET Development, ON Semiconductor Germany, [3]SiC Material Development ON Semiconductor

6" Silicon Carbide substrates contain more than 10000 crystal defects per cm^2. A large fraction of those are embedded into active SiC device structures which may cause electrical failures, alter the device performance or significantly reduce the operating life time of individual devices. In this work we provide insights on cause and effect of several types of crystal defects and discuss approaches how to reduce their occurrence, investigate their degradation modes and strategies to eliminate affected dies.

09:15 a.m.
5C.2 - Correlation between MOSFETs Breakdown and 4H-SiC Epitaxial Defects, P. Fiorenza[1], S. Adamo[2], M. S. Alessandrino[2], C. Bottari[2], B. Carbone[2], C. Di Martino[2], A. Russo[2], M. Saggio[2], C. Venuto[2], E. Vitanza[2], E. Zanetti[2], F. Giannazzo[1], F. Roccaforte[1], 1. Consiglio Nazionale delle Ricerche - Istituto per la Microelettronica e Microsistemi (CNR-IMM), 2. STMicroelectronics

The breakdown of 4H-SiC MOSFETs was correlated with the presence of different crystalline defects in the 4H-SiC epitaxial layer. Fowler-Nordheim gate bias conduction was used to screen the MOSFETs. In particular, the devices failing under HTGB stress exhibited an anomalous FN behavior and the presence of a surface bump. Finally, a threading dislocation (TD) was found at the HTRB breakdown location . SPM techniques revealed the increase of the hole concentration close to the defect.

09:40 a.m.
5C.3 - A Straightforward Electrical Method to Determine Screening Capability of GOX Extrinsics in Arbitrary, Commercially Available SiC MOSFETs, Judith Berens, Thomas Aichinger, Infineon Technologies Austria AG

Gate-oxide (GOX) voltage screening is used to sort out MOSFETs with critical extrinsic defects. Higher screening voltages result in higher screening efficiencies and lower FiT rates of delivered products. We present a method to determine the threshold voltage for irreversible oxide damage of arbitrary SiC MOSFETs, which is strongly linked

to the maximum screening voltage. As such, the method provides a straightforward way to indirectly benchmark GOX reliability via the onset voltage of irreversible damage.

10:05 a.m.
5C.4 - Characterization of Early Breakdown of SiC MOSFET Gate Oxide by Voltage Ramp Tests, Yongju Zheng[1], Rahul Potera, Tony Witt, SemiQ Inc.

We studied the behavior of gate oxide breakdown of 1200V 4H-SiC DMOSFETs by voltage ramp, which screens out infant/early failures that could be extrinsic failures in time-dependent-dielectric breakdown tests. The results also indicate that the early failures correlate to the density of large pit defects on epi-wafer and gate area of the devices. An electric field limit on the screening voltage was identified accompanied by negative Vth shift, which can degrade device performance.

10:30 a.m.
5C.5 (Invited) - Space Radiation Effects on SiC Power Device Reliability, Jean-Marie Lauenstein, Megan C. Casey, Ray L. Ladbury, NASA Goddard Space Flight Center, Hak S. Kim, Anthony M. Phan, Alyson D. Topper, Science Systems and Applications

Heavy-ion radiation can result in SiC power device degradation and/or catastrophic failure. Test procedures and data interpretation must consider the impact that heavy-ion induced off-state leakage current will have on subsequent single-event effect susceptibility, testability, and reliability. This work presents test data for diodes, power MOSFETs, and JFETs. Susceptibility to single-event effects is compared between SiC and Si power devices. Initial recommendations on heavy-ion radiation test methods are made and radiation hardness assurance is discussed.

11:20 a.m.
5C.6 - A New Test Procedure to Realistically Estimate End-of-Life Electrical Parameter Stability of SiC MOSFETs in Switching Operation, P. Salmen[1], M. W. Feil[2], K. Waschneck[3], H. Reisinger[2], G. Rescher[4], T. Aichinger[4], [1]Infineon Technologies AG, [2]Infineon Technologies AG, Am Campeon 1-15, [3]Infineon Technologies GmbH & Co. KG, [4]Infineon Technologies Austria AG

We present a new, pulsed-gate stress test approach to determine electrical parameter stability of SiC MOSFETs over a lifetime. We demonstrate that the results of our test procedure reflect most realistically worst-case, end-of-life parameter drifts that occur in typical SiC MOSFET switching applications.

11:45 a.m.
5C.7 - Investigation of Gate Leakage Current Behavior for Commercial 1.2 kV 4H-SiC Power MOSFETs, Shengnan Zhu, Tianshi Liu, Marvin H. White, Anant K. Agarwal, The Ohio State University, Arash Salemi, David Sheridan, Alpha and Omega Semiconductor

The gate leakage current behavior and threshold voltage variation under different gate voltages for commercial 1.2 kV 4H-SiC power MOSFETs have been measured and analyzed. The results reveal insights into different failure mechanisms under different oxide electric fields. It is suggested that the constant-voltage TDDB measurements should be conducted under low gate oxide electrical fields to avoid overestimation of the lifetime under normal operating gate voltage.

5C - Authors' Corner
11:45 a.m. – 12:10 p.m. PDT

Tutorial 18
(In cooperation with IEW)
Wednesday, March 24, 08:45 a.m. – 10:15 a.m. PDT
Gianluca Boselli, Texas Instruments

08:45 a.m.
TuT18 (Tutorial) - Electronic Design Automation (EDA) Solutions for Latch-up Verification in CMOS and HV Technologies, Michael Khazhinsky, Silicon Labs

The verification of latch-up protection networks in CMOS and HV technologies is a difficult challenge. There are several factors including increasing design and process complexity, higher-pin counts, wide operating voltage ranges, and the overall computational difficulties in dealing with large data sets. Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification. These checks are typically focused on layout topology. However electrical information for latch-up risk areas throughout the chip is not readily available. While DRC checks are still useful at early design stages, relying on conventional DRC latch-up checking exclusively, poses a significant risk of missing hidden latch-up pitfalls. Consequently, a fully automated latch-up rule checking approach analyzing electrical information is highly desired. In this tutorial we will review the essential requirements of the latch-up electronic design automation (EDA) verification flow. Then an overview of existing latch-up EDA solutions across the industry will be given. We will introduce generic rules that can be used as basis for a typical latch-up EDA verification flow in CMOS and HV technologies. Finally, recommendations for future EDA tool development and standardization will be provided.

Tutorial 19
(In cooperation with IEW)
Wednesday, March 24, 10:15 a.m. – 11:45 a.m. PDT
Gianluca Boselli, Texas Instruments

10:15 a.m.
TuT19 (Tutorial) - EOS, ESD, Transient, AMR, EIPD, Robustness, Aging - Do All of These Pieces go to the Same Puzzle?, Hans Kunz, Texas Instruments

Electrical Over-Stress (EOS) continues to be one of the largest categories of Customer Returns of Integrated Circuits (ICs). In recent years, there has been resurgence in interest in EOS, including recent attempts by the Industry to better define terms and concepts related to EOS, in hopes of helping suppliers and customers better address the issues. This presentation will examine EOS in relationship to Absolute Maximum Ratings (AMR) and the newly defined term Electrically Induced Physical Damage (EIPD), with an ultimate goal of continuing a conversation about the state of EOS trouble-shooting and how more precise terms and concepts can be harnessed in the process of root-cause analysis. The presentation will also explore relationships between EOS and ESD and contemplate whether combining or separating these categories is ultimately helpful in addressing the EOS problem. Similarly, the relationship between EOS and device Aging will be explored. The complexity of specifying limits for transient events and the complexity of attempting to define or measure EOS robustness will also be discussed.

Exhibitor Meet & Greet
11:20 a.m. – 03:00 p.m. PDT

Break
12:05 p.m. – 03:00 p.m. PDT

5D – EM (Emerging Memory Reliability)
Wednesday, March 24, 03:00 p.m. – 05:10 p.m. PDT
Kai Ni, Rochester Institute of Technology
Venue: Big Sur

5D – Intro
Wednesday, March 24, 03:00 p.m. – 03:05 p.m. PDT

03:05 p.m.
5D.1 (Focus) - Reliability Aspects of Ferroelectric Hafnium Oxide for Application in Non-Volatile Memories, Thomas Mikolajick, Halid Mulaosmanovic, Patrick D. Lomenzo, Uwe Schroeder, Stefan Slesazeck, NaMLab gGmbH, Thomas Mikolajick, Benjamin Max, Institute of Semiconductors and Microsystems

Ferroelectricity in hafnium oxide can solve the scaling issues associated with integrating perovskite based ferroelectric into CMOS processes. With the advent of this new ferroelectric material, basic reliability challenges associated with retention, imprint, fatigue and disturbs in the memory array need to be re- examined. In particular, the high coercive field of ferroelectric hafnium oxide is a double-edged property that helps to enable scaled FeFET devices on the one hand, but also makes the optimization of imprint and field cycling endurance a difficult task. The reliability optimization needs to be specific for the concrete memory concept FeRAM, FeFET or FTJ. This paper summarizes the specific issues for each concept and discusses the current status.

03:30 p.m.
5D.2 – Ultrathin Ferroelectricity and Its Applicationin Advanced Logic and Memory Devices, Sayeef Salahuddin, University of California, Berkeley

Compared to archetypical perovskites, HfO2 based ferroelectric materials are process-compatible with advanced CMOS transistors. As a result, they promise to bring ferroelectric technologies into widespread applications. At the same time, ferroelectricity in these materials is also different. In conventional perovskites, the polarization becomes weaker as the thickness is decreased due to ‘size effects’. Balking this conventional trend, our recent work has shown that ferroelectricity in HfO2 in fact enhances as the thickness goes down.

03:55 p.m.
5D.3 - Elucidating 1S1R Operation to Reduce the Read Voltage Margin Variability by Stack and Programming Conditions Optimization, J. Minguet Lopez, L. Hudeley, L. Grenouillet, D. Alfaro Robayo, J. Sandrini, G. Navarro, M. Bernard, C. Carabasse, D. Deleruyelle[3], N. Castellani, M. Bocquet[2], J. M. Portal[2], E. Nowak, G. Molas, [1]CEA, [2]Aix Marseille Univ, [3]INL CNRS

An extensive experimental study on HfO 2 OxRAM technology co-integrated with GSSN-based Ovonic Threshold Selector (OTS) in 4kb 1S1R memory arrays is coupled with a semi-analytical dynamic model describing OTS switching variability. The 1S1R read voltage margin is quantified statistically, based on OTS switching voltage dispersion, OxRAM variability, and reliability degradation during endurance. 1S1R figures of merit (overall functionality, reliability, and maximum bank size) are optimized depending on OTS and OxRAM devices' features and programming conditions.

04:20 p.m.
5D.4 - Composition Segregation of Ge-Rich GST and its Effect on Reliability, Yung-Huei Lee, P.J. Liao, Vincent Hou, Dawei Heh, Chih-Hung Nien, Wen-Hsien Kuo, Gary T. Chen, Shao- Ming Yu, Yu-Sheng Chen, Jau-Yi Wu, Xinyu Bao, Carlos H. Diaz, TSMC

PCRAM SET/RESET cycling caused GST component segregation. We compared electrical characteristics and failure analysis of GST with different Ge compositions to show how the GST segregation affects reliability. In-situ

TEM anneal revealed Ge-rich films have an inferior GST segregation uniformity compared to Ge2Sb2Te5. This chemical inhomogeneity could be a problem for the Ge-rich PCM array when designing the programming operations due to the broader array resistance distributions induced by the GST segregation.

04:45 p.m.
5D.5 - A Reliable Triple-Level Operation of Resistive-Gate Flash Featuring Forming-Free and High Immunity to Sneak Path, W. Y. Yang[1], E. R. Hsieh[2], C. H. Cheng[1], B. Y. Chen[1], K. S. Li[3], Steve S. Chung[1,*], [1]National Chiao Tung University, [2]National Central University, [3]Taiwan Semiconductor Research Institute

We demonstrated for the first time a triple-level operation of a resistive-gate Flash (RG-Flash) on a FinFET platform. Comprehensive reliabilities have been examined. The results show the forming-free property, low programming (PGM) current (<0.1uA), and ultra-fast PGM time (<10ns), enabling extremely high active energy efficiency, 3 fJ/switching. Furthermore, a multi-level capability featuring a 3-bit-per-cell (8 levels) operation has been demonstrated successfully. We have also achieved more than 10^5 cycles endurance and excellent data retention for each level in 125°C for over one month. The array-level reliability is also evaluated, showing well disturbance-immune during SET/RESET, no sneak-path issues, which keep healthy signal-to-noise margin, with window= 10x between two levels, even if the array is expanded to 1 million-cells size. This work provides a strong candidate for the next generation Flash with resistive switching and CMOS process compatibility.

5D - Authors' Corner
05:10 p.m. – 05:30 p.m. PDT

Tutorial 20
(In cooperation with IEW)
Wednesday, March 24, 03:00 p.m. – 04:30 p.m. PDT
Gianluca Boselli, Texas Instruments

03:00 p.m.
TuT20 (Tutorial) - Exploring Relation of ESD and EMC: Tests, Events to Damage, Failure Types, and Co-Design Approaches, Alan Righter, Analog Devices

This tutorial will explore the events of EMC and ESD as they relate to test methods, damage signatures from the different tests in ICs, and co-design approaches addressing EMC and ESD. First, the various tests will be described and compared to one another. Next common damage signatures for each type of event will be described. With this information, the concept of co-design can be explored to relate to the type of event and the damage signature the co-design is designed to protect. Some co-design tradeoffs may be needed in the consideration of what events are most likely / important in a particular application, but could conflict in co-design, and these will be described.

Tutorial 21
Wednesday, March 24, 03:00 p.m. – 04:30 p.m. PDT
Chetan Prasad, Intel Corporation

03:00 p.m.
TuT21 (Tutorial) - FinFET Self-heating: Measurements, Concerns and Applications, Zakariae Chbili, Intel

FinFET Self-heating has been an emerging reliability concern in advanced nodes. Understanding self-heating measurement results and accuracy is extremely important. In this tutorial we will present several methods for self-heating characterization and a detailed methodology guide. We will also discuss the impact of several parameters on the interpretation of the results. Some parameters include test structure type, layout, location, variability and ambient temperature. Next, we will dive into the impact of self-heating on FEOL reliability mechanisms such as hot carrier and TDDB during characterization and in normal usage, including a case study on a

ring oscillator circuit. Finally, we will show a non-volatile memory application where self-heating is used to improve the programming and retention of the memory device.

Tutorial 22
(In cooperation with IEW)
Wednesday, March 24, 04:30 p.m. – 06:00 p.m. PDT
Gianluca Boselli, Texas Instruments

04:30 p.m.
TuT22 (Tutorial) - Full Chip CDM ESD Verification, Melanie Etherton, NXP Semicon

The nature of CDM ESD events, where charges distributed over the complete IC and package discharge through internal circuitry, results in a challenge for designing ESD robust products without unnecessarily increasing leakage or impacting functional performance. This tutorial provides insight to design and verification strategies that will allow for optimization of ESD protection by providing predictive capabilities for CDM ESD robustness, including complex products with billions of transistors, sensitive analog circuitry and multiple supply domains.

Poster Session
Wednesday, March 24, 05:30 p.m. – 07:30 p.m. PDT
Chris Connor, Intel
Venue: Live in Gather.Town

P1 - Monitoring Setup and Hold Timing Limits, F. Cacho[1], L. Anghel[2], X. Federspiel[1], [1]STMicroelectronics - 850 rue Jean Monnet 38926 Crolles, [2]Univ. Grenoble Alpes

Consideration of Process, Voltage, Temperature and Aging (PVTA) variations in aggressive nanometric technologies is a challenging topic which involve yield, performance, and reliability tradeoff. The delay violation monitors published in the past 20 years in the literature detect critical path setup delay degradations. However, none of them covers potential hold time violations. In this paper, we propose a hold time violation monitor which issue pre-error signals, prior the occurrence of hold time violation.

P2 - Aging of Current DACs and its Impact in Equalizer Circuits, Tonmoy Dhar, Jitesh Poojary, Ramesh Harjani, Sachin S. Sapatnekar, University of Minnesota

This paper illustrates the impact of temporal degradations due to aging on current digital-to-analog converters (IDACs) within the context of a feed-forward equalizer (FFE) that is used in high-speed links. Aging causes mismatch in the current mirror, a matching-critical building block of IDACs, which degrades IDAC performance. The work analyzes and models the effect of mismatch over IDAC performance metrics and demonstrates how this affects FFE behavior. Finally, a novel scheme for FFE recalibration to recover from this degradation is presented.

P3 - BTI Arbitrary Stress Patterns Characterization & Machine-Learning Optimized CET Maps Simulations, L. Gerrer, J. Cluzel, F. Gaillard, X. Garros, Laboratoire de Caractérisation et Test Electrique, X.Federspiel, F.Cacho, D.Roy, E.Vincent, S TMicroelectronics

Dynamic variability remains a major hurdle to microelectronics. To limit its impact circuit designers need effective & accurate degradation models. Despite remarkable efforts in characterizing BTI, the devices are scarcely tested under realistic stresses endured by the device inside a functioning circuit, as done in this work. A machine-learning algorithm elaborates the CET Map used by the RC model. Simulated degradations are in good agreement with measurement for AC and DC and arbitrary stress patterns.

P4 - Mushroom-Type Phase Change Memory with Projection Liner: An Array-Level Demonstration of Conductance Drift and Noise Mitigation, R.L. Bruce[1], S. Ghazi Sarwat[2], I. Boybat[2], C.-W. Cheng[1], W. Kim[1], S R. Nandakumar[2], C. Mackin[3], T. Philip[4], Z. Liu[4], K. Brew[4], N. Gong[1], I. Ok[4], P. Adusumilli[1], K. Spoon[3], S. Ambrogio[3], B. Kersting[2], T. Bohnstingl[2], M. Le Gallo[2], A. Simon[4], N. Li[1], I. Saraf[4], J.-P. Han[1], L. Gignac[1], J.M. Papalia[1], T. Yamashita[4], N. Saulnier[4], G. W. Burr[3], H. Tsai[3], A. Sebastian[2], V. Narayanan[1], M. BrightSky[1,] 1. IBM T.J. Watson Research Center, 2. IBM Research Europe, 3. IBM Research-Almaden, 4. IBM Research - Albany NanoTech

We demonstrate, for the first time, conductance drift and noise mitigation by integrating a projection liner into multi-level mushroom-type PCM devices. Lower drift and low device-to-device variability for devices with projection liner is confirmed with array-level measurements involving over 1,000 devices. Simulations show the inference life span of deep neural network accelerators significantly increases when employing these devices for in-memory computing.

P5 - Modeling and Spectroscopy of Ovonic Threshold Switching Defects, R. Degraeve[1], T. Ravsher[1,2], S. Kabuyanagi[3], A. Fantini[1], S. Clima[1], D. Garbin[1], G.S.Kar[1], [1]imec, [2]KULeuven, [3] Kioxia assigned at imec.

This paper presents a two-state model for OTS defects with a field and temperature-dependent transition. Switching transients of OTS selectors are simulated and the dependence of the threshold voltage on the relaxation time is modeled. A spectroscopic technique to access the physical defect properties is developed and demonstrated on SiGeAsTe.

P6 - Impact of Mechanical Strain on Wakeup of HfO_2 Ferroelectric Memory, A. Kruv[1], S. R. C. McMitchell, S. Clima, O. O. Okudur, N. Ronchi, G. Van den bosch, M. Gonzalez, I. De Wolf[1], J.Van Houdt[2], imec, [1] KU Leuven, Department of Materials Engineering, [2] KU Leuven, Department of Physics and Astronomy

HfO 2 ferroelectric memory has the potential to outperform Flash, yet reliability concerns limit its application. One of them is the cycling required to 'wake-up' the ferroelectric response. Much effort has been put into increasing wake-up efficiency, however, the understanding of strain effects on cycling behavior in multiphasic HfO- 2 is lacking. This work investigates the strain impact on 2P r and 2V c cycling evolution in HfO 2 devices, paving the way for stress engineering for improved device reliability.

P7 - Multilevel Programming Reliability in Si-Doped GeSbTe for Storage Class Memory, G. Lama, M. Bernard, N. Bernier, G. Bourgeois, E. Nolot, N. Castellani, J. Garrione, M. C. Cyrille, G. Navarro*, E. Nowak, Université Grenoble Alpes

Phase-Change Memory (PCM) demonstrated to be a promising memory technology to address Storage Class Memory (SCM) applications that can be distinguished in memory-type and storage-type. In this work, we demonstrate how Si doping in αGST can lead to a huge improvement of multi-level cell (MLC) operations. This result, combined with an improved data retention, proves Si-doped αGST suitability for storage-type SCM, whereas high endurance and high speed in undoped αGST allows to target memory-type SCM.

P8 - Impact of Multilevel Retention Characteristics on RRAM Based DNN Inference Engine, Wonbo Shim[1], Jian Meng[2], Xiaochen Peng[1], Jae-sun Seo[2], Shimeng Yu[1], [1]Georgia Institute of Technology, [2]Arizona State University

The retention characteristics of multilevel HfO 2 RRAM based synaptic array was statistically measured from a 90nm test chip and modeled at different temperatures. Not only the average conductance drifts but also the variance of conductance exacerbates at elevated temperatures. The experimental data are modeled into the DNN (ResNet-18)

simulation with 1-4 weight bit precisions. The inference accuracy drops significantly at 55ºC or above, so further engineering on RRAM retention or circuit/algorithmic techniques are needed.

P9 - Study on the Guard Rings for Latchup Prevention between HV-PMOS and LV-PMOS in a 0.15-µm BCD Process, Chao-Yang Chen[1,2], Jian-Hsing Lee[1], Karuna Nidhi[1], Tzer-Yaa Bin[1], Geeng-Lih Lin[1], Ming-Dou Ker[2], [1]Vanguard International Semiconductor Corporation, [2]National Chiao Tung University

An abnormal lower latchup immunity is really induced by the guard rings which were originally applied to prevent latchup occurrence between the HV-PMOS and LV-PMOS in a 0.15-µm BCD process. The parasitic npn BJT, that exits between the guard rings from HV-NW (biased at high-voltage V_{DDH}) to the LV-NW (biased at low-voltage V_{DDL}), may cause a holding voltage lower than the voltage difference between V_{DDH} and V_{DDL}. To apply the guard rings for latchup prevention, the study results reported in this work are very important to the foundries and the IC design houses.

P10 - Design Optimization of MV-NMOS to Improve Holding Voltage of a 28nm CMOS Technology ESD Power Clamp, Sagar P Karalkar[1], Vishal Ganesan[2], Milova Paul[1], KyongJin Hwang[1], Robert Gauthier[3], GLOBALFOUNDRIES, [2]Wilschdorfer Landstraße 101, [3]Essex Junction

An effective design for medium voltage ESD nMOS power clamp with layout modification of the source junction in 28nm high voltage CMOS technology is presented. Modification of N+/P+ source segmented design of ESD nMOS shows the most efficient ESD power clamp performance in terms of It2/area and holding voltage among other design structure experiments. With having similar It2 performance and area, the segmented GGNMOS has holding voltage of 1V higher than that of the base line GGNMOS for power pad protection. TLP, vf-TLP, HBM and DC-IV characterization techniques were used to characterize the structure.

P11 - A Novel High Voltage Drain Extended FinFET SCR for SoC Applications, Monishmurali M[1], Mayank Shrivastava[1], Indian Institute of Science

Physical insights into missing SCR action in STI DeFinFET SCR is developed. I was found that the missing SCR action in STI-DeFinFET SCR is due to the weak PNP strength. A novel Dual-Fin STI DeFinFET SCR architecture is revealed to address this roadblock, which offered a failure threshold 3X times higher than the conventional device. Furthermore, to investigate the filament behaviour, a 64-Fin Dual-Fin STI DeFinFET SCR is simulated, revealing power scalability issues in them.

P12 - Peculiar Current Instabilities & Failure Mechanism in Vertically Stacked Nanosheet ggN-FET, Monishmurali M[1], Mayank Shrivastava[1], Indian Institute of Science

Vertically-stacked nanosheet N-FET exhibit multiple instability points in their TLP-IV . This is due to non-uniform sheet turn-on and was independent of the presence of body contact. However, this instability was more severe, with a decreased body-source distance. 24-Fin simulations revealed a more severe low-current instability due to non-uniform sheet and fin turn-on. For a smaller body to source contact distance, this non-uniform turn-on was seen to result in an early failure of the device.

P13 - Characterization of NMOS-Based ESD Protection for Wide-range Pulse Immunity, Yasuyuki Morishita, Satoshi Maeda, Renesas Electronics Corporation

Several immunity requirements for electronic systems in automotive, using transient pulses with high energy, often cause EOS damage in automotive IC products. To improve the situation, IC suppliers need further understanding of device operation for the wide-range pulses beyond component level ESD pulses. This paper provides failure

mechanisms for the wide-range pulses in 5V NMOS-based ESD protection which is widely used for the automotive IC products. Through our experimental results, it is clarified that copper interconnects in the ESD protection become more dominant for the pulse immunity beyond several tens of microseconds.

P14 - Estimation of Oxide Breakdown Voltage during a CDM Event using Very Fast Transmission Line Pulse and Transmission Line Pulse Measurements, Chloe Troussier[1,2,3], Johan Bourgeat, Blaise Jacquier, [1]STMicroelectronics SA, 2. CNRS, 3.Univ. Grenoble Alpes, *Institute of Engineering Univ. Grenoble Alpes

Using TLP (Transmission Line Pulse) and VF-TLP (Very Fast Transmission Line Pulse) to emulate a fast transient stress, a study of oxide reliability during a CDM (Charged Devise Model) event was done to establish an empirical law between the time to breakdown and the voltage applied to the gate. A wide array of transistors in different configurations was tested to reflect real situation during a CDM event.

P15 - Investigation of the Failure Mechanism of InGaAs-pHEMT under High Temperature Operating Life Tests, Yasunori Tateno, Ken Nakata, Sumitomo Electric Industries, Akio Oya, Keita Matsuda, Yoshihide Komatsu, Shinichi Osada, Masafumi Hirata, Shigeyuki Ishiyama, Toshiki Yoda, Atsushi Nitta, Tomio Sato, Sumitomo Electric Device Innovations

The purpose of this study is to investigate the physical mechanism of degradation of InGaAs-pHEMT under high temperature operating life (HTOL) tests. Using the measurements of the S-parameters before and after HTOL tests, we found that gate-source and gate-drain capacitance changed as a result of electron capture in the surface recess region. We also performed an operational reliability simulation based on the Reaction-Diffusion Degradation Model. From the results, we concluded that surface depassivation is the main cause of the degradation of InGaAs-pHEMT.

P16 - Time Series Modeling of the Cycle-to-Cycle Variability in h-BN Based Memristors, J. B. Roldán[1], D. Maldonado[1], F.J. Alonso[2], A. M. Roldán[1], F. Hui[3], Y. Shi[4], F. Jiménez-Molinos[1], A.M. Aguilera[2], M. Lanza[5], [1]Dep. Electrónica y Tecnología de Computadores. Universidad de Granada. Facultad de Ciencias, [2]Dep. Estadística e Investigación Operativa. Universidad de Granada. Facultad de Ciencias, [3]Faculty of Materials Science and Engineering, Technion - Israel Institute of Technology, [4] IMEC, [5]King Abdullah University of Science and Technology (KAUST)

We have characterized and modeled memristor devices based on the Au/Ti/multilayer h-BN/Au/Ti stack. Resistive switching (RS) operation has been analysed by extracting the reset and set voltages and currents. The evolution of the set and reset parameters along a RS series was mathematically modeled in a cycle-to-cycle (CTC) basis by means of the Time Series Analysis (TSA). To do so, the Autocorrelation Functions (ACF) and the Partial Autocorrelation Functions (PACF) have been calculated. These tools help to perform a comprehensive variability study and to obtain the corresponding analytical models within the TSA context. Finally, we have included this modeling procedure in a complete compact model such as the Stanford to be able to account for this variability at the circuit level. Experimental current versus voltage ***(I-V)*** curves have been correctly fitted with the model.

P17 - Runtime Variability Monitor for Data Retention Characteristics of Commercial NAND Flash Memory, Matchima Buddhanoy, Sadman Sakib, Biswajit Ray, The University of Alabama in Huntsville

Data retention becomes an important reliability constraint for scaled flash memory. For ensuring data integrity, the storage controller employs several management techniques. The controller algorithm will be enhanced if variability of NAND flash is utilized. In this paper, we investigate variability of data retention characteristics within a given MLC memory after high-temperature bake. We find significant page-to-page and block-to-block variability and show a method to predict the variability based on run-time characterization of memory array.

P18 - The Characterization of Degradation on Various SiON pMOSFET Transistors under AC/DC NBTI Stress, Gang-Jun Kim, Moonjee Yoon, SungHwan Kim, Myeongkyu Eo, Shinhyung Kim, Taehun You, Namhyun Lee, Kijin Kim, Sangwoo Pae, Memory Division Samsung Electronics

The characteristics of the degradation on pMOSFETs which have various SiON gate dielectric under AC/DC NBTI stress were studied. The degradation mechanism of NBTI varied along the nitridation of the gate dielectric. This paper characterized the mechanisms. From the experimental results, the NBTI degradation models considering AC/DC operation of the chip were suggested. Base on the model, the simulation of 512Gb NAND chips was performed, and it was confirmed that no chip failure occurred.

P19 - A Theoretical Framework for Trap Generation and Passivation in NAND Flash Tunnel Oxide during Distributed Cycling and Retention Bake, Tarun Samadder, Satyam Kumar, Karansingh Thakor, Souvik Mahapatra, Indian Institute of Technology Bombay (IIT Bombay)

Memory Reliability Investigation Tool (MERIT) framework, with a generic Reaction-Diffusion-Drift (RDD) model is used to simulate the channel interface (ΔN_{IT}) and bulk oxide (ΔN_{OT}) traps time kinetics in the tunnel oxide (TO) of NAND Flash during Erase-Program (EP) cycling and retention bake after cycling. The generation and passivation of traps are calculated from cycle-to-cycle during distributed EP cycling, and trap passivation is calculated during bake. The framework can model multiple EP cycling phases with varying EP cycling delays, and EP cycling and bake temperature (T). The use of different EP cycling T to mimic the distributed cycling impact is analyzed. The Universal Detrapping Metric (UDM) for various inserted delays and cycling temperatures is verified.

P20 - Efficient Data Recovery Technique for 3D TLC NAND Flash Memory Based on WL Interference, Liu Yang[1,2,3], Qi Wang[1,2,3], Qianhui Li[1,2], Xiaolei Yu[1,2], Jing He[1,2], Zongliang Huo[1,2,3], 1. Institute of Microelectronics of the Chinese Academy of Sciences, 2. University of Chinese Academy of Science, 3. Yangtze Memory Technologies Co. Ltd Beijing

In the paper, WL interference (WI) is used to recharge retention-failed cells to reduce retention error to be lower than ECC correction capability. Voltage region dividing is proposed to inject proper amount of electrons into cells according to their Vth states. Experiment result shows that proposed WI technique outperforms the state-of-the art work , the VSRP technique, in both data recovery capability and data recovery efficiency.

P21 - An Efficient Methodology to Evaluate BEOL and MOL TDDB in Advanced Nodes, S. Jose, C. Yin, Y. Chen, C. M. Hong, M. D. Shroff, NXP Semiconductors, X. L. Zhao, F. Zhang, GLOBALFOUNDRIES

BEOL and MOL TDDB lifetime extrapolations are significantly impacted by process variations as the dielectric processing becomes increasingly complex on advanced technology nodes. In order to evaluate the true intrinsic reliability behavior, the impact of process variations needs to be decoupled. Process variations, when overlooked, can cause sampling artefacts which can affect extrapolated lifetime up to 5 orders of magnitude. We propose an efficient straight-forward method to decouple die-to-die variations from the intrinsic TDDB behavior.

P22 - Assessing SiCr Resistor Drift for Automotive Analog ICs, K.A. Stewart,[1], K. Kimura,[2], M. Ring,[3], K. Noldus,[4], P. Hulse,[5], R.C. Jerome,[1], A. Hasegawa,[6], J.P. Gambino,[1], D.T. Price[1], ON Semiconductor, [1]Gresham, [2]Gunma, Japan, [3] S. Portland, [4] Oudenaarde, [5] Pocatello, [6] Aizu

A very stable resistor is needed for analog integrated circuits employed in harsh automotive environments. Precision SiCr thin-film resistors have been characterized by DC and pulsed I-V measurements, high-temperature operating life, and high temperature storage stress. Maximum current density for a maximum drift of 0.1% over the product lifetime are determined. Furthermore, SiCr resistors are stressed to failure and the physical failure mechanism is analyzed**.**

P23 - Mitigating Switching Variability in Carbon Nanotube Memristors, J. Farmer, W. Whitehead, A. Hall, D. Veksler, G. Bersuker, MTD, D. Gao, Al-Moatasem El-Sayed, T. Durrant, A. Shluger*, Nanolayers Research Computing LTD, *Department of Physics and Astronomy University College London, T. Rueckes, L. Cleveland, H. Luan, R. Sen, Nantero Inc.

Root-cause of instability in carbon nanotubes memristors is analyzed employing ultra-short pulse technique in combination with atomic-level material modeling. Separating various factors affecting switching operations allowed to identify structural features and operational conditions leading to improved cell characteristics.

P24 - Robust RRAM-Based in-Memory Computing in Light of Model Stability, Gokul Krishnan[1]*, Jingbo Sun[1], Jubin Hazra[2], Xiaocong Du[1], Maximilian Liehr[2], Zheng Li[1], Karsten Beckmann[2], Rajiv V. Joshi[3], Nathaniel C. Cady[2], Yu Cao[1], [1]Arizona State University, [2]State University of New York Polytechnic Institute, [3]IBM T. J. Watson Research Center Yorktown Heights

The quality of RRAM-based in-memory computing is limited by many realistic factors, including device non-idealities, periphery circuits, and DNN models. Based on the statistical characterization of 65nm 1T1R RRAM devices, we develop a cross-layer tool that incorporates device, circuit, architecture, and algorithm for system-level evaluation. Furthermore, we propose a novel loss landscape-based DNN model selection for stability, which effectively tolerates device variations and achieves a post-mapping accuracy higher than that with 50% lower RRAM variations.

P25 - Mechanisms of Contact Formation and Electromigration Reliability in Wirebond Packages, A. T. Osmanson[1], M. Tajedini Y.R. Kim[1], H. Madanipour[1], C. Kim[13], B. Glasscock[2], M. Khan[2], 1. University of Texas at Arlington, 2. Texas Instruments

This study explores the interconnect materials' characteristics and their effects on contact area between ball bonds and Al pads in wirebond packages. We believe that an understanding of how the strain hardening effects on the contact area between a ball bond and an Al pad, and thereby on the contact resistance of the wirebond, can allow us to manipulate the package components and materials to yield optimal wirebond packages with desired reliability against electromigration (EM).

P26 - Back Gate Bias Effect and Layout Dependence on RTN in FDSOI Technologies, P. Srinivasan, D. Song, D. Rose, M. LaCroix, A. Dasgupta, GLOBALFOUNDRIES Inc.

The effect of back gate bias and device layout design on Random Telegraph Noise (RTN) behavior is discussed. The effect of RTN on multi-PC fingers fully-depleted Silicon on Insulator (FDSOI) devices were studied in both front gate (FG) and front gate connected to back-gate (FG + BG) condition. Lower RTN induced gate voltage variation is noticed in FG+BG condition than FG. In addition, higher amplitude variation occurs in single-PC devices. Similar level of RTN induced gate voltage variation mean is observed in comparison with bulk FinFET, although the distributions are different.

P27 - Simulation Study of the Origin of Ge High Speed Photodetector Degradation, B. Arunachalam, Université Grenoble Alpes, J.-E. Broquin, Université Grenoble Alpes, Q. Rafhay, Université Grenoble Alpes, D. Roy, STMicroelectronics, A. Kaminski, Université Grenoble Alpes

The reliability of Si photonics and optoelectronics devices is emerging as a major new topic. By using TCAD simulations, this work investigates the microscopic origins of the Ge High Speed Photodetector (HSPD) performance losses during stress obtained in [1]. It confirms the key roles of the carrier lifetime degradation on both dark current increase and photonics current decrease, which could be triggered by surface recombination (SR),

especially at the Buried Oxide (BOX). Other sources of degradation are studied, as fixed charges in the SiO_2 passivation layer and interface state (D_{it}).

P28 - Universal Impacts of Local Electric Fields on the Projected Dielectric Lifetime, Lieyi Sheng, Ihsiu Ho, Quality and Reliability, ON Semiconductor

Presence of interface roughness is shown to enhance local E-fields that increase the acceleration parameter (γ) and reduce Weibull slope (β) in time-dependent-dielectric breakdown. This is qualitatively supported by TCAD, which also show that for the same local enhancement the slope β exhibits a voltage dependency. The errors in γ and in β due to local E-fields add uncertainty to dielectric lifetime projection

P29 - Study of the Microstructure and the Mechanical Properties of Pb-2.5Ag-2Sn Solder Joint, K. Kariya[1], A. Yumiba[2], M. Ukita[1], T. Ikeda[2], M. Koganemaru[2], N. Masago[1], [1] Research & Development Center, Rohm Co., [2]Kagoshima University

In this study the microstructure and the mechanical properties of Pb-2.5Ag-2Sn solder, the most used die attach material for power devices, were investigated. Simple lap joints with different microstructure in the solder joint layer were fabricated by changing the temperature profile of soldering process. From the correlation between the microstructure analysis results and the mechanical properties, it was found that the microstructure of the solder joint layer has a significant effect on the reliability.

P30 - Customized Parallel Reliability Testing Platform with Multifold Throughput Enhancement for Intel Stressing Tests, P. Xiao, H. Hadziosmanovic, M. Klessens, R. Jiang, J. Ortega, D. Schroeder, J. Palmer, I. Tsameret, Intel Corporation

Using a typical Semiconductor Parameter Analyzer (SPA) for semiconductor reliability stress tests has limitations. These issues can be effectively mitigated through the usage of massively parallel reliability tests. This paper presents a new Parallel Reliability Test Platform (PRTP) that has been developed and integrated at Intel Corp. with the support of Intel's test partners. The PRTP was built innovatively by integrating customized and modularized electronic hardware, new parallel probing solutions and in-house developed automation systems.

P31 - Analysis of the Interactions of HCD under "On" and "Off" State Modes for 28nm FDSOI AC RF Modeling, T. Garba-Seybou[1,2], X. Federspiel[1], A. Bravaix[2], F.Cacho[1], (1) STMicroelectronics, (2) ISEN-REER

We present a detailed analysis of the interactions of hot carrier degradation under "On" state and "Off" state". Pulsed stress are used to analyze the frequency dependence of HCD and "off-state". Such approach is required for accurate AC RF ageing modeling. Keywords— CMOS, HCI, RF, interaction, off-state, reliability, energy-driven hot carrier model, hot hole traps

P32 - A Defect Characterization Technique for the Sidewall Surface of Nano-Ridge and Nanowire Based Logic and RF Technologies, A. Vais, B. Hsu[1], O. Syshchyk[1], H. Yu, A. Alian, Y. Mols, K. V. Kodandarama, B. Kunert, N. Waldron, E. Simoen[2], N. Collaert, imec Leuven, [1] ESAT, [2] Universiteit Ghent

We introduce a set of new characterization techniques for the direct defect analysis of the sidewall surfaces of Nano-ridge, Nanowire, and FinFET based devices, being used in current (and future) logic and RF technologies. We demonstrate the application of these techniques on GaAs mesa, Nano-ridge, and InGaAs nano-wire based PIN diodes where surface defect densities are difficult to extract currently. We show that a close match in extracted density, with both measured data and calibrated TCAD simulations of above device types, is achieved validating the applicability of the techniques.

P33 - Effects of Temperature and Supply Voltage on Soft Errors for 7-nm Bulk FinFET Technology, A. Feeley, Y. Xiong, B. L. Bhuva, Vanderbilt University, B. Narasimham, Broadcom Inc., S.-J. Wen, R. Fung, Cisco Systems

Integrated circuits are expected to operate across a wide range of temperatures and supply voltages. At the 7-nm FinFET technology node, the self-heating of individual transistors may further increase local temperatures on a die. The combined effects of supply voltage variations and elevated temperatures on soft-error rates for the 7-nm node are investigated. Results show increased sensitivity to soft errors at reduced supply voltage and elevated temperature conditions due to decreased charge collection.

P34 - Frequency, LET, and Supply Voltage Dependence of Logic Soft Errors at the 7-nm Node, Y. Xiong, A. Feeley, L.W. Massengill, B.L. Bhuva, Vanderbilt University, S.-J. Wen, R. Fung, CISCO Systems Inc.

Logic soft-error rates are expected to exceed latch soft- error rates at advanced technology nodes due to operating frequencies in the GHz range. Predictive models for logic soft- errors need difficult-to-obtain data for single-event transient pulse widths. This work proposes an empirical method for estimating logic soft-error rates using shift registers designed with conventional D flip-flops at the 7-nm node. Availability of this model will provide insight to designers on logic soft-error contributions during the design stages.

P35 - Gate Driver Protection Methods for SiC MOSFET Short Circuit Testing, Jairo Nevarez, Anthony Olmedo, Rachel Williams, Polina Pechnikova, Wolfspeed - A Cree Company

Gate circuit protection methods are necessary to protect the short circuit system and its gate driver. This paper proposes the following methods- the double ended Zener diode clipping protection and the gate source capacitor protection. The added gate driver protection saves not only in testing system down time, but also in repair cost. The added gate protections are a catalyst to the short circuit system without degrading the short circuit test and results.

P36 - Methodology to Improve Safety Critical SoC Based Platform: A Case Study, Ooi Michael, Loo Tung Lun, Koay Eng Keong, Intel Corp PG12 Halaman Kampung Jawa

Machine Hazard Risk is dangerous if failure affects humans. Systematic methodology to designing SIL compliant appliances that use SoCs without safety entity paired with safety micro-controller as a platform solution. Important system level considerations and learning range from BIOS enhancement to platform level connectivity choices to monitors and failure prediction is covered in the paper. Conference participants will learn about the methodology through a proof of concept done on a Core platform and Arduino micro-controller .

P37 - Comparative Study on the Energy Distribution of Defects under HCD and NBTI in Short Channel p-FinFETs, Hao Chang[1,3], Longda Zhou[1,3], Hong Yang[1,3]*, Zhigang Ji[2], Qianqian Liu[1], Eddy Simoen[4], Huaxiang Yin[1,3], Wenwu Wang[1,3]*, [1]Institute of Microelectronics, [2]Shanghai Jiaotong University, [3]University of Chinse Academy of Sciences, [4]IMEC

A comparative study is carried out to clarify the energy distribution of traps under hot carrier degradation (HCD) and negative bias temperature instability (NBTI) in short channel p-FinFETs. Two sources of traps, pre-existing traps and generated traps, are identified and their energy profiles are separated using Discharging-based Multi-pulse (DMP) method. The pre-existing traps are located below valance band of silicon (E_v), while the two generated traps are located in 0.4eV above E_v and near conduction band (E_c) of silicon, respectively. The two generated traps are highly sensitive to stress voltage and stress time under NBTI and HCD, however, the generated trap 1 is more sensitive to stress temperature than generated trap 2 under HCD. When switching to long channel devices, the overall degradation is reduced due to less trap generation.

P38 - Traps Based Reliability Barrier on Performance and Revealing Early Ageing in Negative Capacitance FET, Aniket Gupta[1], Govind Bajpai[1], Priyanshi Singhal[1], Navjeet Bagga[2], Om Prakash[3], Shashank Banchhor[4], Hussam Amrouch[5], Nitanshu Chauhan[1,4]*, [1]National Institute of Technology Uttarakhand, [2]PDPM-IIITDM Jabalpur, [3]Karlsruhe Institute of Technology (KIT), [4]Indian Institute of Technology Roorkee, [5] University of Stuttgart

This work demonstrates the individual and combined impact of Si-SiO_2 interface traps *(N_{it})* and Ferroelectric (FE) bulk traps (*N_{bulk})* on the performance of p-NC-FDSOI FETs. We found: 1) The high interface electric field and trap induced polarization variation causes early aging effect; 2) Performance degradation due to FE N_{bulk} in p-NC-FDSOI FET; 3) The combined effect of N_{it} and N_{bulk} predominantly degrades the performance of p-NC-FDSOI FET as compare to the baseline p-FDSOI FET.

P39 - HCI Temperature Sense Effect from 180nm to 28nm Nodes, X. Federspiel, A. Camara, A. Michard, C. Diouf, F. Cacho, STMicroelectronics

Since the introduction of finfets and FDSOI, many publications presented HCI – self heating deconvolution methods, because the self-heating is significantly higher than in bulk technologies. All these works used HCI temperature activation energy Ea to renormalize stress. We will show here, that across various technologies, using apparent Ea can induce significant errors since temperature sense effect can represent up to 50% of the apparent measured value.

P40 - Impacts of Depth and Lateral Profiles of Fluorine Atoms in Gate Oxide Films on Reliability, Shuntaro Fujii, Shohei Hamada, Tatsushi Yagi, Isao Maru, Shogo Katsuki, Toshiro Sakamoto, Atsushi Okamoto, Soichi Morita, Tsutomu Miyazaki, Asahi Kasei Microsystems

Fluorine (F) implantation into gate poly-Si was used to incorporate F atoms in gate oxide films. Different F profiles in depth direction of gate oxide films were prepared. Enhanced segregation of F atoms at SiO_2/Si interfaces was important for improvement of time dependent dielectric breakdown (TDDB) lifetime and suppression of hot carrier degradation. TDDB and low frequency noise dependences on gate length suggested that F profiles in lateral direction of gate oxide films should be cared for reliability of short channel devices.

P41 - Stochastic and Deterministic Modeling Frameworks for Time Kinetics of Gate Insulator Traps during and after Hot Carrier Stress in MOSFETs, Satyam Kumar, Tarun Samadder, Karansingh Thakor, Uma Sharma, Souvik Mahapatra, Indian Institute of Technology Bombay (IIT Bombay)

A stochastic Reaction-Diffusion-Drift (RDD) model framework is proposed for trap time kinetics under Hot Carrier Degradation (HCD) stress and post-stress conditions. Consistency of the 3-D stochastic RDD, 3-D TCAD incorporated deterministic RDD and an "equivalent" 1-D deterministic RDD frameworks is shown. Measured HCD kinetics is decoupled into contributions by pure HCD and Bias Temperature Instability (BTI). The pure HCD time kinetics during and after stress is modeled using the above frameworks. Lack of recovery for the pure HCD component after stress is explained.

P42 - Comparison of Analog and Noise Performance between Buried Channel Versus Surface Devices in HKMG I/O Devices, L. Pirro, A. Jayakumar, O. Zimmerhackl, D. Lipp, R. Illgen, A. Muehlhoff, R. Pfuetzner, A. Zaka, M. Otto, J. Hoentschel, GLOBALFOUNDRIES Fab1 LLC & Co.KG, Y. Raffel, K. Seidel, R. Olivo, Fraunhofer-IPMS

In this work buried channel devices were successfully integrated in HKMG. Analog, noise and reliability performance have been reported and compared to a surface device. The devices were processed to have the same

V_{Tsat} for the nominal geometry of a corresponding surface device. Advantages and drawbacks of the two integrations are discussed and explained with the support of calibrated TCAD simulations.

P43 - Aging Models for n-and p-type LDMOS Covering Low, Medium and High V_{GS} Operation, Guido T. Sasse[1], Vignesh Subramanian[1], Ljubo Radic[2], NXP Semiconductors, [1]Nijmegen, [2]Chandler

In this paper, we present aging models to describe degradation in LDMOS transistors covering the full V_{GS}/V_{DS} space that the devices see during operation. Three distinct regions are identified that require dedicated modelling: low V_{GS} (off-state), medium V_{GS} (on-state) and high V_{GS} regime. Models are presented for both n-type and p-type LDMOS and verified with experimental data.

P44 - "Pinch to Detect": A Method to Increase the Number of Detectable RTN Traps in Nano-Scale MOSFETs, Angeliki Tataridou, Gérard Ghibaudo, Christoforos Theodorou, IMEP-LAHC, *Institute of Engineering Univ. Grenoble Alpes

This work presents a new methodology for the characterization of RTN in nanometer length MOSFETs, detecting a maximum number of active RTN traps. The channel pinch-off effect can be used for the modulation of RTN amplitudes and kinetics, which leads to the appearance of new RTN signals. It is shown that the combination of measurements for three different channel shapes increases the total number of detectable RTN traps. This conclusion is supported by TCAD simulations.

P45 - Reliability-Conscious MOSFET Compact Modeling with Focus on the Defect-Screening Effect of Hot-Carrier Injection, Pratik B. Vyas[1], Ninad Pimparkar[1], Robert Tu[1], Wafa Arfaoui[2], Germain Bossu[2], Mahesh Siddabathula[2], Steffen Lehmann[3], Jung-Suk Goo[1], Ali B. Icel[1], [1]GLOBALFOUNDRIES U.S. Inc., [2]Reliability Engineering, [3]GLOBALFOUNDRIES Dresden Module One LLC & Co. KG

As the reliability qualification poses a major concern in advanced-node CMOS technologies, accurate aging prediction becomes crucial in the circuit design. The HCI (Hot-Carrier Injection) induced aging is so complicated that its modeling is often significantly simplified, focusing on digital circuits. We present here a novel reliability-conscious compact modeling method that can accurately calibrate the full post-HCI-stress I-V characteristics of the MOSFET, taking into the account the observed defect-screening effect.

P46 - ON-State Reliability of GaN-on-Si Schottky Barrier Diodes: Si_3N_4 vs. Al_2O_3/SiO_2 GET Dielectric, Eliana Acurio, Universidad San Francisco de Quito Quito, Lionel Trojman, LISITE, IMNE, Brice de Jaeger, imec, Benoit Bakeroot, CMST, imec & Ghent University, Stefaan Decoutere, imec

This paper aims to study the reliability of GET-SBDs fabricated on 650-V GaN-on-Si buffers considering single and multilayer dielectrics with different materials (Si 3 N 4 and Al 2 O 3 /SiO 2). It has been demonstrated that Al 2 O 3 /SiO 2 dielectric yields better reliability and lower variability across the wafer suggesting a better quality of the AlGaN-barrier/dielectric interface and more uniform process control than with Si 3 N 4 dielectric. It makes Al 2 O 3 /SiO 2 dielectric a more attractive option for the 650V AlGaN/GaN SBDs technology.

P47 - Robustness of GaN Gate Injection Transistors under Repetitive Surge Energy and Overvoltage, Joseph P. Kozak*, Qihao Song, Ruizhe Zhang, Jingcun Liu, Yuhao Zhang*, Virginia Polytechnic Institute and State University

This work studies the robustness of the GaN gate injection transistor (GIT) under repetitive overvoltage events implemented at the device hard-switched turn-off. A clamped, inductive switching circuit with a 400 V dc bias is used to generate the overvoltage stress events with different overvoltage magnitude up to 1050 V (90% of the device

destruction limit) and different switching periods. The GITs show no failure or permanent degradation in electrical parameters after 1-million stress events.

P48 - Study on Avalanche Uniformity in 1.2KV GaN Vertical PIN Diode with Bevel Edge-Termination, Ke Zeng, Srabanti Chowdhury, Stanford University, Brendan Gunning, Robert Kaplar, Sandia National Labs, Travis Anderson, Naval Research Lab

GaN vertical PIN diodes with different bevel edge termination angles were fabricated on three wafers with varying p-layer doping concentrations, respectively. The breakdown behavior in terms of the breakdown voltage and the electroluminescence were studied as functions of these variables. The repeatable avalanche breakdown and highest breakdown voltage were measured with the lowest p doping of $3x10^{17}$ cm^{-3} and with the lowest bevel angle, indicating the efficacy of the bevel edge termination under these specific circumstances. As p-layer doping increases and the bevel angle becomes steeper, the devices exhibit lower breakdown voltages and less robust breakdown characteristic, often destructive. From this study, we also conclude that at very high p-layer doping of 2×10^{19} cm^{-3}, the bevel etch alone cannot provide an effective edge termination.

P49 - Investigation on VTH and RON Slow/Fast Drifts in SiC MOSFETs, M. Cioni[1], A. Bertacchini[2], A. Mucci[1], G. Verzellesi[2], P. Pavan[1], A. Chini[1], 1. Dipartimento di Ingegneria "Enzo Ferrari", 2. Dipartimento di Scienze e Metodi dell'Ingegneria

RON and VTH drifts in TO-247 SiC packaged MOSFETs are investigated in this paper. The use of a novel on-the-fly measurement setup able to capture their variation over a 100µs to 1000s time range revealed the presence of two separated fast and slow mechanisms affecting the VTH and RON stability.

P50 - Advancing Static Performance and Ruggedness of 600V SiC MOSFETs: Experimental Analysis and Simulation Study, Dongyoung Kim, Nick Yun, Woongje Sung, State University of New York Polytechnic Institute Colleges of Nanoscale Science and Engineering

600V MOSFETs were fabricated on 6-inch 4H-SiC substrates. Channel lengths and JFET widths were varied to study their impact on the on-state performances and blocking behaviors. Based on physical cross-sectional SEM analyses of fabricated 600V MOSFETs, new structures were proposed to further improve the static and short circuit performances. Both static and non-iso thermal, mixed mode-simulations were conducted to support the novelty of the proposed structures. 3rd quadrant I-V behavior is also discussed.

P51 - Effect of Interface and Bulk Charges on the Breakdown of Nitrided Gate Oxide on 4H-SiC, B. Mazza[1-2], S. Patane[2], F. Cordiano[1], M. Giliberto[1], G.Renna[1], A.Severino[1], E.Zanetti[1], M. Boscaglia[1], G.Franco[1], 1. STMicroelectronics, 2. Dipartimento di Scienze Matematiche ed Informatiche

The disadvantage of 4H-SiC/SiO_2 compared to the Si/SiO_2 interface is the high trap density limiting the channel mobility and gate oxide stability and often leads to early failure in power MOSFETs. One important process improvement is the nitridation of the oxide. In this work, we investigate techniques to characterize and quantify the nitridation effect, validating the better performance after NO nitridation due to passivation of near interface oxide traps (NIOTs) and bulk charges as well as an improved gate oxide reliability.

P52 - Investigation of the Bipolar Degradation of SiC MOSFET Body Diodes and the Influence of Current Density, S. Palanisamy[1], T. Basler[1], J. Lutz[1], C.Künzel[1], L.Wehrhahn-Kilian[2], R.Elpelt[2], Technische Universität Chemnitz, Germany[1], Infineon Technologies AG[2]

Bipolar degradation continues to be a key issue that should be taken into account in 4H-SiC devices using bipolar operation modes. The generation and expansion of recombination-induced stacking faults (SFs) in 4H-SiC devices results in a forward-voltage drift, which has been widely discussed in the literature. In this work, 1.2 kV SiC MOSFET body diodes were stressed at different current densities to investigate the influence of crystal-induced voltage drifts like bipolar degradation caused by stacking faults (SFs), expansion from pre-existing basal plane dislocations (BPDs) or conversion points. Additionally, thermomechanical failures (gate-oxide damage, front-side metallization degradation, bond-wire heel crack and lift-off) inevitably occurred due to high surge-current stress. The measurement results illustrate the spectrum of degradation by applying different current densities to the body diode of SiC MOSFETs.

P53 - Accuracy of Thermal Analysis for SiC Power Devices, S. Race[1], T. Ziemann[1], S. Tiwari[1], I. Kovacevic-Badstuebner[1], U. Grossner[1], Advanced Power Semiconductor Laboratory

Thermal analysis of Silicon Carbide (SiC) power semiconductor packages is a crucial design step to ensure highly reliable device performance at elevated temperatures. This paper analyzes the thermal behavior of SiC power semiconductor packages by means of comprehensive FEM simulations, allowing to more precisely determine the error of the temperature estimation based on the square-root-t approximation for SiC power devices.

Closing Ceremony - Prize Drawing & IRPS 2022 Announcement
Wednesday, March 24 07:30 p.m. – 08:30 p.m. PDT
Robert Kaplar, Sandia National Labs
Charlie Slayman, Cisco Systems
Venue: Monterey Main Stage